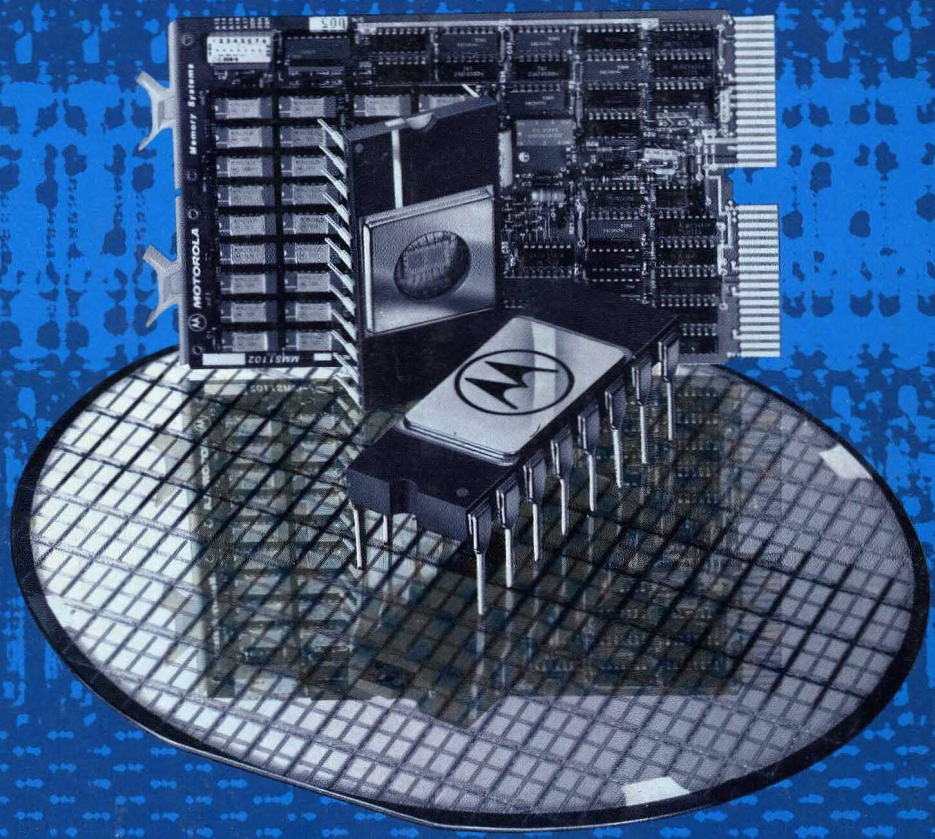
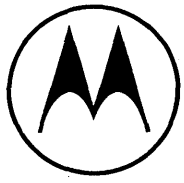
MOTOROLA MEMORY DATA





MOTOROLA

MEMORIES

Prepared by
Technical Information Center

Motorola has developed a very broad range of MOS and bipolar memories for virtually any digital data processing system application. Complete specifications for the individual circuits are provided in the form of data sheets. In addition, selector guides are included to simplify the task of choosing the best combination of circuits for optimum system architecture.

New Motorola memories are being introduced continually. For late releases, additional technical information or pricing, contact your nearest authorized Motorola distributor or Motorola sales office.

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Series A

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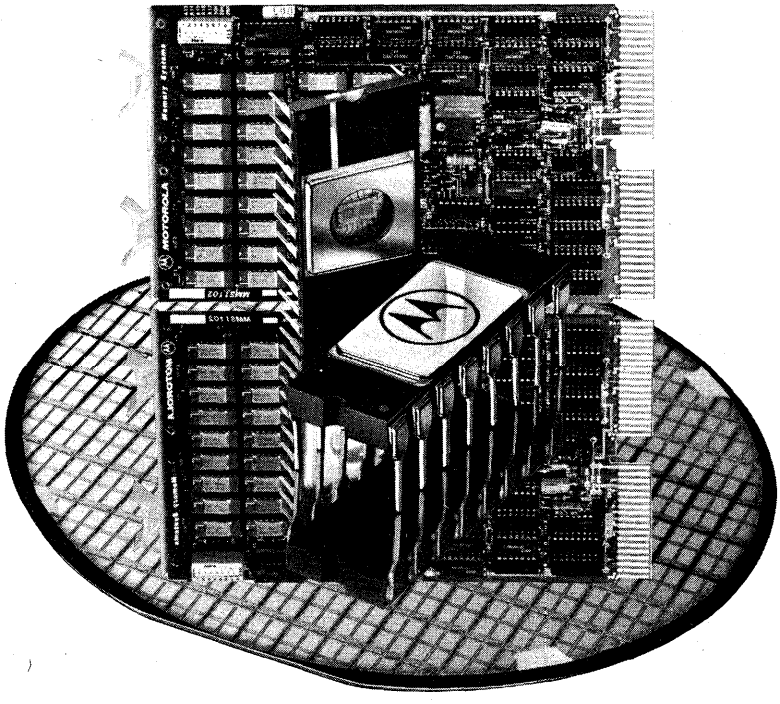
SELECTOR GUIDES CROSS-REFERENCE

1



MEMORIES SELECTION GUIDE

NOTES

Boldface denotes industry standard part numbers.

Operating temperature ranges —
MOS: 0°C to 70°C
CMOS: -40°C to 85°C and -55°C to +125°C
ECL: Consult individual data sheets
TTL: Military, -55°C to +125°C; Commercial, 0°C to 70°C

FOOTNOTES

ss Second source

1 MOS power supplies —
Three +12, ±5 V
One +5 V
All MOS outputs are three-state except the 6570 and 6580 series which are open-collector.

2 Character generators include shifted and unshifted characters, ASCII, alphanumeric control, math, Japanese, British, German, European, and French symbols.

RAMs

Organization	Part Number	Access Time (ns max)	Number of Power Supplies[1]	Number of Pins	Second Source
MOS DYNAMIC RAMs					
4096 × 1	MCM**4096**-6	250	3	16	*ss*
4096 × 1	MCM**4096**-16	300	3	16	*ss*
4096 × 1	MCM**4096**-11	350	3	16	*ss*
4096 × 1	MCM**4027A**-2	150	3	16	*ss*
4096 × 1	MCM**4027A**-3	200	3	16	*ss*
4096 × 1	MCM**4027A**-4	250	3	16	*ss*
4096 × 1	MCM6604A	350	3	16	
4096 × 1	MCM6604A-2	250	3	16	
4096 × 1	MCM6604A-4	300	3	16	
4096 × 1	MCM6605A	300	3	22	
4096 × 1	MCM6605A-2	200	3	22	
16,384 × 1	MCM**4116A**-15	150	3	16	*ss*
16,384 × 1	MCM**4116A**-20	200	3	16	*ss*
16,384 × 1	MCM**4116A**-25	250	3	16	*ss*
16,384 × 1	MCM**4116A**-30	300	3	16	*ss*
16,384 × 1	MCM4516A-15*	150	1	16	*ss*
65,536 × 1	MCM6664A-15*	150	1	16	*ss*
MOS STATIC RAMs					
128 × 8	MCM6810	450	1	24	
128 × 8	MCM68A10	360	1	24	
128 × 8	MCM68B10	250	1	24	
1024 × 4	MCM**2114**-20	200	1	18	*ss*
1024 × 4	MCM**2114**-25	250	1	18	*ss*
1024 × 4	MCM**2114**-30	300	1	18	*ss*
1024 × 4	MCM**2114**-45	450	1	18	*ss*
1024 × 4	MCM**21L14**-20	200	1	18	*ss*
1024 × 4	MCM**21L14**-25	250	1	18	*ss*
1024 × 4	MCM**21L14**-30	300	1	18	*ss*
1024 × 4	MCM**21L14**-45	450	1	18	*ss*
1024 × 1	MCM2115A	45	1	16	
1024 × 1	MCM2125A	45	1	16	
4096 × 1	MCM6641-20	200	1	18	*ss*
4096 × 1	MCM6641-25	250	1	18	*ss*
4096 × 1	MCM6641-30	300	1	18	*ss*
4096 × 1	MCM6641-45	450	1	18	*ss*
4096 × 1	MCM66L41-20	200	1	18	*ss*
4096 × 1	MCM66L41-25	250	1	18	*ss*
4096 × 1	MCM66L41-30	300	1	18	*ss*
4096 × 1	MCM66L41-45	450	1	18	*ss*
4096 × 1	MCM**2147**-55*	55	1	18	*ss*
4096 × 1	MCM**2147**-70*	70	1	18	*ss*
4096 × 1	MCM**2147**-85*	85	1	18	*ss*

*To be introduced.

See Notes on Page 1-2.

MEMORIES SELECTION GUIDE (continued)

CMOS STATIC RAMs

Organization	Part Number	Access Time (ns max)	Number of Power Supplies	Number of Pins	Second Source
64 × 1	MCM14505	180**	1	14	
256 × 1	MCM14537	700**	1	16	
64 × 4	MCM14552	700**	1	24	
256 × 4	MCM145101-1	450	1	22	ss
256 × 4	MCM145101-3	650	1	22	ss
256 × 4	MCM145101-8	800	1	22	ss
4096 × 1	MCM146504	450	1	18	ss
1024 × 1	MCM146508*	460	1	16	ss
1024 × 1	MCM146508-1*	300	1	16	ss
1024 × 1	MCM146518*	460	1	18	ss
1024 × 1	MCM146518-1*	300	1	18	ss

**Typical access time @ V_{DD} = 10 Vdc.

ECL BIPOLAR RAMs

Organization	Part Number	Access Time (ns max)	Output	Number Pins	Second Source
8 × 2	MCM10143	15	ECL Output	24	
256 × 1	MCM10144	26	ECL Output	16	ss
16 × 4	MCM10145	15	ECL Output	16	ss
1024 × 1	MCM10146	29	ECL Output	16	ss
128 × 1	MCM10147	15	ECL Output	16	ss
16 × 4	MCM10148	15	ECL Output	16	
256 × 1	MCM10152	15	ECL Output	16	ss

TTL BIPOLAR RAMs

256 × 4	MCM93412*	45	Open-Collector	22	ss
256 × 4	MCM93422*	45	Three-State	22	ss
1024 × 4	MCM93415*	45	Open-Collector	16	ss
1024 × 4	MCM93425*	45	Three-State	16	ss

*To be introduced.

See Notes on Page 1-2.

EPROMs

Organization	Part Number	Access Time (ns max)	Number of Power Supplies[1]	Number of Pins	Second Source
MOS EPROMs					
1024 × 8	MCM**2708**	450	3	24	*ss*
1024 × 8	MCM27A08	300	3	24	*ss*
1024 × 8	MCM68708	450	3	24	*ss*
1024 × 8	MCM68A708	300	3	24	
2048 × 8	TMS**2716**	450	3	24	*ss*
2048 × 8	TMS27A16	300	3	24	*ss*
2048 × 8	MCM**2716***	450	1	24	*ss*
2048 × 8	MCM27A16*	350	1	24	*ss*
4096 × 8	MCM2532*	450	1	24	
8192 × 8	MCM68764*	450	1	24	*ss*

PROMs

Organization	Part Number	Access Time (ns max)	Output	Number Pins	Second Source
ECL PROMs					
32 × 8	MCM**10139**	25	ECL Output	16	*ss*
256 × 4	MCM**10149**	30	ECL Output	16	*ss*
TTL PROMs					
64 × 8	MCM5003/5303	125	Open-Collector	24	*ss*
64 × 8	MCM5004/5304	125	2K Pull-Up	24	*ss*
512 × 4	MCM**7620**	70	Open-Collector	16	*ss*
512 × 4	MCM**7621**	70	Three-State	16	*ss*
512 × 4	MCM**7640**	70	Open-Collector	24	*ss*
512 × 4	MCM**7641**	70	Three-State	24	*ss*
1024 × 4	MCM**7642**	70	Open-Collector	18	*ss*
1024 × 4	MCM**7643**	70	Three-State	18	*ss*
1024 × 8	MCM**7680**	70	Open-Collector	24	*ss*
1024 × 8	MCM**7681**	70	Three-State	24	*ss*
2048 × 4	MCM**7684***	70	Open-Collector	18	*ss*
2048 × 4	MCM**7685***	70	Three-State	18	*ss*

*To be introduced.

See Notes on Page 1-2.

ROMs

Organization	Part Number	Access Time (ns max)	Number of Power Supplies	Number of Pins	Second Source
MOS STATIC ROMs					
Character Generators[2]					
128 × (7 × 5)	MCM6670	350	1	18	
128 × (7 × 5)	MCM6674	350	1	18	
128 × (9 × 7)	MCM66700	350	1	24	ss
128 × (9 × 7)	MCM66710	350	1	24	ss
128 × (9 × 7)	MCM66714	350	1	24	ss
128 × (9 × 7)	MCM66720	350	1	24	ss
128 × (9 × 7)	MCM66730	350	1	24	ss
128 × (9 × 7)	MCM66734	350	1	24	
128 × (9 × 7)	MCM66740	350	1	24	ss
128 × (9 × 7)	MCM66750	350	1	24	ss
128 × (9 × 7)	MCM66760	350	1	24	ss
128 × (9 × 7)	MCM66770	350	1	24	
128 × (9 × 7)	MCM66780	350	1	24	
128 × (9 × 7)	MCM66790	350	1	24	
Binary ROMs					
1024 × 8	MCM68A30-8	350	1	24	
1024 × 8	MCM68A**308-7**	350	1	24	
2048 × 8	MCM68A**316-91**	350	1	24	
1024 × 8	MCM68B30A	250	1	24	ss
1024 × 8	MCM68A30A	350	1	24	ss
1024 × 8	MCM68B**308**	250	1	24	ss
1024 × 8	MCM68A**308**	350	1	24	ss
2048 × 8	MCM68A**316E**	350	1	24	ss
2048 × 8	MCM68A**316A**	350	1	24	ss
4096 × 8	MCM68A**332**	350	1	24	ss
4096 × 8	MCM68A332-2*	350	1	24	
8192 × 8	MCM68A364*	350	1	24	ss
8192 × 8	MCM68A364-3*	350	1	24	
8192 × 8	MCM68B364-3*	250	1	24	
CMOS ROM					
256 × 4	MCM14524	1200	1	16	

*To be introduced.

See Notes on Page 1-2.

MEMORY SYSTEMS

For most purposes, memory systems are as unique and individualistic as is the variety of equipment in which they are used. There are, however, some computer systems — microcomputers and minicomputers — whose widespread acceptance results in the use of large numbers of memory systems of a specific architecture. Some of these have been identified, resulting in the standard, inventoried systems described below. Due to large-volume requirement and broad-based sales, these systems represent excellent values.

ADD-IN SYSTEMS FOR MICROCOMPUTERS

Application	Organization				
	32K × 8	16K × 9 Parity Option	16K × 8	8K × 9 Parity Option	8K × 8
For 6800 Systems					
Dynamic RAMs					
Standard			MMS68100		MMS68100-1
Non-Volatile		MMS68102A	MMS68102	MMS68102A1	MMS68102-1
for D2 Kit			MMS68104		
Pseudo-Static RAMs		MMS68103A	MMS68103	MMS68103A1	MMS68103-1
For 8080A Systems					
Dynamic RAMs	MMS80810		MMS80810-1		

ADD-IN SYSTEMS FOR MINICOMPUTERS

Application	Organization						
	64K × 18	48K × 18	32K × 18 32K × 16*	16K × 18 16K × 16*	12K × 18 12K × 16*	8K × 18 8K × 16*	4K × 16
For LSI-11/2/23 and PDP-11/03,/23			MMS1102-34PC MMS1102-34*	MMS1102-32PC MMS1102-32*		MMS1102-31PC MMS1102-31*	
LSI-11				MMS1110*	MMS1110-1*	MMS1110-2*	MMS1110-3*
For General Automation 16/110, 16/220			MMS1600-32* MMS1600-32P	MMS1600-16* MMS1600-16P			
For PDP-11/05/10/35/40/45/50/55/60 Access Time							
390 ns	MMS1117-58PC	MMS117-56PC	MMS1117-54PC	MMS1117-52PC			
360 ns	MMS1117-48PC	MMS117-46PC	MMS1117-44PC	MMS1117-42PC			
290 ns	MMS1117-38PC	MMS117-36PC	MMS1117-34PC	MMS1117-32PC			
For PDP-11/04 and 11/34				MMS1118	MMS1118-1	MMS1118-2	
For PDP-11s with "MF11L" Backplane				MMS1118L*	MMS1118L-1*	MMS1118L-2*	

MODULES FOR GENERAL-PURPOSE APPLICATIONS

Dynamic RAMs	
128K × 18 bits	MMS3418

THE OFFICIAL MOS MEMORY CROSS-REFERENCE

From Motorola

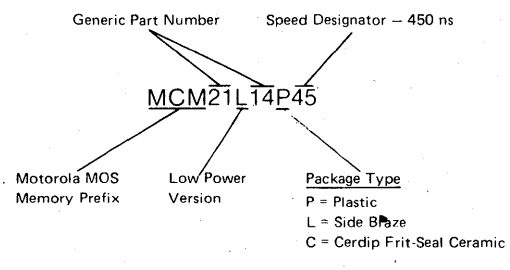
APRIL 1979

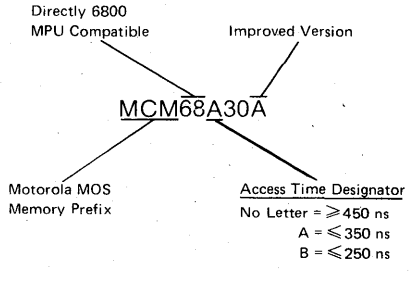
PART NUMBER	ORGANIZATION DESCRIPTION	MOTOROLA'S ACCESS TIME (ns max)	NO. OF PINS	POWER SUPPLIES	MOTOROLA PIN-TO-PIN REPLACEMENT
AMD					
Am2716	2048 X 8 EPROM	450	24	+5 V	MCM2716
Am4044	4096 X 1 SRAM	200-450	18	+5 V	MCM66L41
Am9016	16,384 X 1 DRAM	150-300	16	+12, ±5 V	MCM4116A
Am9114	1024 X 4 SRAM	200-450	18	+5 V	MCM2114
Am91L14	1024 X 4 SRAM	200-450	18	+5 V	MCM21L14
Am9124	1024 X 4 SRAM	200-450	18	+5 V	MCM2114
Am9147	4096 X 1 SRAM	55-85	18	+5 V	MCM2147
Am9208B	1024 X 8 SRAM	350	24	+5 V	MCM68A308
Am9217	2048 X 8 SROM	350	24	+5 V	MCM68A316A
Am9218	2048 X 8 SROM	350	24	+5 V	MCM68A316E
Am9232	4096 X 8 SROM	350	24	+5 V	MCM68A332
Am9708	1024 X 8 EPROM	450	24	+12, ±5 V	MCM68708
AMI					
S2114	1024 X 4 SRAM	200-450	18	+5 V	MCM2114
S2114L	1024 X 4 SRAM	200-450	18	+5 V	MCM21L14
S2147	4096 X 1 SRAM	70-100	18	+5 V	MCM2147
S4264	8192 X 8 SROM	350	24	+5 V	MCM68A364
S5101	256 X 4 SRAM	450-800	22	+5 V	MCM145101
S6508	1024 X 1 SRAM	300-460	16	+5 V	MCM146508
S6518	1024 X 1 SRAM	300-460	18	+5 V	MCM146518
S6810	128 X 8 SRAM	250-450	24	+5 V	MCM6810
S6830	1024 X 8 SROM	350	24	+5 V	MCM68A30A
S6831A	2048 X 8 SROM	350	24	+5 V	MCM68A316A
S6831B	2048 X 8 SROM	350	24	+5 V	MCM68A316E
FAIRCHILD					
F16K	16,384 X 1 DRAM	150-300	16	+12, ±5 V	MCM4116A
2114	1024 X 4 SRAM	200-450	18	+5 V	MCM2114
F2708	1024 X 8 EPROM	450	24	+12, ±5 V	MCM2708
F2708I	1024 X 8 EPROM	300	24	+12, ±5 V	MCM27A08
2716	2048 X 8 EPROM	450	24	+5 V	MCM2716
3508	1024 X 8 SROM	350	24	+5 V	MCM68A308
F3516E	2048 X 8 SROM	350	24	+5 V	MCM68A316E
FM4027	4096 X 1 DRAM	120-250	16	+12, ±5 V	MCM4027A
4096	4096 X 1 DRAM	250-350	16	+12, ±5 V	MCM4096
F68B10	128 X 8 SRAM	250-450	24	+5 V	MCM68B10
F68B308	1024 X 8 SROM	250-350	24	+5 V	MCM68B308
F68708	1024 X 8 EPROM	450	24	+12, ±5 V	MCM68708
FUJITSU					
MB2147	4096 X 1 SRAM	70-100	18	+5 V	MCM2147
MBM2716	2048 X 8 EPROM	450	24	+5 V	MCM2716
MB4044	4096 X 1 SRAM	200-450	18	+5 V	MCM6641
MB8114	1024 X 4 SRAM	200-450	18	+5 V	MCM2114
MB8116	16,384 X 1 DRAM	150-300	16	+12, ±5 V	MCM4116A
MB8224	4096 X 1 DRAM	250-350	16	+12, ±5 V	MCM4096
MB8227	4096 X 1 DRAM	120-250	16	+12, ±5 V	MCM4027A
MB8308	1024 X 8 SROM	350	24	+5 V	MCM68A308
MB8518H	1024 X 8 EPROM	450	24	+12, ±5 V	MCM2708
GENERAL INSTRUMENT					
RO3-8316A	2048 X 8 SROM	350	24	+5 V	MCM68A316A
RO3-9316	2048 X 8 SROM	350	24	+5 V	MCM68A316E
RO3-9332A	4096 X 8 SROM	350	24	+5 V	MCM68A332
RO3-9364B	8092 X 8 SROM	350	24	+5 V	MCM68A364
HITACHI					
HM462716	2048 X 8 EPROM	450	24	+5 V	MCM2716
HM435101	256 X 4 SRAM	450-800	22	+5 V	MCM145101
HM462708	1024 X 8 EPROM	450	24	+12, ±5 V	MCM2708
HM468A10	128 X 8 SRAM	350	24	+5 V	MCM68A10
HM46830	1024 X 8 SROM	350	24	+5 V	MCM68A30A
HM4704L	4096 X 1 DRAM	150-250	16	+12, ±5 V	MCM4027A
HM4716	16,384 X 1 DRAM	150-300	16	+12, ±5 V	MCM4116A
HM472114A	1024 X 4 SRAM	200-450	18	+5 V	MCM21L14
HM4847	4096 X 1 SRAM	55-85	18	+5 V	MCM2147

PART NUMBER	ORGANIZATION DESCRIPTION	MOTOROLA'S ACCESS TIME (ns max)	NO. OF PINS	POWER SUPPLIES	MOTOROLA PIN-TO-PIN REPLACEMENT
INTEL					
2104A	4096 X 1 DRAM	120-250	16	+12, ±5 V	MCM4027A
2114	1024 X 4 SRAM	200-450	18	+5 V	MCM2114
2114L	1024 X 4 SRAM	200-450	18	+5 V	MCM21L14
2117	16,384 X 1 DRAM	150-300	16	+12, ±5 V	MCM4116A
2147	4096 X 1 SRAM	70-100	18	+5 V	MCM2147
2308	1024 X 8 SROM	350	24	+5 V	MCM68A308
2316A	2048 X 8 SROM	350	24	+5 V	MCM68A316A
2316E	2048 X 8 SROM	350	24	+5 V	MCM68A316E
2708-1	1024 X 8 EPROM	300	24	+12, ±5 V	MCM27A08
2708	1024 X 8 EPROM	450	24	+12, ±5 V	MCM2708
2716	2048 X 8 EPROM	450	24	+5 V	MCM2716
2716-1	2048 X 8 EPROM	350	24	+5 V	MCM27A16
2716-2	2048 X 8 EPROM	350	24	+5 V	MCM27A16
5101	256 X 4 SRAM	450-800	22	+5 V	MCM145101
INTERSIL					
D2114	1024 X 4 SRAM	200-450	18	+5 V	MCM2114
MK4027	4096 X 1 DRAM	150-250	16	+12, ±5 V	MCM4027A
IM6508	1024 X 1 SRAM	300-460	16	+5 V	MCM146508
IM6508-1	1024 X 1 SRAM	300-460	18	+5 V	MCM146518
IM7027	4096 X 1 DRAM	120-250	16	+12, ±5 V	MCM4027A
IM7114	1024 X 4 SRAM	200-450	18	+5 V	MCM21L14
IM7116	16,384 X 1 DRAM	150-300	16	+12, ±5 V	MCM4116A
IM7141	4096 X 1 SRAM	200-450	18	+5 V	MCM6641
IM7141L	4096 X 1 SRAM	200-450	18	+5 V	MCM66L41
ITT					
ITT4027	4096 X 1 DRAM	120-250	16	+12, ±5 V	MCM4027A
ITT4116	16,384 X 1 DRAM	150-300	16	+12, ±5 V	MCM4116
MIC					
MIC2316E	2048 X 8 SROM	350	24	+5 V	MCM68A316E
MIC2332	4096 X 8 SROM	350	24	+5 V	MCM68A332
MOSTEK					
MK2708	1024 X 8 EPROM	450	24	+12, ±5 V	MCM2708
MK2716	2048 X 8 EPROM	450	24	+5 V	MCM2716
MK4027	4096 X 1 DRAM	120-250	16	+12, ±5 V	MCM4027A
MK4096	4096 X 1 DRAM	250-350	16	+12, ±5 V	MCM4096
MK4104	4096 X 1 DRAM	200-450	18	+5 V	MCM6641
MK4114	1024 X 4 SRAM	200-450	18	+5 V	MCM2114
MK4116	16,384 X 1 DRAM	150-300	16	+12, ±5 V	MCM4116A
MK30000	1024 X 8 SROM	350	24	+5 V	MCM68A308
MK31000	2048 X 8 SROM	350	24	+5 V	MCM68A316A
MK32000	4096 X 8 SROM	350	24	+5 V	MCM68A332
MK34000	2048 X 8 SROM	350	24	+5 V	MCM68A316E
MK36000	8192 X 8 SROM	350	24	+5 V	MCM68A364
MK36000-4	8192 X 8 SROM	250	24	+5 V	MCM68B364
NATIONAL					
MM2114	1024 X 4 SRAM	200-450	18	+5 V	MCM2114
MM2147	4096 X 1 SRAM	55-85	18	+5 V	MCM2147
MM2708	1024 X 8 EPROM	450	24	+12, ±5 V	MCM2708
MM2716	2048 X 8 EPROM	450	24	+5 V	MCM2716
MM5235	8192 X 8 SROM	350	24	+5 V	MCM68A364
MM5257	4096 X 1 SRAM	200-450	18	+5 V	MCM6641
MM5257L	4096 X 1 SRAM	200-450	18	+5 V	MCM66L41
MM5290	16,384 X 1 DRAM	150-300	16	+12, ±5 V	MCM4116A
NEC/EA					
μPD414A	4096 X 1 DRAM	150-250	16	+12, ±5 V	MCM4027A
μPD414	4096 X 1 DRAM	250-350	16	+12, ±5 V	MCM4096
μPD416	16,384 X 1 DRAM	150-300	16	+12, ±5 V	MCM4116A
μPD2114L	1024 X 4 SRAM	200-450	18	+5 V	MCM21L14
μPD2147	4096 X 1 SRAM	55-85	18	+5 V	MCM2147
μPD2716	2048 X 8 EPROM	450	24	+5 V	MCM2716
μPD4104	4096 X 1 SRAM	200-450	18	+5 V	MCM66L41
μPD5101	256 X 4 SRAM	450-800	22	+5 V	MCM145101
μPD6508	1024 X 1 SRAM	300-460	16	+5 V	MCM146508
EA2308/8308	1024 X 8 SROM	350	24	+5 V	MCM68A308
μPD or EA2316A/8316A	2048 X 8 SROM	350	24	+5 V	MCM68A316A
μPD or EA2316E/8316E	2048 X 8 SROM	350	24	+5 V	MCM68A316E
EA2708	1024 X 8 EPROM	450	24	+12, ±5 V	MCM2708
μPD or EA2716	2048 X 8 EPROM	450	24	+5 V	MCM2716

PART NUMBER	ORGANIZATION DESCRIPTION	MOTOROLA'S ACCESS TIME (ns max)	NO. OF PINS	POWER SUPPLIES	MOTOROLA PIN-TO-PIN REPLACEMENT
NITRON					
NC6570	128 X (9 X 7) SROM	350	24	+5 V	MCM66700
NC6571	128 X (9 X 7) SROM	350	24	+5 V	MCM66710
NC6572	128 X (9 X 7) SROM	350	24	+5 V	MCM66720
NC6573	128 X (9 X 7) SROM	350	24	+5 V	MCM66730
NC6574	128 X (9 X 7) SROM	350	24	+5 V	MCM66740
NC6575	128 X (9 X 7) SROM	350	24	+5 V	MCM66750
NC6832	2048 X 8 SROM	550	24	+12, ±5 V	MCM6832
SIGNETICS					
2607	1024 X 8 SROM	350	24	+5 V	MCM68A308
2608	1024 X 8 SROM	350	24	+5 V	MCM68A30A
2609	128 X (9 X 7) SROM	350	24	+5 V	MCM66700
2660	4096 X 1 DRAM	120-250	16	+12, ±5 V	MCM4027A
2614	1024 X 4 SRAM	200-450	18	+5 V	MCM21L14
2616	2048 X 8 SROM	350	24	+5 V	MCM68A316E
2633	4096 X 8 SROM	350	24	+5 V	MCM68A332
2664	8192 X 8 SROM	350	24	+5 V	MCM68A364
2690	16,384 X 1 DRAM	250-350	16	+12, ±5 V	MCM4116A
2708	1024 X 8 EPROM	450	24	+12, ±5 V	MCM2708
2716	2048 X 8 EPROM	450	24	+5 V	MCM2716
4027	4096 X 1 DRAM	150-250	16	+12, ±5 V	MCM4027A
5101	256 X 4 SRAM	450-800	22	+5 V	MCM145101
SYNERTEK					
SY2114	1024 X 4 SRAM	200-450	18	+5 V	MCM21L14
SY2147	4096 X 1 SRAM	55-85	18	+5 V	MCM2147
SY2316A	2048 X 8 SROM	350	24	+5 V	MCM68A316A
SY2316B	2048 X 8 SROM	350	24	+5 V	MCM68A316E
SY2716	2048 X 8 EPROM	450	24	+5 V	MCM2716
SY5101	256 X 4 SRAM	450-800	22	+5 V	MCM145101
TEXAS INSTRUMENTS					
TMS 2516	2048 X 8 EPROM	450	24	+5 V	MCM2716
TMS 2708	1024 X 8 EPROM	450	24	+12, ±5 V	MCM2708
TMS 2716	2048 X 8 EPROM	450	24	+12, ±5 V	TMS 2716
TMS 4027	4096 X 1 DRAM	120-250	16	+12, ±5 V	MCM4027A
TMS 4044	4096 X 1 SRAM	200-450	18	+5 V	MCM6641
TMS 4045	1024 X 4 SRAM	200-450	18	+5 V	MCM2114
TMS 4116	16,384 X 1 DRAM	150-300	16	+12, ±5 V	MCM4116A
TMS 4700	1024 X 8 SROM	350	24	+5 V	MCM68A308
TMS 4732	4096 X 8 SROM	350	24	+5 V	MCM68A332

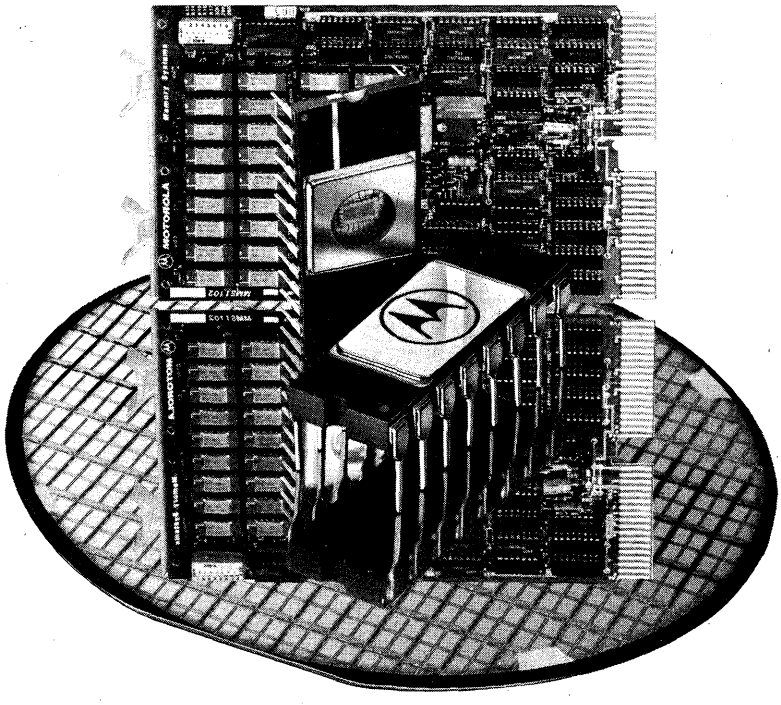
Part Number Guide





NMOS Memories
RAM, EPROM, ROM

2



MOTOROLA

MCM2114
MCM21L14

4096-BIT STATIC RANDOM ACCESS MEMORY

The MCM2114 is a 4096-bit random access memory fabricated with high density, high reliability N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, is directly compatible with TTL and DTL, and requires no clocks or refreshing because of fully static operation. Data access is particularly simple, since address setup times are not required. The output data has the same polarity as the input data.

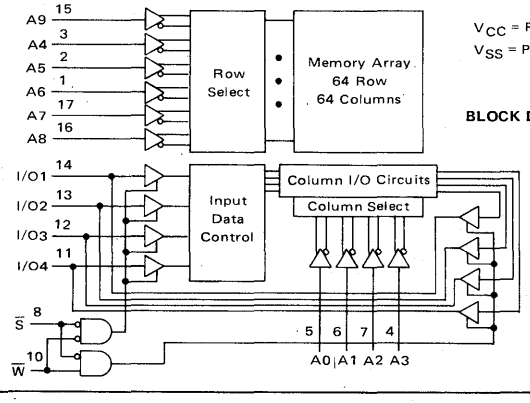
The MCM2114 is designed for memory applications where simple interfacing is the design objective. The MCM2114 is assembled in 18-pin dual-in-line packages with the industry standard pin-out. A separate chip select ($\overline{S}$) lead allows easy selection of an individual package when the three-state outputs are OR-tied.

The MCM2114 series has a maximum current of 100 mA. Low power versions (i.e., MCM21L14 series) are available with a maximum current of only 70 mA.

- 1024 Words by 4-Bit Organization
- Industry Standard 18-Pin Configuration
- Single +5 Volt Supply
- No Clock or Timing Strobe Required
- Fully Static: Cycle Time = Access Time
- Fully TTL/DTL Compatible
- Common Data Input and Output
- Three-State Outputs for OR-Ties
- Low Power Version Available

MAXIMUM ACCESS TIME/MINIMUM CYCLE TIME

MCM2114-20 MCM21L14-20	200 ns	MCM2114-30 MCM21L14-30	300 ns
MCM2114-25 MCM21L14-25	250 ns	MCM2114-45 MCM21L14-45	450 ns



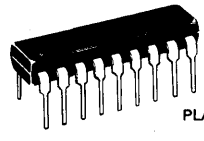
V_{CC} = Pin 18
V_{SS} = Pin 9

BLOCK DIAGRAM

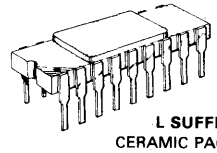
MOS

(N-CHANNEL, SILICON-GATE)

4096-BIT STATIC RANDOM ACCESS MEMORY

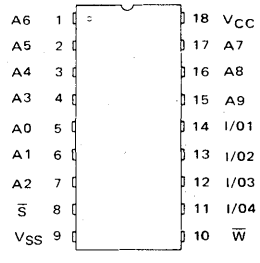


P SUFFIX
PLASTIC PACKAGE
CASE 707



L SUFFIX
CERAMIC PACKAGE
CASE 680

PIN ASSIGNMENT



PIN NAMES

A0-A9	Address Input
$\overline{W}$	Write Enable
$\overline{S}$	Chip Select
I/O1-I/O4	Data Input/Output
V_{CC}	Power (+5 V)
V_{SS}	Ground

2

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Value	Unit
Temperature Under Bias	-10 to +80	°C
Voltage on Any Pin With Respect to V_{SS}	-0.5 to +7.0	Vdc
DC Output Current	5.0	mA
Power Dissipation	1.0	Watt
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	-65 to +150	°C

Note: 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(T_A = 0° to 70°C, V_{CC} = 5.0V ±5%, unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	MCM2114			MCM21L14			Unit
		Min	Nom	Max	Min	Nom	Max	
Input Load Current (All Input Pins, V_{in} = 0 to 5.5 V)	I_{LI}	–	–	10	–	–	10	μA
I/O Leakage Current ($\overline{S}$ = 2.4 V, $V_{I/O}$ = 0.4 V to V_{CC})	$\|I_{LO}\|$	–	–	10	–	–	10	μA
Power Supply Current (V_{in} = 5.5, $I_{I/O}$ = 0 mA, T_A = 25°C)	I_{CC1}	–	80	95	–	–	65	mA
Power Supply Current (V_{in} = 5.5 V, $I_{I/O}$ = 0 mA, T_A = 0°C)	I_{CC2}	–	–	100	–	–	70	mA
Input Low Voltage	V_{IL}	-0.5	–	0.8	-0.5	–	0.8	V
Input High Voltage	V_{IH}	2.0	–	6.0	2.0	–	6.0	V
Output Low Current V_{OL} = 0.4 V	I_{OL}	2.1	6.0	–	2.1	6.0	–	mA
Output High Current V_{OH} = 2.4 V	I_{OH}	–	-1.4	-1.0	–	-1.4	-1.0	mA
Output Short Circuit Current	I_{OS} (2)	–	–	40	–	–	40	mA

Note: 2. *Duration not to exceed 30 seconds.*

CAPACITANCE

(f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	5.0	pF
Input/Output Capacitance ($V_{I/O}$ = 0 V)	$C_{I/O}$	5.0	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.)

Input Pulse Levels . . . . . 0.8 Volt to 2.4 Volts
Input Rise and Fall Times . . . . . 10 ns
Input and Output Timing Levels . . . . . 1.5 Volts
Output Load . . . . . 1 TTL Gate and C_L = 100 pF

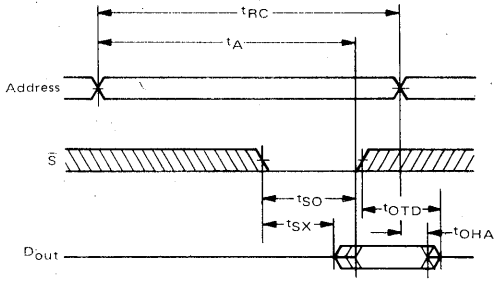
AC OPERATING CONDITIONS AND CHARACTERISTICS
Read (Note 3), Write (Note 4) Cycles

RECOMMENDED AC OPERATING CONDITIONS (T_A = 0 to 70°C, V_{CC} = 5.0 V ± 5%)

Parameter	Symbol	MCM2114-20 MCM21L14-20		MCM2114-25 MCM21L14-25		MCM2114-30 MCM21L14-30		MCM2114-45 MCM21L14-45		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	200	–	250	–	300	–	450	–	ns
Access Time	t_A	–	200	–	250	–	300	–	450	ns
Chip Selection to Output Valid	t_{SO}	–	70	–	85	–	100	–	120	ns
Chip Selection to Output Active	t_{SX}	20	–	20	–	20	–	20	–	ns
Output 3-State From Deselection	t_{OTD}	–	60	–	70	–	80	–	100	ns
Output Hold From Address Change	t_{OHA}	50	–	50	–	50	–	50	–	ns
Write Cycle Time	t_{WC}	200	–	250	–	300	–	450	–	ns
Write Time	t_W	120	–	135	–	150	–	200	–	ns
Write Release Time	t_{WR}	0	–	0	–	0	–	0	–	ns
Output 3-State From Write	t_{OTW}	–	60	–	70	–	80	–	100	ns
Data to Write Time Overlap	t_{DW}	120	–	135	–	150	–	200	–	ns
Data Hold From Write Time	t_{DH}	0	–	0	–	0	–	0	–	ns

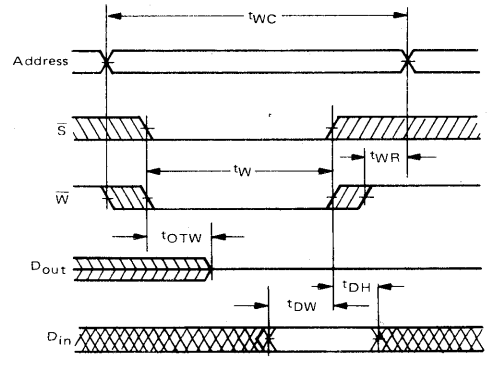
Notes: 3. A Read occurs during the overlap of a low $\overline{S}$ and a high $\overline{W}$.
4. A Write occurs during the overlap of a low $\overline{S}$ and a low $\overline{W}$.

READ CYCLE TIMING (Note 5)



Note: 5. $\overline{W}$ is high for a Read cycle.

WRITE CYCLE TIMING (Notes 6 and 7)



Notes: 6. If the $\overline{S}$ low transition occurs simultaneously with the $\overline{W}$ low transition, the output buffers remain in a high-impedance state.
7. $\overline{W}$ must be high during all address transitions.

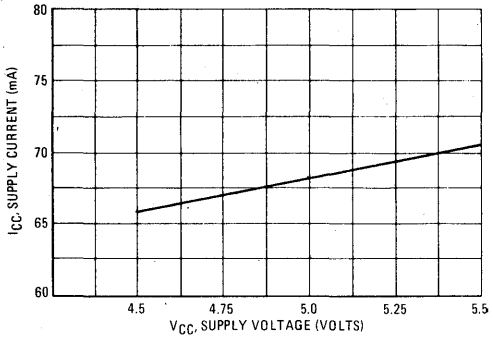
WAVEFORMS

Waveform Symbol	Input	Output
———	MUST BE VALID	WILL BE VALID
▨	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
▨	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
▨	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
———		HIGH IMPEDANCE

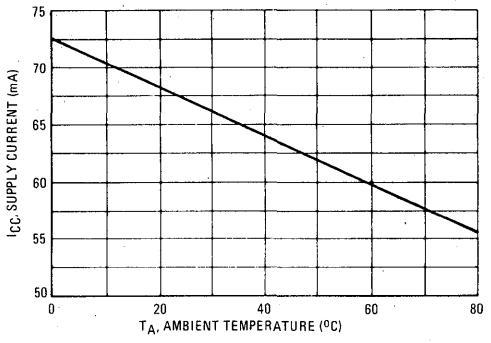
2

TYPICAL CHARACTERISTICS

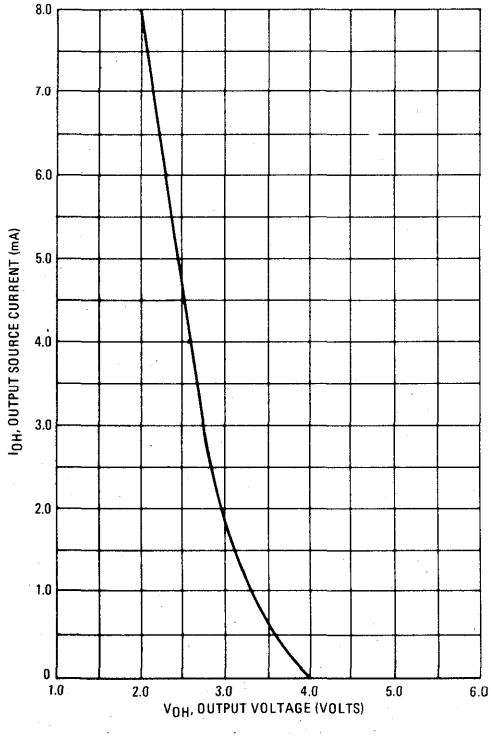
SUPPLY CURRENT versus SUPPLY VOLTAGE



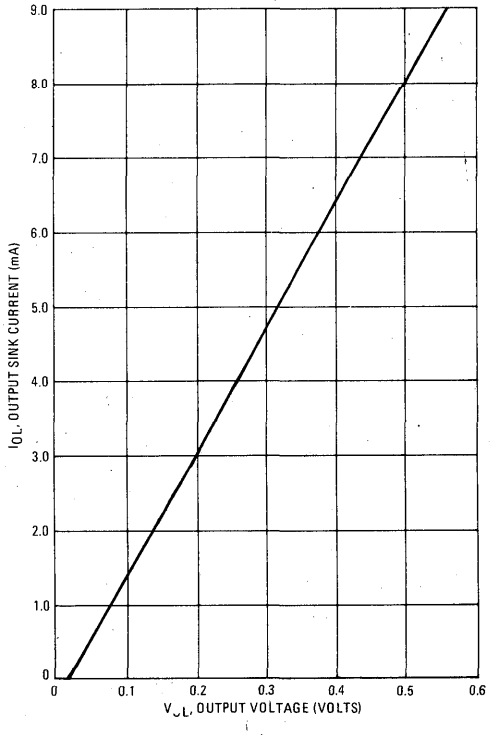
SUPPLY CURRENT versus AMBIENT TEMPERATURE



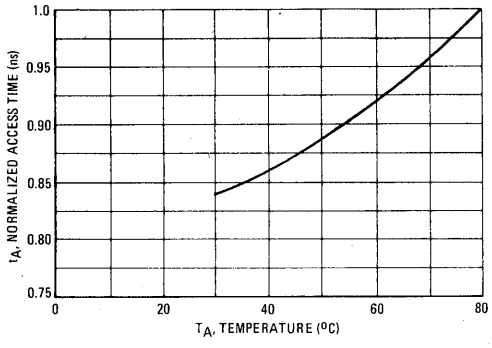
OUTPUT SOURCE CURRENT versus OUTPUT VOLTAGE



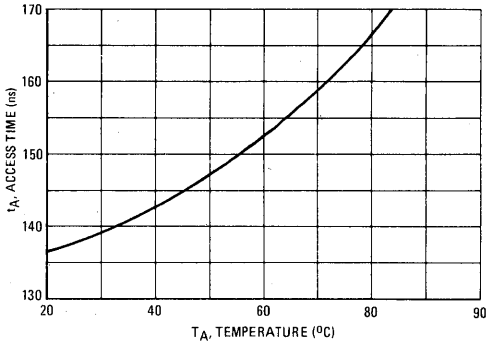
OUTPUT SINK CURRENT versus OUTPUT VOLTAGE



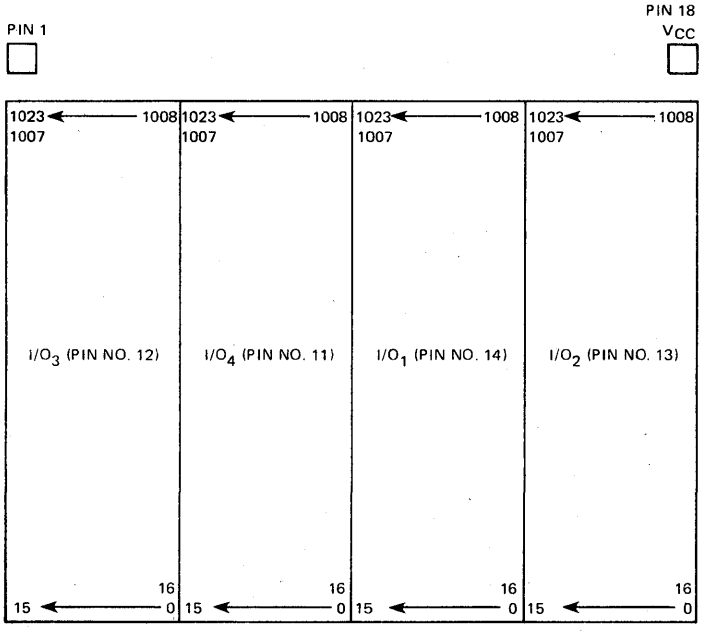
NORMALIZED ACCESS TIME versus TEMPERATURE



TYPICAL ACCESS TIME versus TEMPERATURE



MCM2114/MCM21L14 BIT MAP



To determine the precise location on the die of a word in memory, reassign address numbers to the address pins as in the table below. The bit locations can then be determined directly from the bit map.

PIN NUMBER	REASSIGNED ADDRESS NUMBER	PIN NUMBER	REASSIGNED ADDRESS NUMBER
1	A6	6	A1
2	A5	7	A2
3	A4	15	$\overline{A9}$
4	A3	16	$\overline{A8}$
5	A0	17	$\overline{A7}$

MOTOROLA

MCM2115A
MCM2125A

Product Preview

2

1024 X 1 STATIC RAM

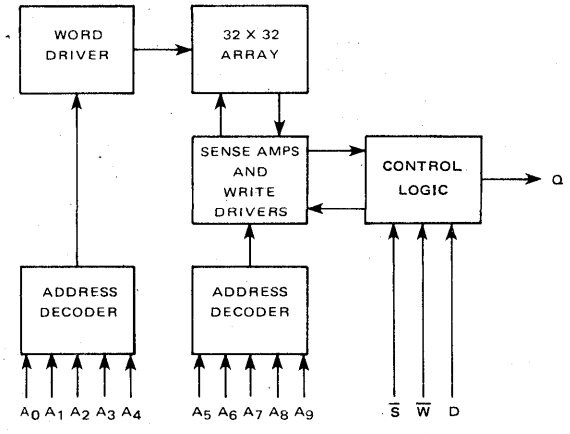
The MCM2115A and MCM2125A families are high-speed, 1024 words by one-bit random-access memories fabricated using HMOS, high-performance N-channel silicon-gate technology. Both open collector (MCM 2115A) and three-state output (MCM2125A) are available. The devices use fully static circuitry throughout and require no clocks or refreshing to operate. Data out has the same polarity as the input data.

Access times are fully compatible with the industry-produced 1K Bipolar RAMs, yet offer 20% to 50% reduction in power over their Bipolar equivalents.

All inputs and outputs are directly TTL compatible. A seperate chip select allows easy selection of an individual device when outputs are OR-tied.

- Organized as 1024 Words of 1 Bit
- Single +5 V Operation
- Maximum Access Time = 45 ns and 70 ns
- Low Operating Power Dissipation

BLOCK DIAGRAM



TRUTH TABLE

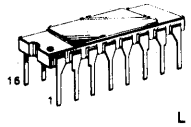
INPUTS			OUTPUT 2115A FAMILY	OUTPUT 2125A FAMILY	MODE
$\overline{S}$	$\overline{W}$	D	Q	Q	
H	X	X	H	Hi-Z	NOT SELECTED
L	L	L	H	Hi-Z	WRITE "0"
L	L	H	H	Hi-Z	WRITE "1"
L	H	X	Data Out	Data Out	READ

This is advance information and specifications are subject to change without notice.

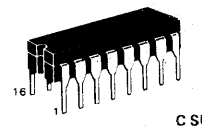
MOS

(N-CHANNEL, SILICON-GATE)

1024-BIT STATIC RANDOM ACCESS MEMORY

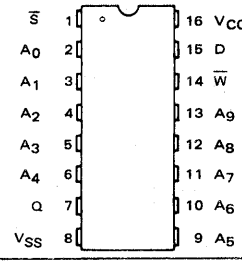


L SUFFIX
CERAMIC PACKAGE
CASE 690



C SUFFIX
FRIT SEAL
CERAMIC PACKAGE
CASE 620

PIN ASSIGNMENT



PIN NAMES	
A	Address
D	Data Input
Q	Data Output
$\overline{S}$	Chip Select
V_{CC}	+5 V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MOTOROLA

MCM2147

Advance Information

MOS
(N-CHANNEL, SILICON-GATE)

4096-BIT STATIC RANDOM ACCESS MEMORY

2

4096-BIT STATIC RANDOM ACCESS MEMORY

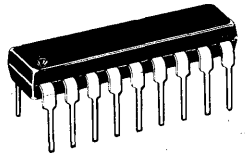
The MCM2147 is a 4096-bit static random access memory organized as 4096 words by 1-bit using Motorola's N-channel silicon-gate MOS technology. It uses a design approach which provides the simple timing features associated with fully static memories and the reduced standby power associated with semi-static and dynamic memories. This means low standby power without the need for clocks, nor reduced data rates due to cycle times that exceed access times.

$\overline{E}$ controls the power-down feature. It is not a clock but rather a chip select that affects power consumption. In less than a cycle time after $\overline{E}$ goes high, deselect mode, the part automatically reduces its power requirements and remains in this low-power standby mode as long as $\overline{E}$ remains high. This feature results in system power savings as great as 85% in larger systems, where most devices are deselected. The automatic power-down feature causes no performance degradation.

The MCM2147 is in an 18 pin dual in-line package with the industry standard pinout. It is TTL compatible in all respects. The data out has the same polarity as the input data. A data input and a separate three-state output provide flexibility and allow easy OR-ties.

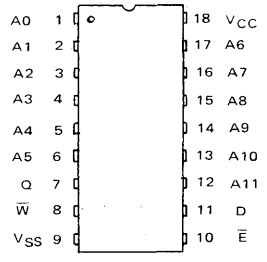
- Fully Static Memory — No Clock or Timing Strobe Required
- Single +5 V Supply
- High Density 18 Pin Package
- Automatic Power-Down
- Directly TTL Compatible—All Inputs and Outputs
- Separate Data Input and Output
- Three-State Output
- Access Time — MCM2147-55 = 55 ns max
  MCM2147-70 = 70 ns max
  MCM2147-85 = 85 ns max
  MCM2147-100 = 100 ns max

C SUFFIX
FRIT-SEAL
CERAMIC PACKAGE
also available

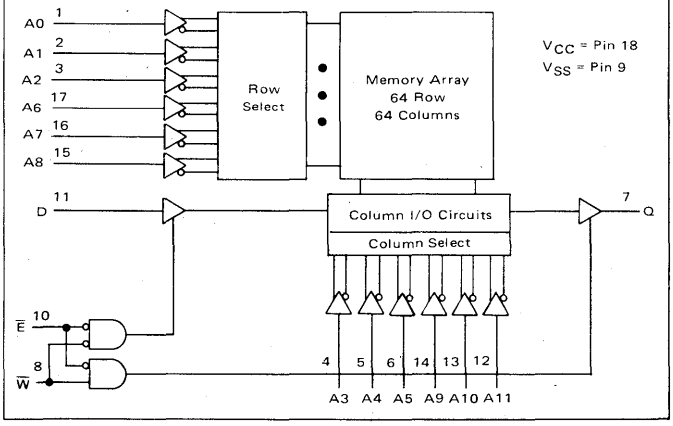


P SUFFIX
PLASTIC PACKAGE
CASE 707

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0-A11	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D	Data Input
Q	Data Output
V_{CC}	Power (+5 V)
V_{SS}	Ground

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	Output	Power
H	X	Not Selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	Data Out	Active

This is advance information and specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Value	Unit
Temperature Under Bias	-10 to +85	°C
Voltage on Any Pin With Respect to V_{CC}	-0.5 to +7.0	Vdc
DC Output Current	20	mA
Power Dissipation	1.0	Watt
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	-65 to +150	°C

Note: 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = 5.0 V ± 5% unless otherwise noted.)

Parameter	Symbol	MCM2147-55			MCM2147-70			MCM2147-85			MCM2147-100			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Load Current (All Input Pins, V_{in} = 0 to 5.5 V)	I_{IL}	–	0.01	10	–	0.01	10	–	0.01	10	–	0.01	10	μA
Output Leakage Current (E = 2.0 V, V_{out} = 0 to 5.5 V)	I_{OL}	–	0.1	50	–	0.1	50	–	0.1	50	–	0.1	50	μA
Power Supply Current (E = V_{IL}, Outputs Open, T_A = 25°C)	I_{CC1}	–	120	170	–	100	150	–	95	130	–	90	110	mA
Power Supply Current (E = V_{IL}, Outputs Open, T_A = 0°C)	I_{CC2}	–	–	180	–	–	160	–	–	140	–	–	120	mA
Standby Current (E = V_{IH})	I_{SB}	–	15	30	–	10	20	–	15	25	–	10	20	mA
Input Low Voltage	V_{IL}	-0.3	–	0.8	-0.3	–	0.8	-0.3	–	0.8	-0.3	–	0.8	V
Input High Voltage	V_{IH}	2.0	–	6.0	2.0	–	6.0	2.0	–	6.0	2.0	–	6.0	V
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	–	–	0.4	–	–	0.4	–	–	0.4	–	–	0.4	V
Output High Voltage (I_{OH} = -4.0 mA)	V_{OH}	2.4	–	–	2.4	–	–	2.4	–	–	2.4	–	–	V

Typical values are for T_A = 25°C and V_{CC} = +5.0 V.

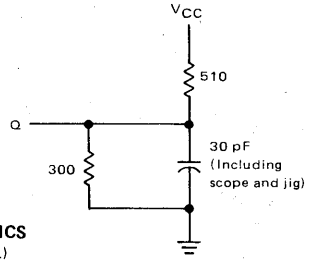
CAPACITANCE

(f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	5.0	pF
Output Capacitance (V_{out} = 0 V)	C_{out}	10	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I\Delta_t}{\Delta V}$.

FIGURE 1 – OUTPUT LOAD



AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.)

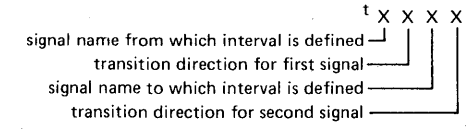
Input Pulse Levels. . . . . 0 Volt to 3.5 Volts
Input Rise and Fall Times . . . . . 10 ns
Input and Output Timing Levels . . . . . 1.5 Volts
Output Load. . . . . See Figure 1

AC OPERATING CONDITIONS AND CHARACTERISTICS, Read, Write Cycles (T_A = 0 to 70°C, V_{CC} = 5.0 V ± 5%)

Parameter	Symbol	MCM2147-55		MCM2147-70		MCM2147-85		MCM2147-100		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Address Valid to Address Don't Care (Cycle Time When Chip Enable is Held Active)	t_{AVAX}	55	–	70	–	85	–	100	–	ns
Chip Enable Low to Chip Enable High	t_{AVQV}	–	55	–	70	–	85	–	100	ns
Address Valid to Output Valid (Access)	t_{ELQV1}*	–	55	–	70	–	85	–	100	ns
Chip Enable Low to Output Valid (Access)	t_{ELQV2}*	–	65	–	80	–	95	–	110	ns
Address Valid to Output Invalid	t_{AVQX}	10	–	10	–	10	–	10	–	ns
Chip Enable Low to Output Invalid	t_{ELQX}	10	–	10	–	10	–	10	–	ns
Chip Enable High to Output High Z	t_{EHQZ}	0	40	0	40	0	40	0	40	ns
Chip Selection to Power-Up Time	t_{PU}	0	–	0	–	0	–	0	–	ns
Chip Deselection to Power-Down Time	t_{PD}	0	30	0	30	0	30	0	30	ns
Address Valid to Chip Enable Low (Address Setup)	t_{AXEL}	0	–	0	–	0	–	0	–	ns
Chip Enable Low to Write High	t_{ELWH}	45	–	55	–	70	–	80	–	ns
Address Valid to Write High	t_{AVWH}	45	–	55	–	70	–	80	–	ns
Address Valid to Write Low (Address Setup)	t_{AVWL}	0	–	0	–	0	–	0	–	ns
Write Low to Write High (Write Pulse Width)	t_{WLWH}	35	–	40	–	55	–	65	–	ns
Write High to Address Don't Care	t_{WHAX}	10	–	15	–	15	–	15	–	ns
Data Valid to Write High	t_{DVWH}	25	–	30	–	45	–	55	–	ns
Write High to Data Don't Care (Data Hold)	t_{WHDX}	10	–	10	–	10	–	10	–	ns
Write Low to Output High Z	t_{WLQZ}	0	30	0	35	0	45	0	50	ns
Write High to Output Valid	t_{WHQV}	0	–	0	–	0	–	0	–	ns

*t_{ELQV1} is access from chip enable when the 2147 is deselected for at least 55 ns prior to this cycle. t_{ELQV2} is access from chip enable for 0 ns < deselect time < 55 ns. If deselect time = 0 ns, then $t_{ELQV} = t_{AVQV}$.

TIMING PARAMETER ABBREVIATIONS



The transition definitions used in this data sheet are:

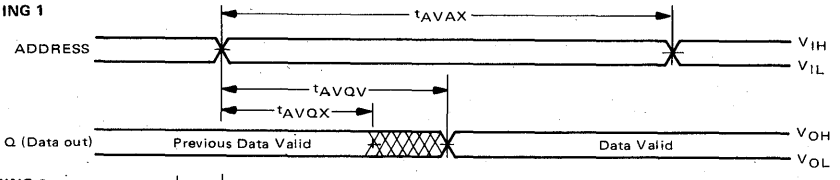
- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

TIMING LIMITS

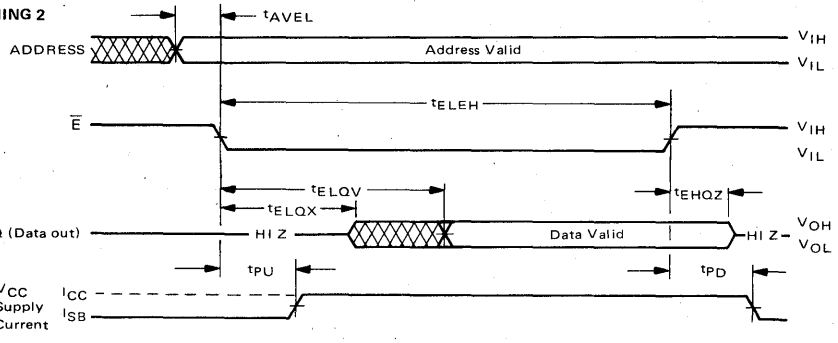
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

2

READ CYCLE TIMING 1
($\overline{E}$ Held Low)

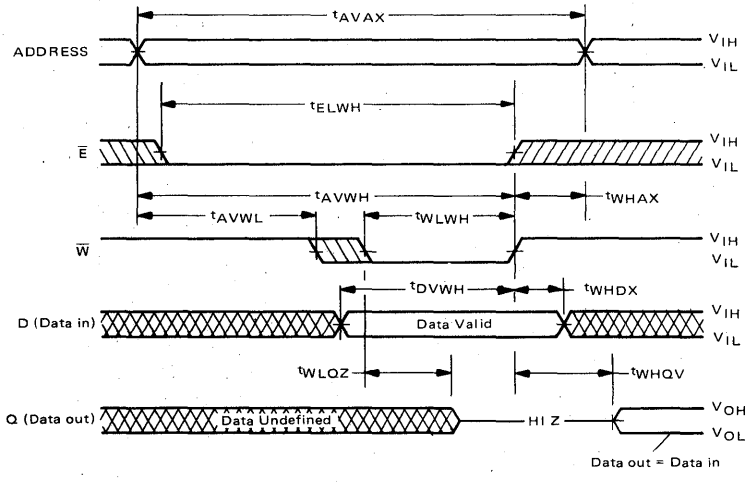


READ CYCLE TIMING 2



NOTE: $\overline{W}$ is high for Read Cycles.

WRITE CYCLE TIMING



WAVEFORMS

Waveform Symbol	Input	Output
———	MUST BE VALID	WILL BE VALID
▨	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
▨	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
▨	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
———	–	HIGH IMPEDANCE

DEVICE DESCRIPTION

The MCM2147 is produced with a high-performance MOS technology which combines on-chip substrate bias generation with device scaling to achieve high speed. The speed-power product of this process is about four times better than earlier MOS processes.

This gives the MCM2147 its high speed, low power and ease-of-use. The low-power standby feature is controlled with the $\overline{E}$ input. *$\overline{E}$ is not a clock and does not have to be cycled.* This allows the user to tie $\overline{E}$ directly to system addresses and use the line as part of the normal decoding logic. Whenever the MCM2147 is deselected, it automatically reduces its power requirements.

SYSTEM POWER SAVINGS

The automatic power-down feature adds up to significant system power savings. Unselected devices draw low standby power and only the active devices draw active power. Thus the average power consumed by a device declines as the system size increases, asymptotically approaching the standby power level as shown in Figure 2.

The automatic power-down feature is obtained without any performance degradation, since access time from chip enable is ⩽ access time from address valid. Also the fully static design gives access time equal cycle time so multiple read or write operations are possible during a single select period. The resultant data rates are 14.3 MHz and 18 MHz for the MCM2147-70 and MCM2147-55 respectively.

DECOUPLING AND BOARD LAYOUT CONSIDERATIONS

The power switching characteristic of the MCM2147 requires careful decoupling. It is recommended that a 0.1 μF to 0.3 μF ceramic capacitor be used on every other device, with a 22 μF to 47 μF bulk electrolytic decoupler every 16 devices. The actual values to be used will depend on board layout, trace widths and duty cycle.

Power supply gridding is recommended for PC board layout. A very satisfactory grid can be developed on a two-layer board with vertical traces on one side and horizontal traces on the other, as shown in Figure 3. If fast drivers are used, terminations are recommended on input signal lines to the MCM2147 because significant reflections are possible when driving their high impedance inputs. Terminations may be required to match the impedance of the line to the driver.

FIGURE 2 – AVERAGE DEVICE DISSIPATION versus MEMORY SIZE

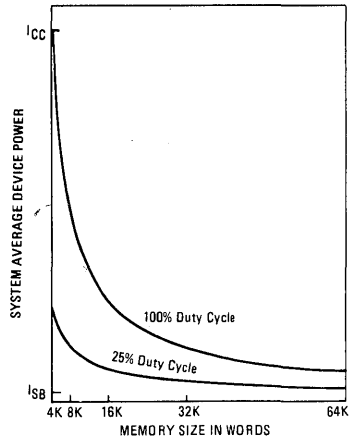
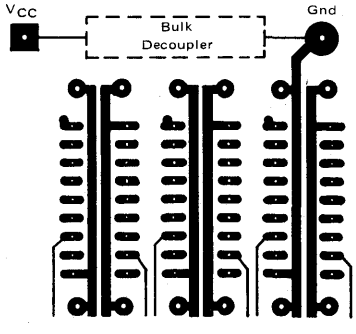


FIGURE 3 – PC LAYOUT



MOTOROLA

MCM4027A

4096-BIT DYNAMIC RANDOM ACCESS MEMORY

2

The MCM4027A is a 4096 x 1 bit high-speed dynamic Random Access Memory. It has smaller die size than the MCM4027 providing improved speed selections. The MCM4027A is fabricated using Motorola's highly reliable N-channel silicon-gate technology.

By multiplexing row and column address inputs, the MCM4027A requires only six address lines and permits packaging in Motorola's standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated.

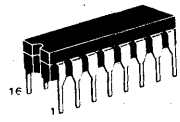
All inputs are TTL compatible, and the output is 3-state TTL compatible. The MCM4027A incorporates a one-transistor cell design and dynamic storage techniques, with each of the 64 row addresses requiring a refresh cycle every 2.0 milliseconds.

- Maximum Access Time = 120 ns – MCM4027AC1
  150 ns – MCM4027AC2
  200 ns – MCM4027AC3
  250 ns – MCM4027AC4
- Maximum Read and Write Cycle Time =
  320 ns – MCM4027AC1, C2
  375 ns – MCM4027AC3, C4
- Low Power Dissipation – 470 mW Max (Active)
  27 mW Max (Standby)
- 3-State Output for OR-Ties
- On-Chip Latches for Address, Chip Select, and Data In
- Power Supply Pins on Package Corners for Optimum Layout
- Industry Standard 16-Pin Package
- Page-Mode Capability
- Compatible with the Popular 2104/MK4096/MCM6604
- Second Source for MK4027

MOS

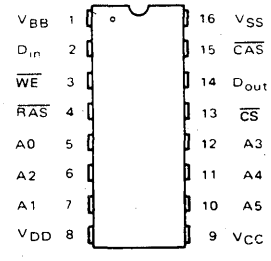
(N-CHANNEL, SILICON-GATE)

4096-BIT DYNAMIC RANDOM ACCESS MEMORY



C SUFFIX
FRIT-SEAL PACKAGE
CASE 620

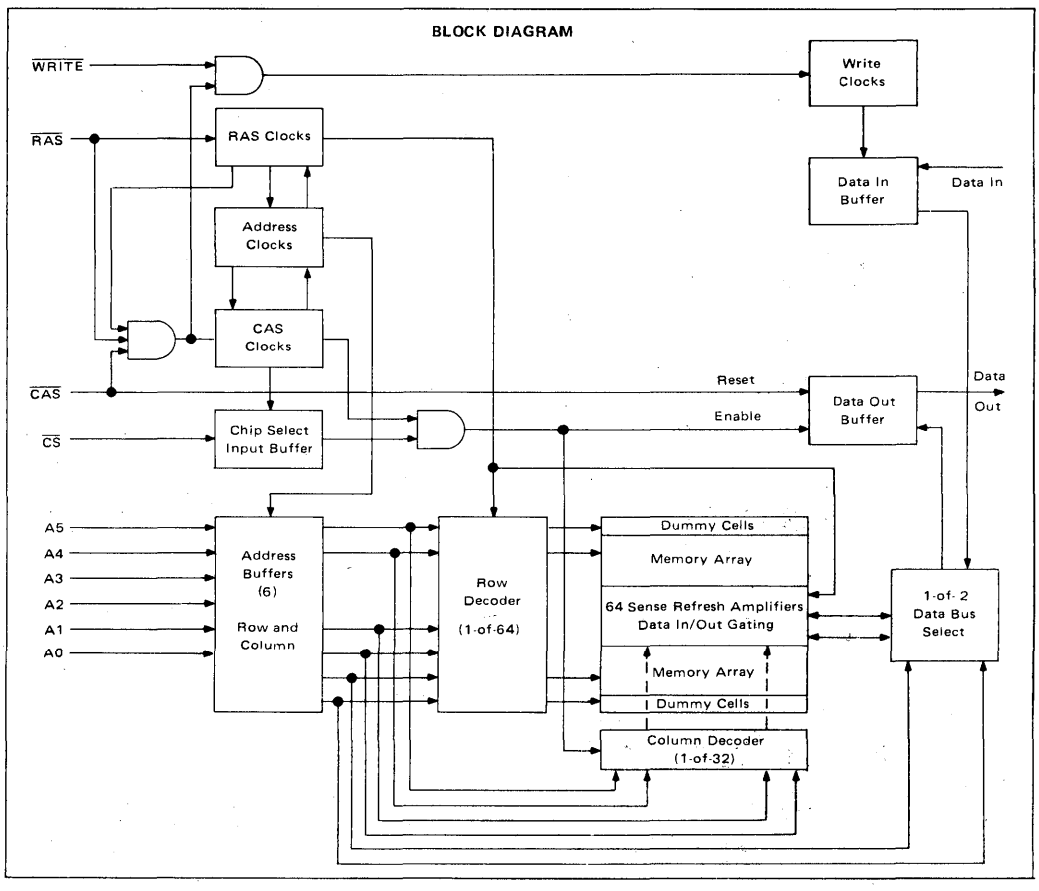
PIN ASSIGNMENT



TRUTH TABLE

Inputs				Data Out			Cycle Power	Ref	Function
RAS	CAS	CS	WE	Previous	Interim	Present			
L	L	L	L	Valid data	High Imp.	Input data	Full-operating	Yes	Write cycle
L	L	L	H	Valid data	High Imp.	Valid data (cell)	Full-operating	Yes	Read cycle
L	L	H	X	Valid data	High Imp.	High Imp.	Full-operating	Yes	Deselected-refresh
L	H	X	X	Valid data	Valid data	Valid data	Reduced operating	Yes	RAS only-refresh
H	L	X	X	Valid data	High Imp.	High Imp.	Standby	No	Standby-output disabled
H	H	X	X	Valid data	Valid data	Valid data	Standby	No	Standby-output valid

H = High, L = Low, X = Don't Care



OPERATING CHARACTERISTICS

ADDRESSING

The MCM4027A has six address inputs (A0–A5) and two clock signals designated Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). At the beginning of a memory cycle, the six low order address bits A0 through A5 are strobed into the chip with $\overline{RAS}$ to select one of the 64 rows. The row address strobe also initiates the timing that will enable the 64 column sense amplifiers. After a specified hold time, the row address is removed and the six high order address bits (A6–A11) are placed on the address pins. This address is then strobed into the chip with $\overline{CAS}$. Two of the 64 column sense amplifiers are selected by A1 through A5. A one of two data bus select is accomplished by A0 to complete the data selection. The Chip Select ($\overline{CS}$) is latched into the port along with the column addresses.

DATA OUTPUT

In order to simplify the memory system designed and reduce the total package count, the MCM4027A contains an input data latch and a buffered output data latch. The state of the output latch and buffer at the end of a memory cycle will depend on the type of memory cycle performed and whether the chip is selected or unselected for that memory cycle.

A chip will be unselected during a memory cycle if:

(1) The chip receives both $\overline{RAS}$ and $\overline{CAS}$ signals, but no $\overline{Chip\ Select}$ signal.

(2) The chip receives a $\overline{CAS}$ signal but no $\overline{RAS}$ signal. With this condition, the chip will be unselected regardless of the state of $\overline{Chip\ Select}$ input.

If, during a read, write, or read-modify-write cycle,

the chip is unselected, the output buffer will be in the high impedance state at the end of the memory cycle. The output buffer will remain in the high impedance state until the chip is selected for a memory cycle.

For a chip to be selected during a memory cycle, it must receive the following signals: $\overline{RAS}$, $\overline{CAS}$, and $\overline{Chip\ Select}$. The state of the output latch and buffer of a selected chip during the following type of memory cycles would be:

(1) Read Cycle – On the negative edge of $\overline{CAS}$, the output buffer will unconditionally go to a high impedance state. It will remain in this state until access time. At this time, the output latch and buffer will assume the logic state of the data read from the selected cell. This output state will be maintained until the chip receives the next $\overline{CAS}$ signal.

(2) Write Cycle – If the $\overline{WE}$ input is switched to a logic 0 before the $\overline{CAS}$ transition, the output latch and buffer will be switched to the state of the data input at the end of the access time. This logic state will be maintained until the chip receives the next $\overline{CAS}$ signal.

(3) Read-Modify-Write – Same as read cycle.

DATA INPUT

Data to be written into a selected storage cell of the memory chip is first stored in the on-chip data latch. The gating of this latch is performed with a combination of the $\overline{WE}$ and $\overline{CAS}$ signals. The last of these signals to make a negative transition will strobe the data into the latch. If the $\overline{WE}$ input is switching to a logic 0 in the beginning of a write cycle, the falling edge of $\overline{CAS}$ strobes the data into the latch. The data setup and hold times are then referenced to the negative edge of $\overline{CAS}$.

If a read-modify-write cycle is being performed, the $\overline{WE}$ input would not make its negative transistion until after the $\overline{CAS}$ signal was enabled. Thus, the data would not be strobed into the latch until the negative transistion of $\overline{WE}$. The data setup and hold times would now be referenced to the negative edge of the $\overline{WE}$ signal. The only other timing constraints for a write-type-cycle is that both the $\overline{CAS}$ and $\overline{WE}$ signals remain in the logic 0 state for a sufficient time to accomplish the permanent storage of the data into the selected cell.

INPUT/OUTPUT LEVELS

All of the inputs to the MCM4027A are TTL-compatible, featuring high impedance and low capacitance (5 to 7 pF). The three-state data output buffer is TTL-compatible and has sufficient current sink capability (3.2 mA) to drive two TTL loads. The output buffer also has a separate V_{CC} pin so that it can be powered from the same supply as the logic being employed.

REFRESH

In order to maintain valid data, each of the 64 internal rows of the MCM4027A must be refreshed once every 2 ms. Any cycle in which a $\overline{RAS}$ signal occurs accomplishes a refresh operation. Any read, write, or read-modify-write cycle will refresh an entire internally selected row. However, if a write or read-modify-write cycle is used to perform a refresh cycle the chip must be deselected to prevent writing data into the selected cell. The memory can also be refreshed by employing only the $\overline{RAS}$ cycle. This refresh mode will not shorten the refresh cycle time; however, the system standby power can be reduced by approximately 30%.

If the $\overline{RAS}$ only refresh cycles are employed for an extended length of time, the output buffer may eventually lose data and assume the high impedance state. Applying $\overline{CAS}$ to the chip will restore activity of the output buffer.

POWER DISSIPATION

Since the MCM4027A is a dynamic RAM, its power drain will be extremely small during the time the chip is unselected.

The power increases when the chip is selected and most of this increase is encountered on the address strobe edge. The circuitry of the MCM4027A is largely dynamic so power is not drawn during the whole time the strobe is active. Thus the dynamic power is a function of the operating frequency rather than the active duty cycle.

In a memory system, the $\overline{CAS}$ signal must be supplied to all the memory chips to ensure that the outputs of the unselected chips are switched to the high impedance state. Those chips that do not receive a $\overline{RAS}$ signal will not dissipate any power on the $\overline{CAS}$ edge except for that required to turn off the chip outputs. Thus, in order to ensure minimum system power, the $\overline{RAS}$ signal should be decoded so that only the chips to be selected receive a $\overline{RAS}$ signal. If the $\overline{RAS}$ signal is decoded, then the chip select input of all the chips can be set to a logic 0 state.

DC OPERATING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS} = Ground.)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{DD}	10.8	12.0	13.2	Vdc	2
	V_{CC}	V_{SS}	5.0	V_{DD}	Vdc	3
	V_{SS}	0	0	0	Vdc	2
	V_{BB}	-4.5	-5.0	-5.5	Vdc	2
Logic 1 Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.4	5.0	7.0	Vdc	2, 4
Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IH}	2.2	5.0	7.0	Vdc	2, 4
Logic 0 Voltage, all inputs	V_{IL}	-1.0	0	0.8	Vdc	2, 4

DC CHARACTERISTICS (V_{DD} = 12 V ±10%, V_{CC} = 5.0 V ±10%, V_{BB} = -5.0 V ±10%, V_{SS} = 0 V, T_A = 0 to 70°C.) Notes 1, 5

Characteristic	Symbol	Min	Typ	Max	Units	Notes
Average V_{DD} Power Supply Current	I_{DD1}			35	mA	6
V_{CC} Power Supply Current	I_{CC}				mA	7
Average V_{BB} Power Supply Current	I_{BB}			250	µA	
Standby V_{DD} Power Supply Current	I_{DD2}			2	mA	9
Average V_{DD} Power Supply Current during "$\overline{RAS}$ only" cycles	I_{DD3}			25	mA	6
Input Leakage Current (any input)	$I_{I(L)}$			10	µA	8
Output Leakage Current	$I_{O(L)}$			10	µA	9, 10
Output Logic 1 Voltage @ I_{out} = -5 mA	V_{OH}	2.4			Vdc	
Output Logic 0 Voltage @ I_{out} = 3.2 mA	V_{OL}			0.4	Vdc	

NOTES 1 through 11:

1. T_A is specified for operation at frequencies to $t_{RC} \geq t_{RC}(min)$. Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible provided that all ac parameters are met.
2. All voltages referenced to V_{SS}.
3. Output voltage will swing from V_{SS} to V_{CC} when enabled, with no output load. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the $V_{OH}(min)$ specification is not guaranteed in this mode.
4. Device speed is not guaranteed at input voltages greater than TTL levels (0 to 5 v).
5. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
6. Current is proportional to cycle rate. $I_{DD1}(max)$ is measured at the cycle rate specified by $t_{RC}(min)$.
7. I_{CC} depends on output loading. During readout of high level data V_{CC} is connected through a low impedance (135 Ω typ) to Data Out. At all other times I_{CC} consists of leakage currents only.
8. All device pins at 0 volts except V_{BB} which is at -5 volts and the pin under test which is at +10 volts.
9. Output is disabled (high-impedance) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1. Transient stabilization is required prior to measurement of this parameter.
10. $0 V \leq V_{Out} \leq +10 V$.
11. Effective capacitance is calculated from the equation:

$$C = \frac{\Delta Q}{\Delta V} \text{ with } \Delta V = 3 \text{ volts.}$$

EFFECTIVE CAPACITANCE (Full operating voltage and temperature range, periodically sampled rather than 100% tested) Note 11

Characteristic		Symbol	Max	Unit
Input Capacitance	(A0-A5), D_{in}, $\overline{CS}$	$C_{in(EFF)}$	5.0	pF
	$\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$		10.0	
Output Capacitance		$C_{out(EFF)}$	7.0	pF

ABSOLUTE MAXIMUM RATINGS (See Notes 1 and 2)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{BB}*	V_{in}, V_{out}	-0.5 to +20	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Output Current (Short Circuit)	I_{out}	50	mAdc

* (V_{SS} - V_{BB} > 4.5 V)

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS ARE EXCEEDED. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. V_{BB} must be applied prior to V_{CC} and V_{DD}. V_{BB} must also be the last power supply switched off.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

AC OPERATING CONDITIONS AND CHARACTERISTICS
(Read, Write, and Read-Modify-Write Cycles)

RECOMMENDED AC OPERATING CONDITIONS (V_{DD} = 12 V ± 10%, V_{CC} = 5.0 V ± 10%, V_{BB} = -5.0 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C.) Notes 1, 5, 12, 18

Parameter	Symbol	MCM4027AC1		MCM4027AC2		MCM4027AC3		MCM4027AC4		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	320		320		375		375		ns	13
Read Write Cycle Time	t_{RWC}	320		320		375		375		ns	13
Page Mode Cycle Time	t_{PC}	160		170		225		285		ns	13
Access Time From Row Address Strobe	t_{RAC}		120		150		200		250	ns	14, 16
Access Time From Column Address Strobe	t_{CAC}		80		100		135		165	ns	15, 16
Output Buffer and Turn-Off Delay	t_{OFF}		35		40		50		60	ns	
Row Address Strobe Precharge Time	t_{RP}	100		100		120		120		ns	
Row Address Strobe Pulse Width	t_{RAS}	120	10,000	150	10,000	200	10,000	250	10,000	ns	
Row Address Strobe Hold Time	t_{RSH}	80		100		135		165		ns	
Column Address Strobe Pulse Width	t_{CAS}	80		100		135		165		ns	
Column Address Strobe Hold Time	t_{CSH}	120		150		200		250		ns	
Row to Column Strobe Lead Time	t_{RCD}	15	40	20	50	25	65	35	85	ns	17
Row Address Setup Time	t_{ASR}	0		0		0		0		ns	
Row Address Hold Time	t_{RAH}	15		20		25		35		ns	
Column Address Setup Time	t_{ASC}	-5		-10		-10		-10		ns	
Column Address Hold Time	t_{CAH}	40		45		55		75		ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	80		95		120		160		ns	
Chip Select Setup Time	t_{CSC}	0		-10		-10		-10		ns	
Chip Select Hold Time	t_{CH}	40		45		55		75		ns	
Chip Select Hold Time Referenced to $\overline{RAS}$	t_{CHR}	80		95		120		160		ns	
Transition Time Rise and Fall	t_T	3	35	3	35	3	50	3	50	ns	18
Read Command Setup Time	t_{RCS}	0		0		0		0		ns	
Read Command Hold Time	t_{RCH}	0		0		0		0		ns	
Write Command Hold Time	t_{WCH}	40		45		55		75		ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	80		95		120		160		ns	
Write Command Pulse Width	t_{WP}	40		45		55		75		ns	
Write Command to Row Strobe Lead Time	t_{RWL}	50		50		70		85		ns	
Write Command to Column Strobe Lead Time	t_{CWL}	50		50		70		85		ns	
Data In Setup Time	t_{DS}	0		0		0		0		ns	19
Data In Hold Time	t_{DH}	40		45		55		75		ns	19
Data In Hold Time Referenced to $\overline{RAS}$	t_{DHR}	80		95		120		160		ns	
Column to Row Strobe Precharge Time	t_{CRP}	0		0		0		0		ns	
Column Precharge Time	t_{CP}	60		60		80		110		ns	
Refresh Period	t_{RFSH}		2		2		2		2	ms	
Write Command Setup Time	t_{WCS}	0		0		0		0		ns	
$\overline{CAS}$ to $\overline{WRITE}$ Delay	t_{CWD}	60		60		80		90		ns	20
$\overline{RAS}$ to $\overline{WRITE}$ Delay	t_{RWD}	100		110		145		175		ns	20
Data Out Hold Time	t_{DOH}	10		10		10		10		µs	

NOTES 12 through 20:

12. AC measurements assume t_T = 5 ns.

13. The specifications for t_{RC}(min) and t_{RWC}(min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.

14. Assumes that $t_{RCD} \leq t_{RCD}$(max).

15. Assumes that $t_{RCD} \geq t_{RCD}$ (max).

16. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.

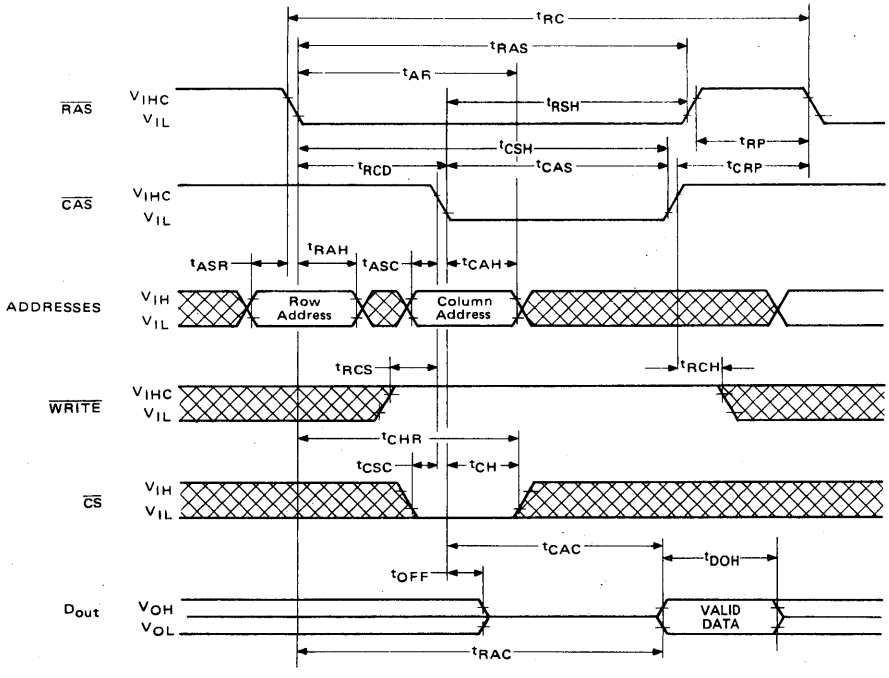
17. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

18. V_{IHC}(min) or V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

19. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify write cycles.

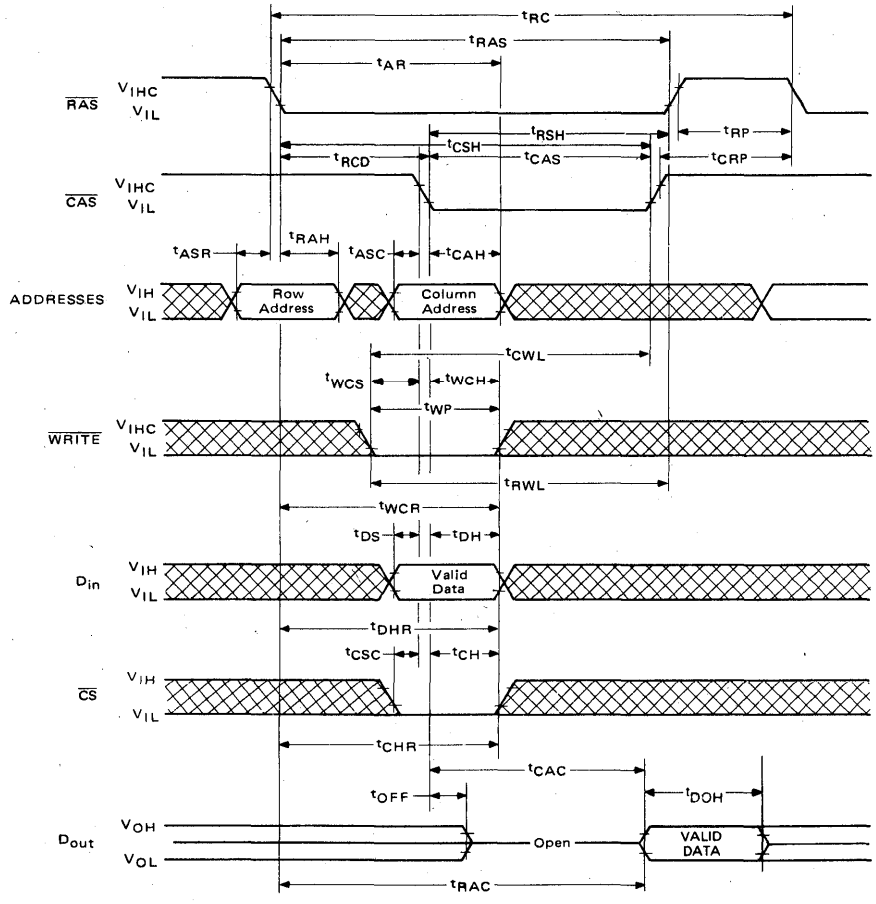
20. t_{WCS}, t_{CWD}, and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characterisitcs only: If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and Data Out will contain the data written into the selected cell. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min), the cycle is a read-write cycle and Data Out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of Data Out (at access time) is indeterminate.

READ CYCLE TIMING

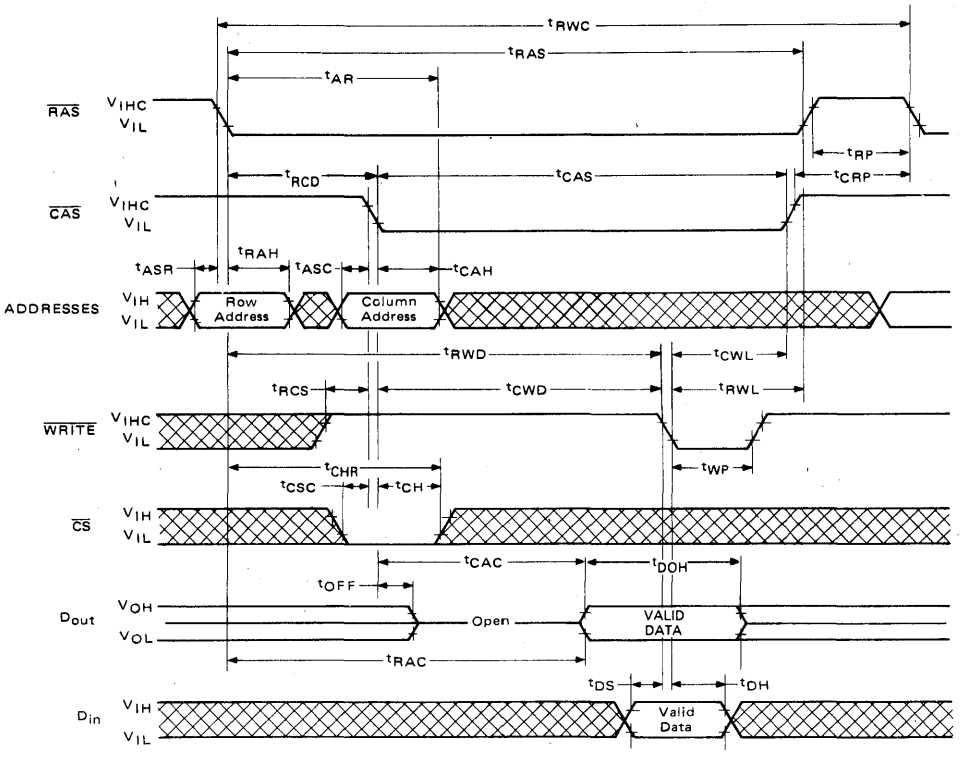


2

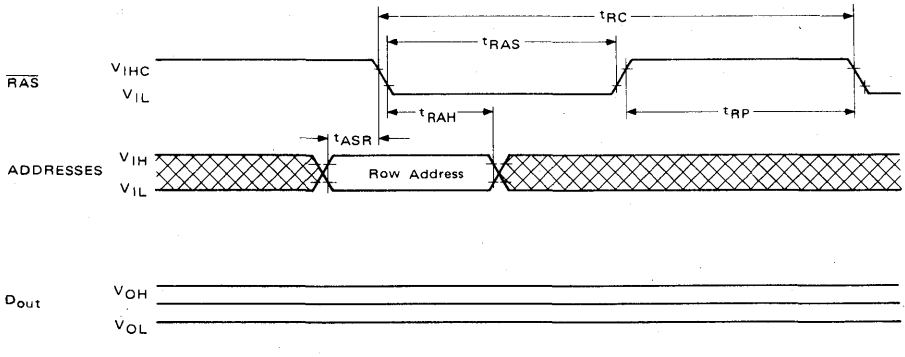
WRITE CYCLE TIMING



READ-MODIFY-WRITE TIMING

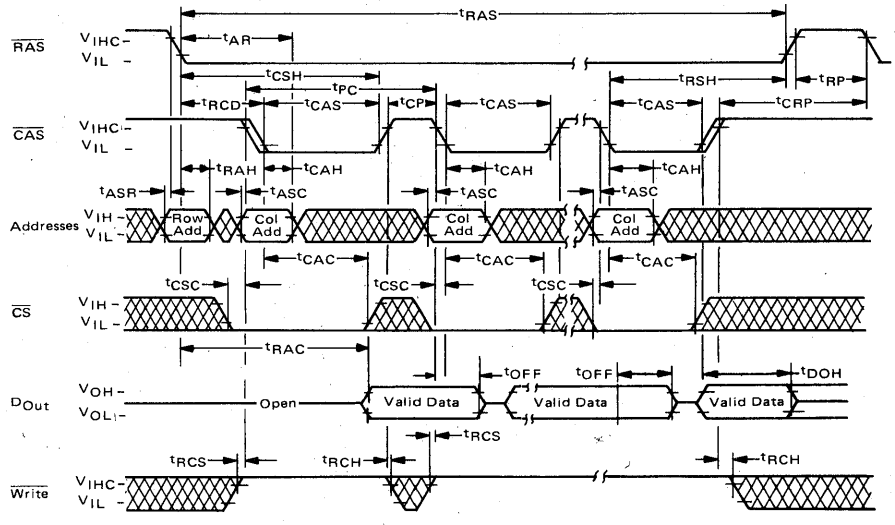


$\overline{\text{RAS}}$ ONLY REFRESH TIMING

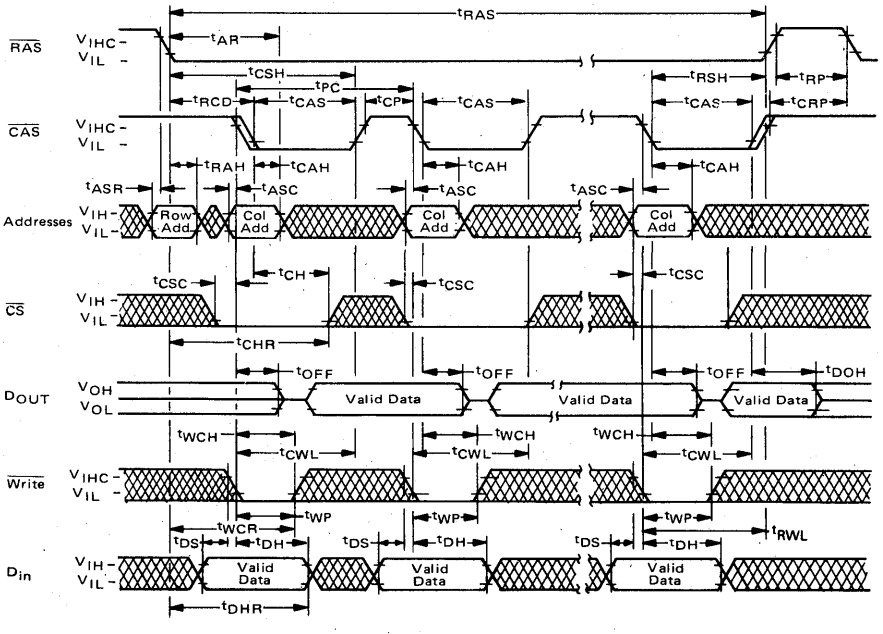


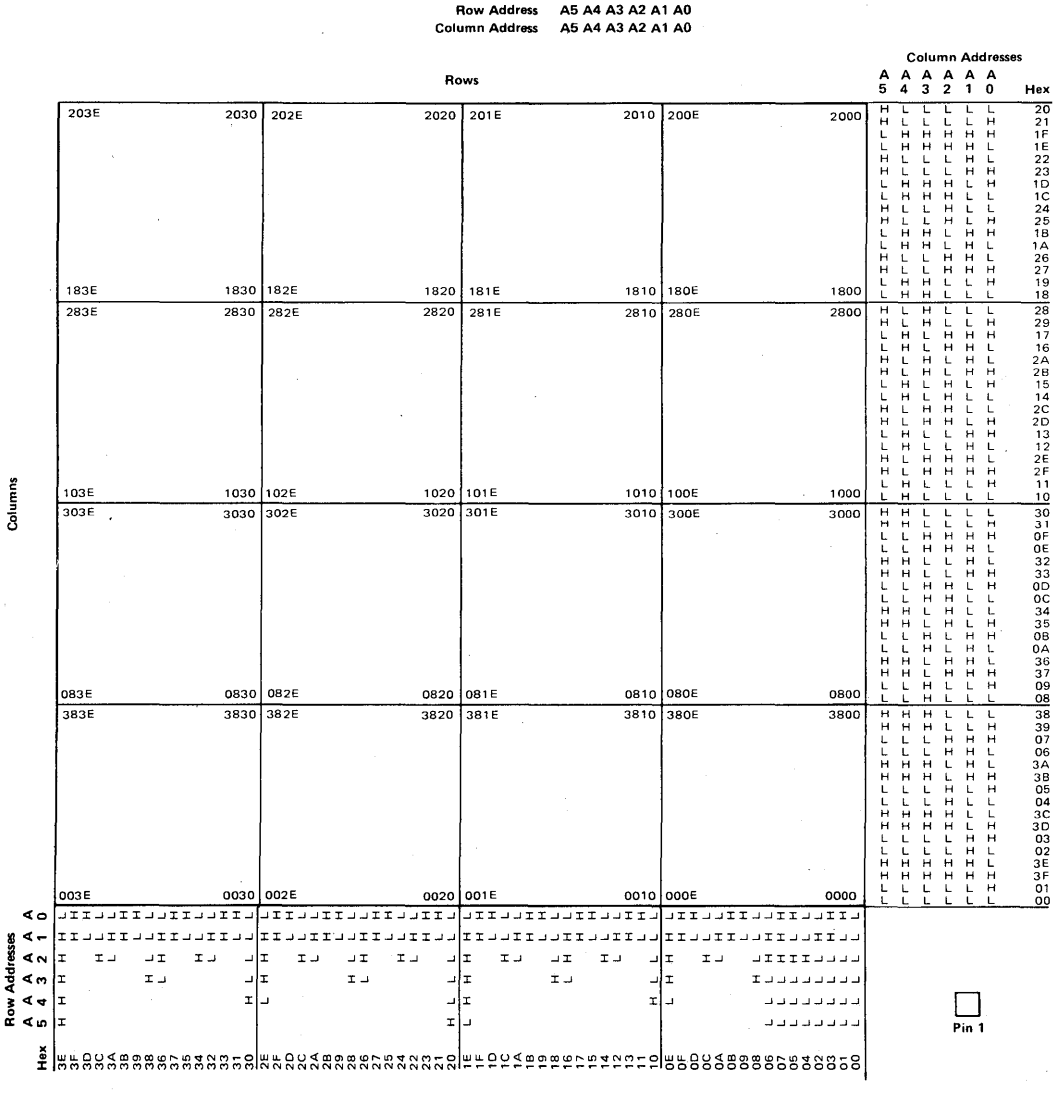
2

PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE





MCM4027A BIT ADDRESS MAP

MOTOROLA

MCM4096

Advance Information

MOS
(N-CHANNEL, SILICON-GATE)

4096-BIT DYNAMIC RANDOM ACCESS MEMORY

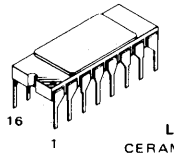
4096-BIT DYNAMIC RANDOM ACCESS MEMORY

The MCM4096 is a 4096-bit, high-speed dynamic Random Access Memory designed for high-performance, low-cost applications in mainframe and buffer memories and peripheral storage. Organized as 4096 one-bit words and fabricated using Motorola's highly reliable N-channel silicon gate technology, this device optimizes speed, power, and density tradeoffs.

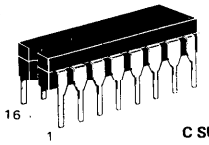
By multiplexing row and column address input, the MCM4096 requires only six address lines and permits packaging in Motorola's standard 16-pin dual in-line packages. Complete address decoding is done on chip with address latches incorporated.

All inputs are TTL compatible, and the output is 3-state TTL compatible. The MCM4096 incorporates a one-transistor cell design and dynamic storage techniques, with each of the 64 row addresses requiring a refresh cycle every 2.0 milliseconds.

- Organized as 4096 Words of 1 Bit
- Maximum Access Time = 250 ns – MCM4096L6, C6
  300 ns – MCM4096L16, C16
  350 ns – MCM4096L11, C11
- Minimum Read and Write Cycle Time =
  375 ns – MCM4096L6, C6
  425 ns – MCM4096L16, C16
  500 ns – MCM4906L11, C11
- Low Power Dissipation
  445 mW Maximum (Active)
  19 mW Maximum (Standby)
- 3-State Output
- On-Chip Latches for Address, Chip Select, and Data In
- Power Supply Pins on Package Corners for Optimum Layout
- Standard 16-Pin Package
- Compatible with the Popular 2104/MK4096/4027/MCM6604/ MCM6604A

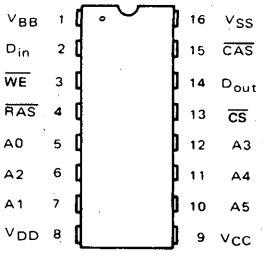


L SUFFIX
CERAMIC PACKAGE
CASE 690



C SUFFIX
FRIT-SEAL
CERAMIC PACKAGE
CASE 620

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{BB}*	V_{in}, V_{out}	-0.5 to +20	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Output Current (Short Circuit)	I_{out}	50	mAdc

*($V_{SS} - V_{DD} \geq 4.5$ V)

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. At power turn-on, the V_{BB} supply must come up before or coincident with V_{DD}.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

This is advance information and specifications are subject to change without notice.

DC OPERATING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS} = Ground)

Parameter	Symbol	4096-6		4096-16		4096-11		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Supply Voltage	V_{DD}	11.4	12.6	11.4	12.6	11.4	12.6	Vdc	1
	V_{CC}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	Vdc	1, 2
	V_{SS}	0	0	0	0	0	0	Vdc	1
	V_{BB}	-4.5	-5.5	-4.5	-5.5	-4.5	-5.5	Vdc	1
Logic 1 Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.7	7.0	2.7	7.0	3.0	7.0	Vdc	1, 3
Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IH}	2.4	7.0	2.4	7.0	2.4	7.0	Vdc	1, 3
Logic 0 Voltage, all inputs	V_{IL}	-1.0	0.8	-1.0	0.8	-1.0	0.8	Vdc	1, 3

DC CHARACTERISTICS (V_{DD} = 12 V ±10%, V_{CC} = 5.0 V ±10%, V_{BB} = -5.0 V ±10%, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic	Symbol	4096-6		4096-16		4096-11		Units	Notes
		Min	Max	Min	Max	Min	Max		
Average V_{DD} Power Supply Current	I_{DD1}	–	35	–	30	–	25	mA	4
V_{CC} Power Supply Current	I_{CC}	–	–	–	–	–	–	mA	5
Average V_{BB} Power Supply Curent	I_{BB}	–	75	–	75	–	75	µA	
Standby V_{DD} Power Supply Current	I_{DD2}	–	1.5	–	1.5	–	1.5	mA	7
Average V_{DD} Power Supply Current during "$\overline{RAS}$ only" cycles	I_{DD3}	–	25	–	22	–	18	mA	4
Input Leakage Current (any input)	$I_{IL(L)}$	–	5	–	5	–	5	µA	6
Output Leakage Current	$I_{O(L)}$	–	10	–	10	–	10	µA	7, 8
Output Logic 1 Voltage @ I_{out} = -5 mA	V_{OH}	2.4	–	2.4	–	2.4	–	Vdc	2
Output Logic 0 Votlage @ I_{out} = 3.2 mA	V_{OL}	–	0.4	–	0.4	–	0.4	Vdc	

NOTES:

1. All voltages referenced to V_{SS}. V_{BB} must be applied before and removed after other supply voltages.
2. Output voltage will swing from V_{SS} to V_{CC} if $V_{CC} \leq V_{DD}$ -4 volts. If $V_{CC} \geq V_{DD}$ -4 volts, the output will swing from V_{SS} to a voltage somewhat less than V_{DD}.
3. Device speed is not guaranteed at input voltages greater than TTL levels (0 to 5 V).
4. Current is proportional to cycle rate; maximum current is measured at the fastest cycle rate.
5. I_{CC} depends upon output loading. The V_{CC} supply is connected to the output buffer only.
6. All device pins at 0 volts except V_{BB} which is at -5 volts and the pin under test which is at +10 volts.
7. Output is disabled (open-circuit) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1.
8. $0 V \leq V_{out} \leq +10 V$.

EFFECTIVE CAPACITANCE (Full operating voltage and temperature range, periodically sampled rather than 100% tested.)

Characteristic		Symbol	Max	Unit
Input Capacitance	(A0-A5) D_{in}, $\overline{CS}$	$C_{in(EFF)}$	10	pF
	$\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$		7.0	
Output Capacitance		$C_{out(EFF)}$	8.0	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS
(Read, Write, and Read-Modify-Write Cycles)

2

RECOMMENDED AC OPERATING CONDITIONS (NOTES 13 and 15)

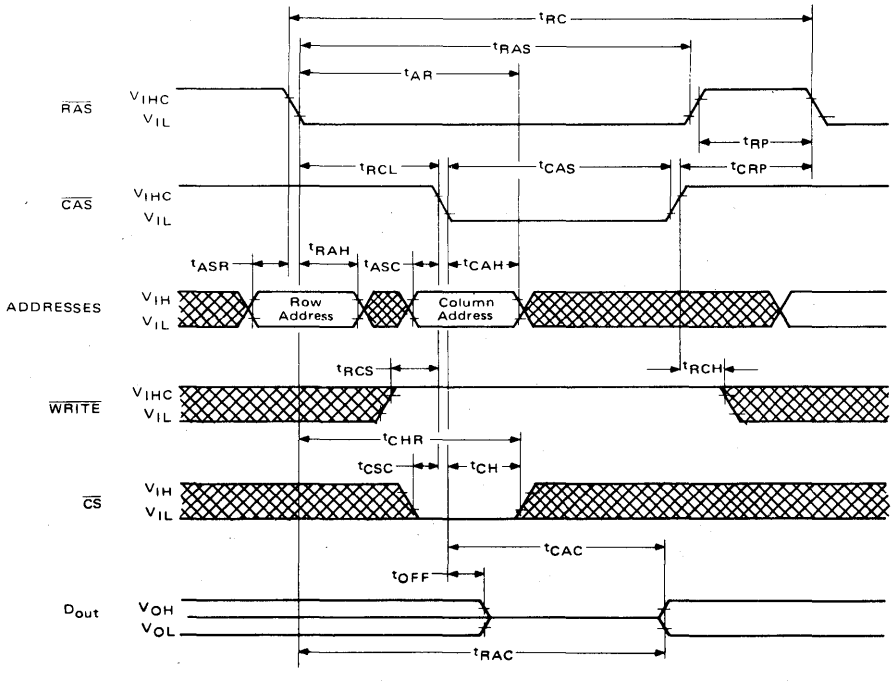
(V_{DD} = 12 V ±10%, V_{CC} = 5.0 V ±10%, V_{BB} = -5.0 V ±10%, V_{SS} = 0 V, T_A = 0 to 70°C)

Parameter	Symbol	MCM4096-6		MCM4096-16		MCM4096-11		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	375	–	425	–	500	–	ns	9
Access Time from Row Address Strobe	t_{RAC}	–	250	–	300	–	350	ns	9, 11
Access Time from Column Address Strobe	t_{CAC}	–	140	–	165	–	200	ns	10, 11
Output Buffer and Turn-Off Delay	t_{OFF}	0	65	0	80	0	100	ns	
Row Address Strobe Precharge Time	t_{RP}	115	–	125	–	150	–	ns	
Row Address Strobe Pulse Width	t_{RAS}	250	10,000	300	10,000	300	10,000	ns	
Column Address Strobe Pulse Width	t_{CAS}	140	–	165	–	200	–	ns	10
Row to Column Strobe Lead Time	t_{RCL}	60	110	80	135	100	150	ns	12
Row Address Setup Time	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	60	–	80	–	100	–	ns	
Chip Select Hold Time	t_{CH}	100	–	100	–	100	–	ns	
Transition Time (Rise and Fall)	t_T	3.0	50	3.0	50	3.0	50	ns	13
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	ns	
Write Command Hold Time	t_{WCH}	110	–	130	–	150	–	ns	
Write Command Pulse Width	t_{WP}	110	–	130	–	150	–	ns	
Column to Row Strobe Lead Time	t_{CRL}	-40	+40	-50	+50	-50	+50	ns	
Write Command to Column Strobe Lead Time	t_{CWL}	110	–	130	–	150	–	ns	
Data in Setup Time	t_{DS}	0	–	0	–	0	–	ns	14
Data in Hold Time	t_{DH}	110	–	130	–	150	–	ns	14
Refresh Period	t_{RFSH}	–	2.0	–	2.0	–	2.0	ms	
Modify Time	t_{Mod}	0	10	0	10	0	10	μs	
Data Out Hold Time	t_{DOH}	10	–	10	–	10	–	μs	

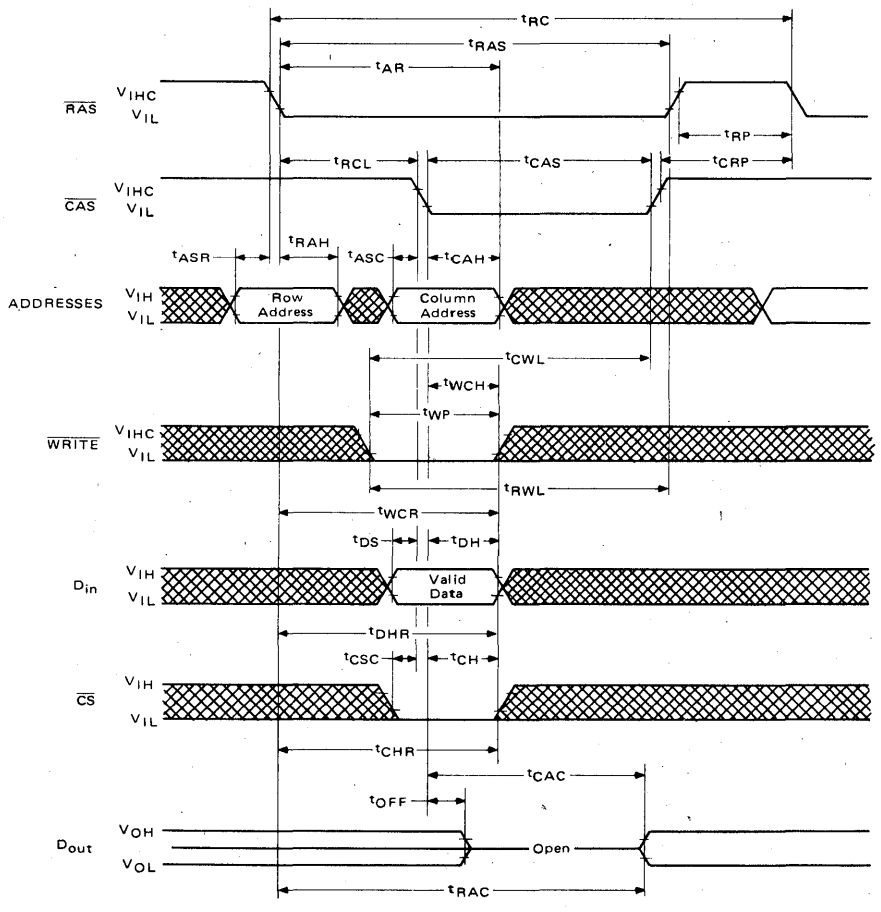
NOTES:

9. Assumes that $t_{RCL} + t_T \leq t_{RCL}$ (max).
10. Assumes that $t_{RCL} + t_T \geq t_{RCL}$ (max).
11. Measured with a load circuit equivalent to 1 TTL load and 100 pF.
12. Operation within the t_{RCL} (max) limit ensures that t_{RAC} (max) can be met. t_{RCL} (max) is specified as a reference point only; if t_{RCL} is greater than the specified t_{RCL} (max) limit, then access time is controlled exclusively by t_{CAC}.
13. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transistion times are measured between V_{IHC} or V_{IH} and V_{IL}.
14. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
15. After the application of supply voltages or after extended periods of operation without clocks, the device must perform a minimum of eight initialization cycles (any valid memory cycle containing both $\overline{RAS}$ and $\overline{CAS}$) prior to normal operation.

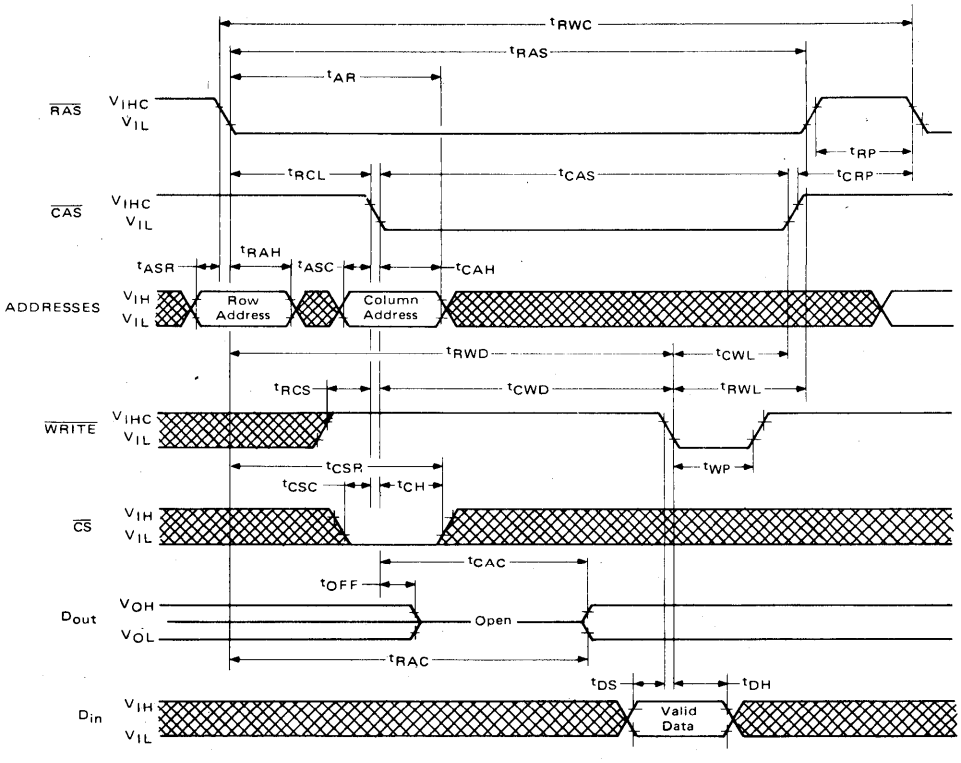
READ CYCLE TIMING



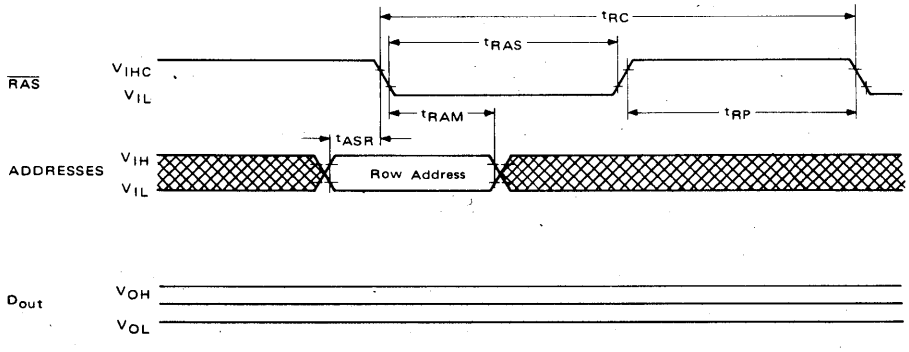
WRITE CYCLE TIMING

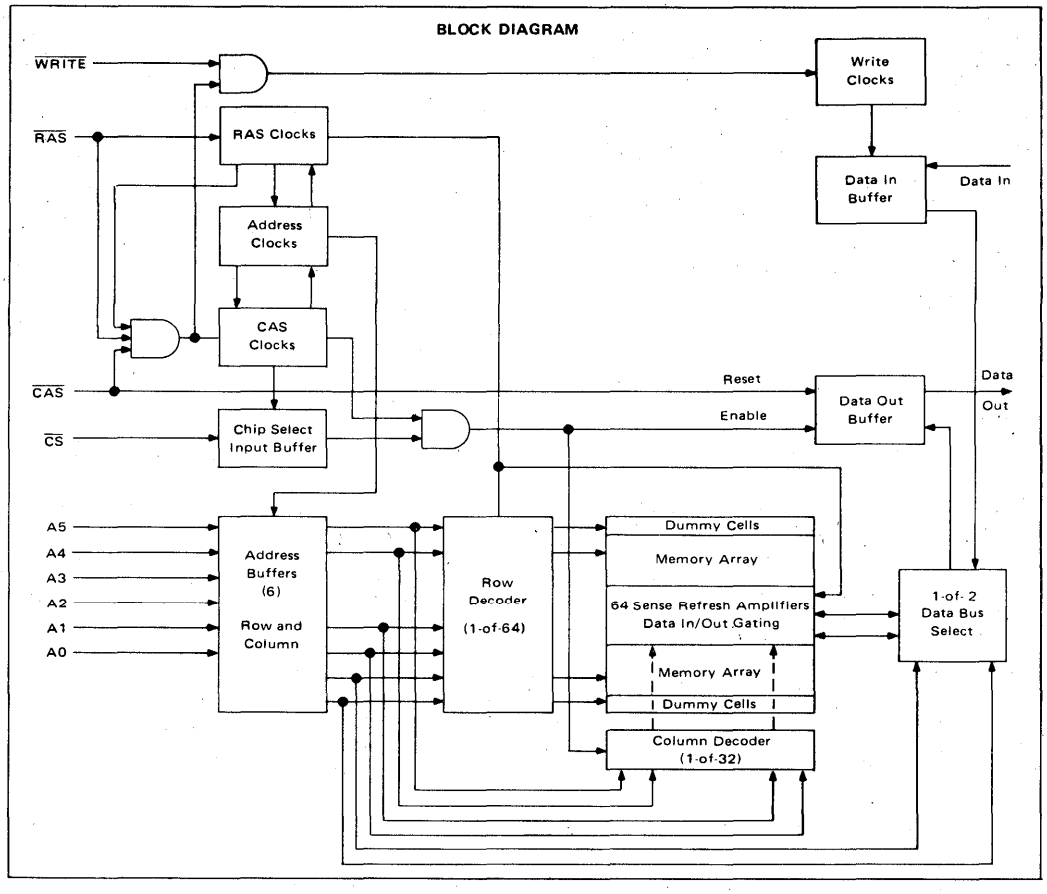


READ-MODIFY-WRITE TIMING



RAS ONLY REFRESH TIMING





OPERATING CHARACTERISTICS

ADDRESSING

The MCM4096 has six address inputs (A0–A5) and two clock signals designated Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). At the beginning of a memory cycle, the six low order address bits A0 through A5 are strobed into the chip with $\overline{RAS}$ to select one of the 64 rows. The row address strobe also initiates the timing that will enable the 64 column sense amplifiers. After a specified hold time, the row address is removed and the six high order address bits (A6–A11) are placed on the address pins. This address is then strobed into the chip with $\overline{CAS}$. Two of the 64 column sense amplifiers are selected by A1 through A5. A one of two data bus select is accomplished by A0 to complete the data selection. The Chip Select ($\overline{CS}$) is latched into the port along with the column addresses.

DATA OUTPUT

In order to simplify the memory system designed and reduce the total package count, the MCM4027 contains an input data latch and a buffered output data latch. The state of the output latch and buffer at the end of a memory cycle will depend on the type of memory cycle performed and whether the chip is selected or unselected for that memory cycle.

A chip will be unselected during a memory cycle if:

(1) The chip receives both $\overline{RAS}$ and $\overline{CAS}$ signals, but no $\overline{Chip\ Select}$ signal.

(2) The chip receives a $\overline{CAS}$ signal but no $\overline{RAS}$ signal. With this condition, the chip will be unselected regardless of the state of $\overline{Chip\ Select}$ input.

If, during a read, write, or read-modify-write cycle,

the chip is unselected, the output buffer will be in the high impedance state at the end of the memory cycle. The output buffer will remain in the high impedance state until the chip is selected for a memory cycle.

For a chip to be selected during a memory cycle, it must receive the following signals: $\overline{RAS}$, $\overline{CAS}$, and $\overline{Chip\ Select}$. The state of the output latch and buffer of a selected chip during the following type of memory cycles would be:

(1) Read Cycle – On the negative edge of $\overline{CAS}$, the output buffer will unconditionally go to a high impedance state. It will remain in this state until access time. At this time, the output latch and buffer will assume the logic state of the data read from the selected cell. This output state will be maintained until the chip receives the next $\overline{CAS}$ signal.

(2) Write Cycle – If the $\overline{WE}$ input is switched to a logic 0 before the $\overline{CAS}$ transition, the output latch and buffer will be switched to the state of the data input at the end of the access time. This logic state will be maintained until the chip receives the next $\overline{CAS}$ signal.

(3) Read-Modify-Write – Same as read cycle.

DATA INPUT

Data to be written into a selected storage cell of the memory chip is first stored in the on-chip data latch. The gating of this latch is performed with a combination of the $\overline{WE}$ and $\overline{CAS}$ signals. The last of these signals to make a negative transition will strobe the data into the latch. If the $\overline{WE}$ input is switching to a logic 0 in the beginning of a write cycle, the falling edge of $\overline{CAS}$ strobes the data into the latch. The data setup and hold times are then referenced to the negative edge of $\overline{CAS}$.

If a read-modify-write cycle is being performed, the $\overline{WE}$ input would not make its negative transistion until after the $\overline{CAS}$ signal was enabled. Thus, the data would not be strobed into the latch until the negative transistion of $\overline{WE}$. The data setup and hold times would now be referenced to the negative edge of the $\overline{WE}$ signal. The only other timing constraints for a write-type-cycle is that both the $\overline{CAS}$ and $\overline{WE}$ signals remain in the logic 0 state for a sufficient time to accomplish the permanent storage of the data into the selected cell.

INPUT/OUTPUT LEVELS

All of the inputs to the MCM4096 are TTL-compatible, featuring high impedance and low capacitance (5 to 7 pF). The three-state data output buffer is TTL-compatible and has sufficient current sink capability (3.2 mA) to drive two TTL loads. The output buffer also has a separate V_{CC} pin so that it can be powered from the same supply as the logic being employed.

REFRESH

In order to maintain valid data, each of the 64 internal rows of the MCM4096 must be refreshed once every 2 ms. Any cycle in which a $\overline{RAS}$ signal occurs accomplishes a refresh operation. Any read, write, or read-modify-write cycle will refresh an entire internally selected row. However, if a write or read-modify-write cycle is used to perform a refresh cycle the chip must be deselected to prevent writing data into the selected cell. The memory can also be refreshed by employing only the $\overline{RAS}$ cycle. This refresh mode will not shorten the refresh cycle time, however the system standby power can be reduced by approximately 30%.

If the $\overline{RAS}$ only refresh cycles are employed for an extended length of time, the output buffer may eventually *lose data and assume the high impedance state. Applying* $\overline{CAS}$ to the chip will restore activity of the output buffer.

POWER DISSIPATION

Since the MCM4096 is a dynamic RAM, its power drain will be extremely small during the time the chip is unselected.

The power increases when the chip is selected and most of this increase is encountered on the address strobe edge. The circuitry of the MCM4027 is largely dynamic so power is not drawn during the whole time the strobe is active. Thus the dynamic power is a function of the operating frequency rather than the active duty cycle.

In a memory system, the $\overline{CAS}$ signal must be supplied to all the memory chips to ensure that the outputs of the unselected chips are switched to the high impedance state. Those chips that do not receive a $\overline{RAS}$ signal will not dissipate any power on the $\overline{CAS}$ edge except for that required to turn off the chip outputs. Thus, in order to ensure minimum system power, the $\overline{RAS}$ signal should be decoded so that only the chips to be selected receive a $\overline{RAS}$ signal. If the $\overline{RAS}$ signal is decoded, then the chip select input of all the chips can be set to a logic 0 state.

MOTOROLA

MCM4116A

16,384-BIT DYNAMIC RANDOM ACCESS MEMORY

The MCM4116A is a 16,384-bit, high-speed dynamic Random Access Memory designed for high-performance, low-cost applications in mainframe and buffer memories and peripheral storage. Organized as 16,384 one-bit words and fabricated using Motorola's highly reliable N-channel double-polysilicon technology, this device optimizes speed, power, and density tradeoffs.

By muliplexing row and column address inputs, the MCM4116A requires only seven address lines and permits packaging in Motorola's standard 16-pin dual in-line packages. This packaging technique allows high system density and is compatible with widely available automated test and insertion equipment. Complete address decoding is done on chip with address latches incorporated.

All inputs are TTL compatible, and the output is 3-state TTL compatible. The data output of the MCM4116A is controlled by the column address strobe and remains valid from access time until the column address strobe returns to the high state. This output scheme allows higher degrees of system design flexibility such as common input/output operation and two dimensional memory selection by decoding both row address and column address strobes.

The MCM4116A incorporates a one-transistor cell design and dynamic storage techniques, with each of the 128 row addresses *requiring a refresh cycle every 2 milliseconds.*

- Flexible Timing with Read-Modify-Write, RAS-Only Refresh, and Page-Mode Capability
- Industry Standard 16-Pin Package
- 16,384 X 1 Organization
- ±10% Tolerance on All Power Supplies
- All Inputs are Fully TTL Compatible
- Three-State Fully TTL-Compatible Output
- Common I/O Capability When Using "Early Write" Mode
- On-Chip Latches for Addresses and Data In
- Low Power Dissipation – 462 mW Active, 20 mW Standby (Max)
- Fast Access Time Options: 150 ns – MCM4116AL-15, AC-15
  200 ns – MCM4116AL-20, AC-20
  250 ns – MCM4116AL-25, AC-25
  300 ns – MCM4116AL-30, AC-30
- Easy Upgrade from 16-Pin 4K RAMs
- Pin Compatible with 2117, 2116, 6616, μPD416, and 4116

ABSOLUTE MAXIMUM RATINGS (See Note 1)

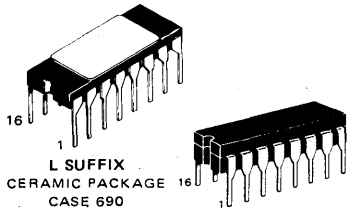
Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{BB}	V_{in},V_{out}	-0.5 to +20	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.0	W
Data Out Current	I_{out}	50	mA

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

MOS

(N-CHANNEL)

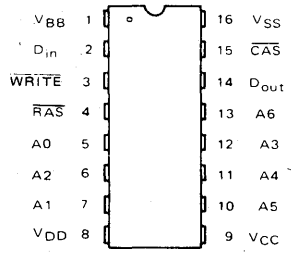
16,384-BIT DYNAMIC RANDOM ACCESS MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 690

C SUFFIX
FRIT-SEAL PACKAGE
CASE 620

PIN ASSIGNMENT



PIN NAMES

A0–A6	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{in}	Data In
D_{out}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{BB}	Power (-5 V)
V_{CC}	Power (+5 V)
V_{DD}	Power (+12 V)
V_{SS}	Ground

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{DD}	10.8	12.0	13.2	Vdc	1
	V_{CC}	4.5	5.0	5.5	Vdc	1, 2
	V_{SS}	0	0	0	Vdc	1
	V_{BB}	-4.5	-5.0	-5.5	Vdc	1
Logic 1 Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.7	–	7.0	Vdc	1
Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IH}	2.4	–	7.0	Vdc	1
Logic 0 Voltage, all inputs	V_{IL}	-1.0	–	0.8	Vdc	1

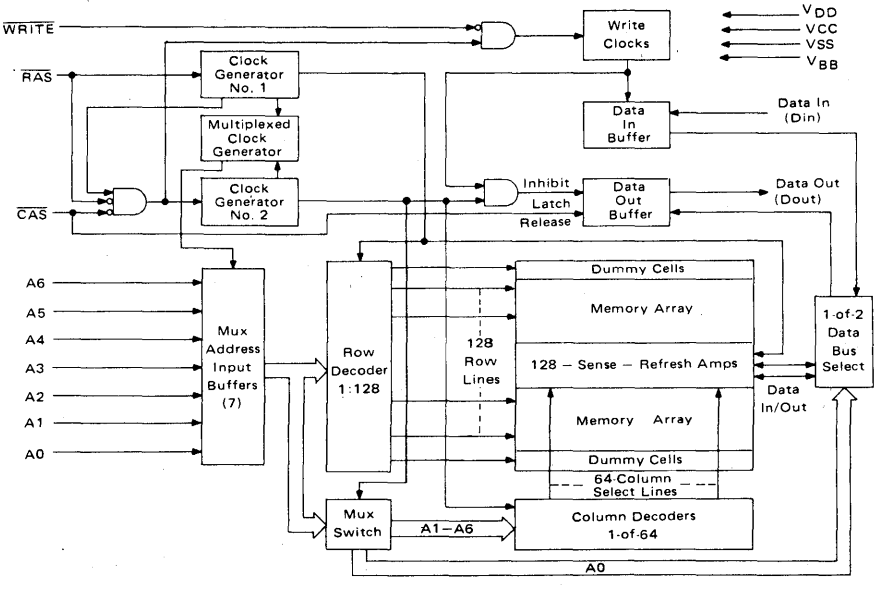
DC CHARACTERISTICS (V_{DD} = 12 V ±10%, V_{CC} = 5.0 V ±10%, V_{BB} = -5.0 V ±10%, V_{SS} = 0 V, T_A = 0 to 70°C.)

Characteristic	Symbol	Min	Max	Units	Notes
Average V_{DD} Power Supply Current	I_{DD1}	–	35	mA	4
V_{CC} Power Supply Current	I_{CC}	–	–	mA	5
Average V_{BB} Power Supply Current	$I_{BB1,3}$	–	200	μA	
Standby V_{BB} Power Supply Current	I_{BB2}	–	100	μA	
Standby V_{DD} Power Supply Current	I_{DD2}	–	1.5	mA	6
Average V_{DD} Power Supply Current during "$\overline{RAS}$ only" cycles	I_{DD3}	–	27	mA	4
Input Leakage Current (any input)	$I_{I(L)}$	–	10	μA	
Output Leakage Current	$I_{O(L)}$	–	10	μA	6, 7
Output Logic 1 Voltage @ I_{out} = -5 mA	V_{OH}	2.4	–	Vdc	2
Output Logic 0 Voltage @ I_{out} = 4.2 mA	V_{OL}	–	0.4	Vdc	

NOTES:

1. All voltages referenced to V_{SS}. V_{BB} must be applied before and removed after other supply voltages.
2. Output voltage will swing from V_{SS} to V_{CC} under open circuit conditions. For purposes of maintaining data in power down mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations. V_{OH}(min) specification is not guaranteed in this mode.
3. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate.
4. Current is proportional to cycle rate; maximum current is measured at the fastest cycle rate.
5. I_{CC} depends upon output loading. The V_{CC} supply is connected to the output buffer only.
6. Output is disabled (open circuit) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1.
7. $0 V \leq V_{out} \leq +5.5 V$.
8. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I\Delta_t}{\Delta V}$

BLOCK DIAGRAM



AC OPERATING CONDITIONS AND CHARACTERISTICS (See Notes 3, 9, 14)
(Read, Write, and Read-Modify-Write Cycles)

RECOMMENDED AC OPERATING CONDITIONS

(V_{DD} = 12 V ±10%, V_{CC} = 5.0 V ±10%, V_{BB} = −5.0 V ±10%, V_{SS} = 0 V, T_A = 0 to 70°C.)

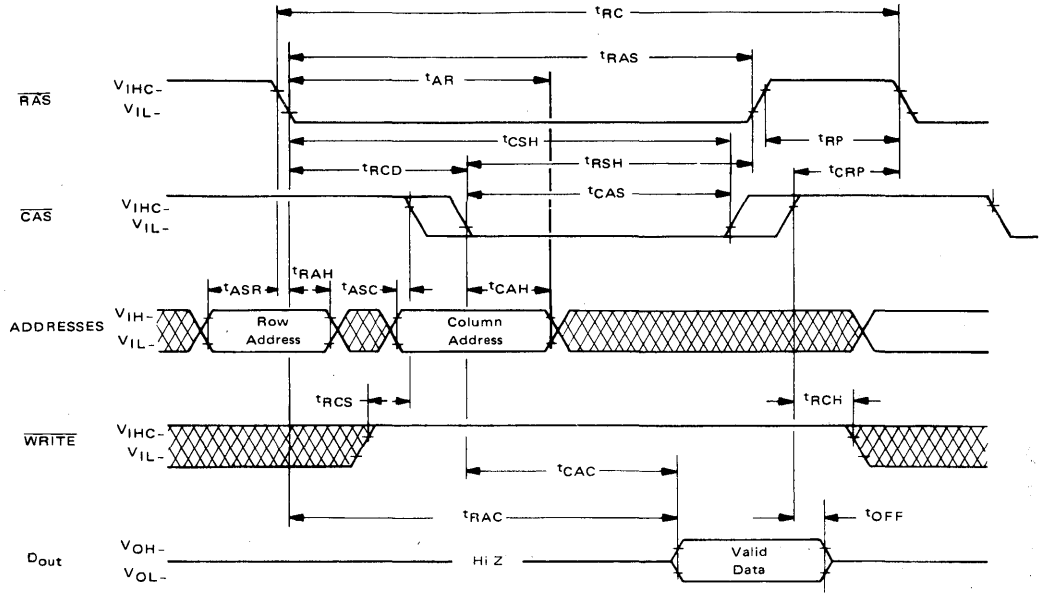
Parameter	Symbol	MCM4116A-15		MCM4116A-20		MCM4116A-25		MCM4116A-30		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	375	–	375	–	410	–	480	–	ns	
Read Write Cycle Time	t_{RWC}	375	–	375	–	515	–	660	–	ns	
Access Time from Row Address Strobe	t_{RAC}	–	150	–	200	–	250	–	300	ns	10, 12
Access Time from Column Address Strobe	t_{CAC}	–	90	–	135	–	165	–	200	ns	11, 12
Output Buffer and Turn-off Delay	t_{OFF}	0	50	0	50	0	60	0	60	ns	17
Row Address Strobe Precharge Time	t_{RP}	100	–	120	–	150	–	180	–	ns	
Row Address Strobe Pulse Width	t_{RAS}	150	10,000	200	10,000	250	10,000	300	10,000	ns	
Column Address Strobe Pulse Width	t_{CAS}	90	10,000	135	10,000	165	10,000	200	10,000	ns	
Row to Column Strobe Lead Time	t_{RCD}	20	60	25	65	35	85	60	100	ns	13
Row Address Setup Time	t_{ASR}	0	–	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	20	–	25	–	35	–	60	–	ns	
Column Address Setup Time	t_{ASC}	−10	–	−10	–	−10	–	−10	–	ns	
Column Address Hold Time	t_{CAH}	45	–	55	–	75	–	100	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	105	–	120	–	160	–	200	–	ns	
Transition Time (Rise and Fall)	t_T	3.0	35	3.0	50	3.0	50	3.0	50	ns	14
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	0	–	ns	
Write Command Hold Time	t_{WCH}	45	–	55	–	75	–	100	–	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	105	–	120	–	160	–	200	–	ns	
Write Command Pulse Width	t_{WP}	45	–	55	–	75	–	100	–	ns	
Write Command to Row Strobe Lead Time	t_{RWL}	60	–	80	–	100	–	180	–	ns	
Write Command to Column Strobe Lead Time	t_{CWL}	60	–	80	–	100	–	180	–	ns	
Data in Setup Time	t_{DS}	0	–	0	–	0	–	0	–	ns	15
Data in Hold Time	t_{DH}	45	–	55	–	75	–	100	–	ns	15
Data in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	105	–	120	–	160	–	200	–	ns	
Column to Row Strobe Precharge Time	t_{CRP}	−20	–	−20	–	−20	–	−20	–	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	100	–	135	–	165	–	200	–	ns	
Refresh Period	t_{RFSH}	–	2.0	–	2.0	–	2.0	–	2.0	ms	
$\overline{WRITE}$ Command Setup Time	t_{WCS}	−20	–	−20	–	−20	–	−20	–	ns	
$\overline{CAS}$ to $\overline{WRITE}$ Delay	t_{CWD}	70	–	95	–	125	–	180	–	ns	16
$\overline{RAS}$ to $\overline{WRITE}$ Delay	t_{RWD}	120	–	160	–	210	–	280	–	ns	16
$\overline{CAS}$ Precharge Time (Page mode cycle only)	t_{CP}	60	–	80	–	100	–	100	–	ns	
Page Mode Cycle Time	t_{PC}	170	–	225	–	275	–	325	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	150	–	200	–	250	–	300	–	ns	

Parameter	Symbol	Typ	Max	Units	Notes
Input Capacitance (A0-A5), D_{in}	C_{I1}	4.0	5.0	pF	9
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}	8.0	10	pF	9
Output Capacitance (D_{out})	C_o	5.0	7.0	pF	7, 9

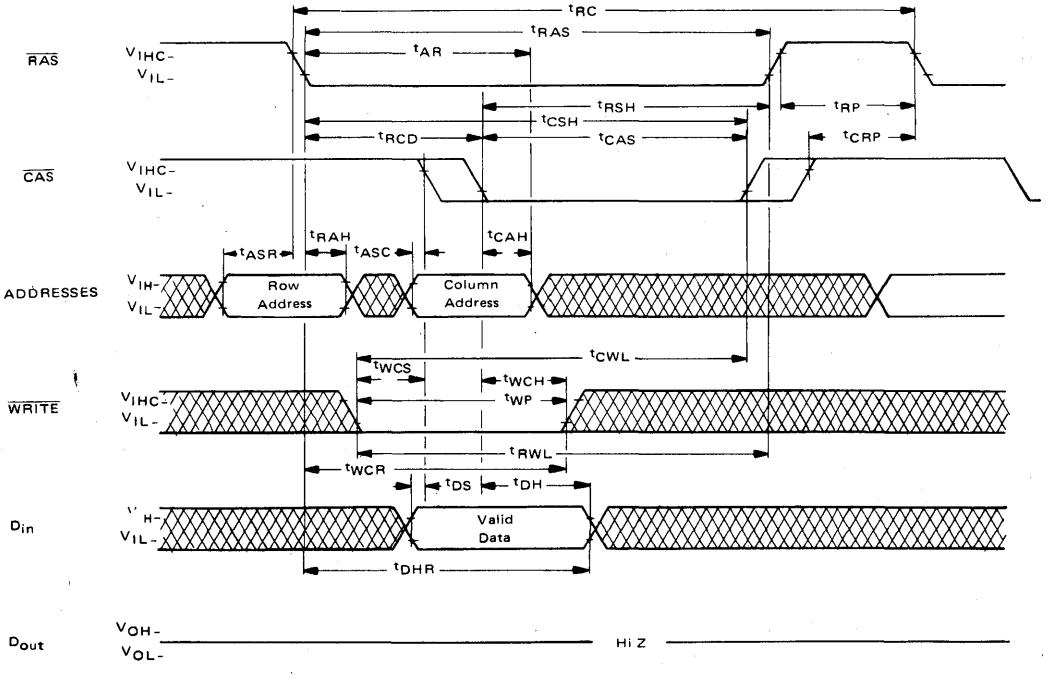
NOTES: (continued)

9. AC measurements assume t_T = 5.0 ns.
10. Assumes that $t_{RCD} + t_T \leq t_{RCD}$ (max).
11. Assumes that $t_{RCD} + t_T \geq t_{RCD}$ (max).
12. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
14. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transistion times are measured between V_{IHC} or V_{IH} and V_{IL}.
15. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
17. Assumes that $t_{CRP} > 50$ ns.

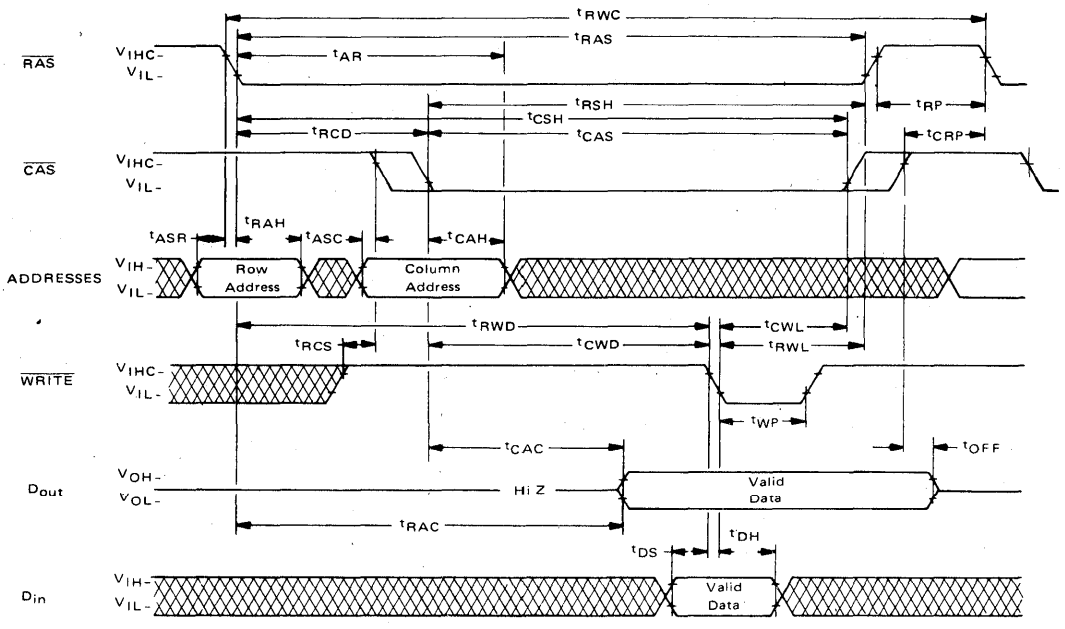
READ CYCLE TIMING



WRITE CYCLE TIMING

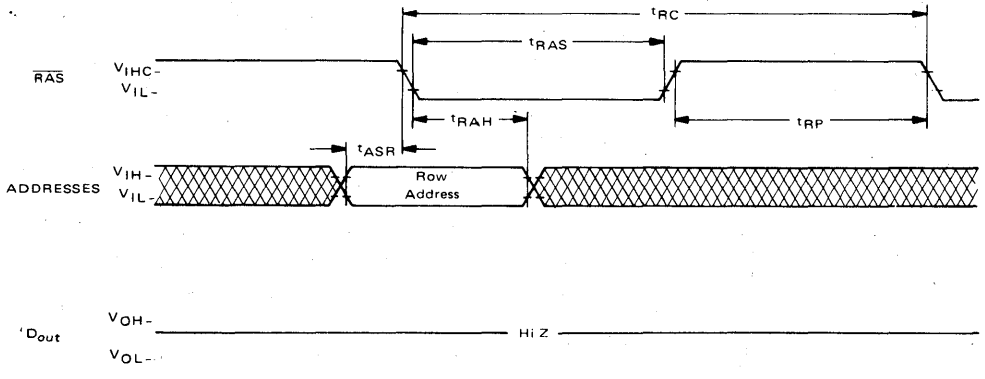


READ-WRITE/READ-MODIFY-WRITE CYCLE

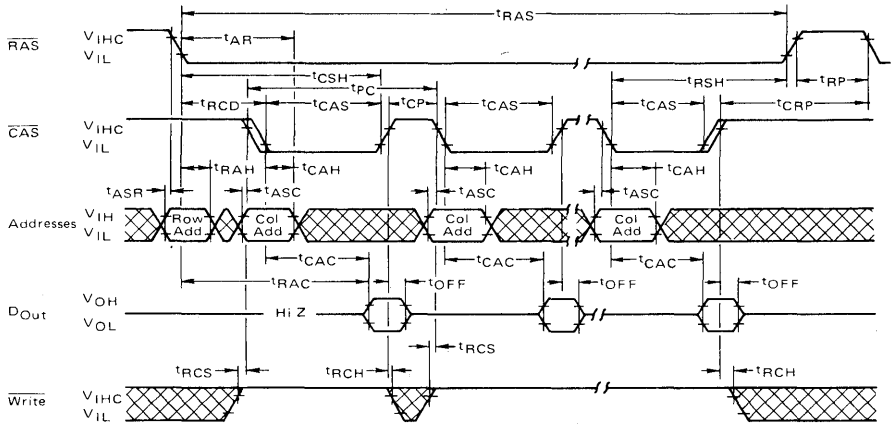


RAS ONLY REFRESH TIMING

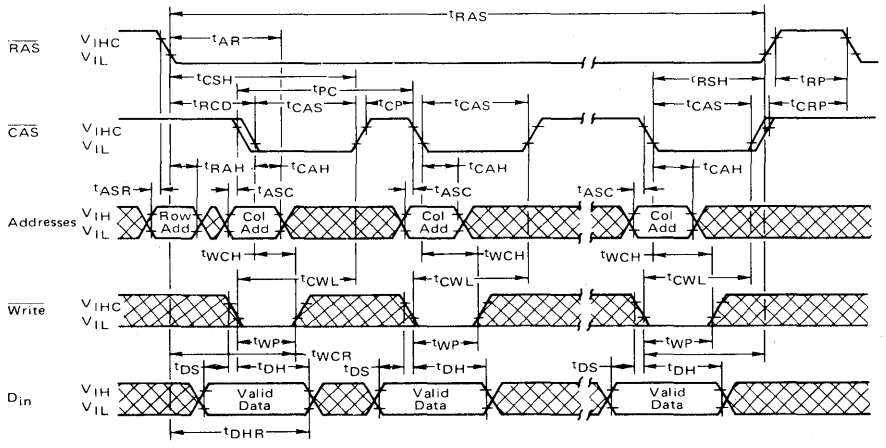
Note: CAS = V_{IHC}, WRITE = Don't Care



PAGE MODE READ CYCLE

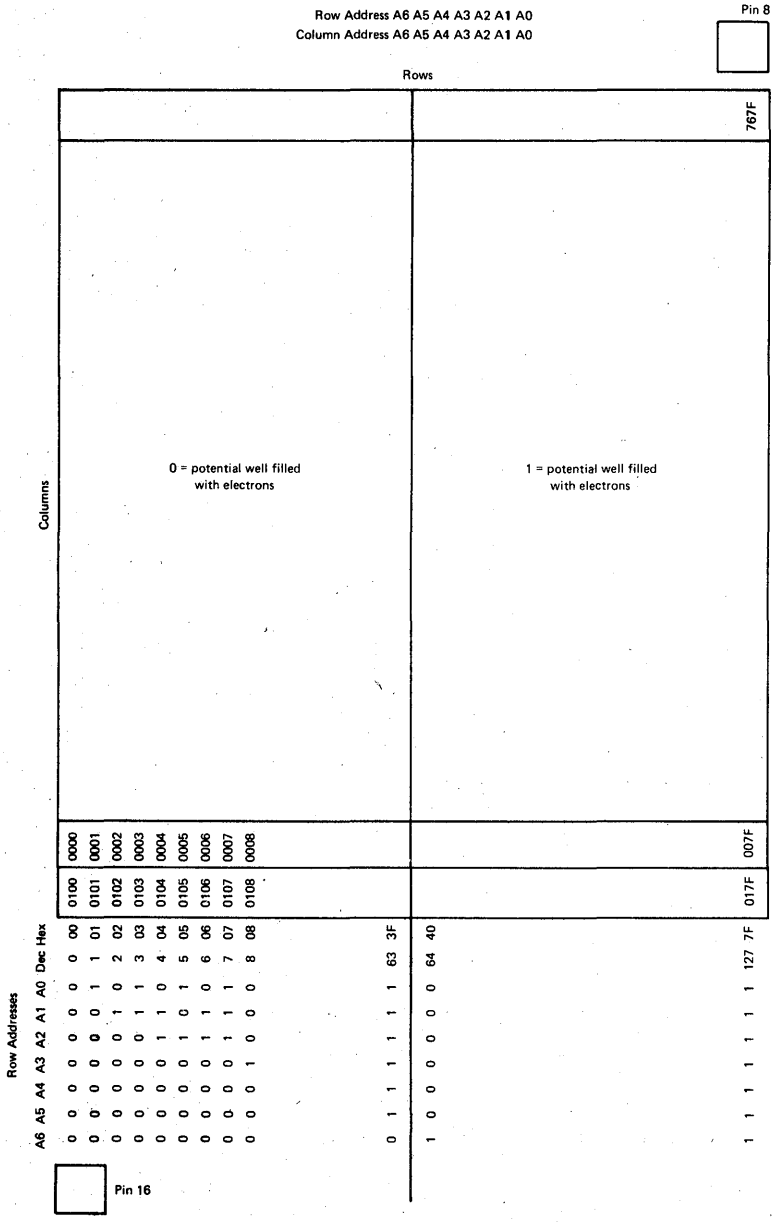


PAGE MODE WRITE CYCLE



2

MCM4116A BIT ADDRESS MAP



Column Addresses								
Hex	Dec	A6	A5	A4	A3	A2	A1	A0
76	118	1	1	1	0	1	1	0
77	119	1	1	1	0	1	1	1
16	30	0	0	1	0	1	1	0
17	31	0	0	1	0	1	1	1
14	28	0	0	1	0	1	0	0
15	29	0	0	1	0	1	0	1
12	26	0	0	1	0	0	1	0
13	27	0	0	1	0	0	1	1
10	24	0	0	1	0	0	0	0
11	25	0	0	1	0	0	0	1
1E	22	0	0	1	1	1	1	0
1F	23	0	0	1	1	1	1	1
1C	20	0	0	1	1	1	0	0
1D	21	0	0	1	1	1	0	1
1A	18	0	0	1	1	0	1	0
1B	19	0	0	1	1	0	1	1
18	16	0	0	1	1	0	0	0
19	17	0	0	1	1	0	0	1
0E	14	0	0	0	1	1	1	0
0F	15	0	0	0	1	1	1	1
0C	12	0	0	0	1	1	0	0
0D	13	0	0	0	1	1	0	1
0A	10	0	0	0	1	0	1	0
0B	11	0	0	0	1	0	1	1
08	8	0	0	0	1	0	0	0
09	9	0	0	0	1	0	0	1
06	6	0	0	0	0	1	1	0
07	7	0	0	0	0	1	1	1
04	4	0	0	0	0	1	0	0
05	5	0	0	0	0	1	0	1
02	2	0	0	0	0	0	1	0
03	3	0	0	0	0	0	1	1
00	0	0	0	0	0	0	0	0
01	1	0	0	0	0	0	0	1

MOTOROLA

MCM4516

Product Preview

16,384-BIT DYNAMIC RAM

The MCM4516 is a 16,384-bit, high-speed, dynamic Random-Access Memory. Organized as 16,384 one-bit words and fabricated using HMOS high-performance, N-channel, silicon-gate technology. This new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

By multiplexing row- and column-address inputs, the MCM4516 requires only eight address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by $\overline{CAS}$ allowing for greater system flexibility.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM4516 incorporates a one-transistor cell design and dynamic storage techniques. In addition to the $\overline{RAS}$-only refresh mode, refresh control function available on pin 1 provides automatic and self-refresh modes.

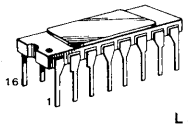
- Organized as 16,384 Words of 1 Bit
- Single +5 Volt Operation
- Fast 120 ns Operation
- Low Power Dissipation:
  200 mW Maximum (Active)
  20 mW Maximum (Standby)
- Three-State Data Output
- Internal Latches for Address and Data Input
- Early-Write Output Capability
- 64K Compatible 128-Cycle, 2 ms Refresh
- Control on Pin 1 for Automatic and Self Refresh
- $\overline{RAS}$-only Refresh Mode
- $\overline{CAS}$ Controlled Output Providing Latched or Unlatched Data
- Upward Pin Compatibility from the 16K RAM (MCM4116) to the 64K RAM (MCM6664)

MOS

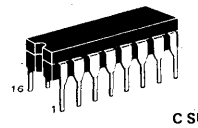
(N-CHANNEL, SILICON-GATE)

16,384-BIT DYNAMIC RAM

2

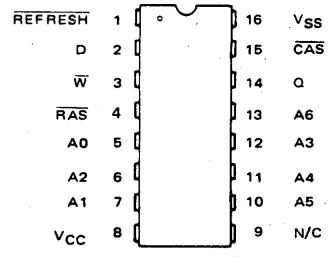


L SUFFIX
CERAMIC PACKAGE
CASE 690



C SUFFIX
FRIT-SEAL
CERAMIC PACKAGE
CASE 620

PIN ASSIGNMENT



OUTPUT BUFFER TRUTH TABLE

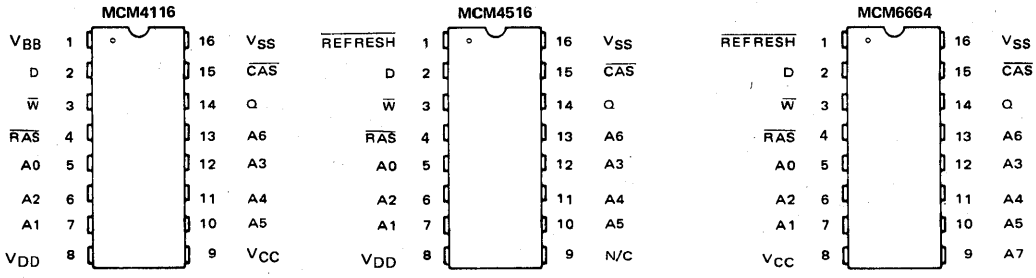
Internal Early Write	$\overline{CAS}$	Refresh Control (CAS Internal)		Output Buffer
H	X	X	(X)	Hi-Z
X	H	X	(X)	Hi-Z
L	L	L	(H)	Maintains Previous Data
L	L	H	(L)	Active

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

This is advance information and specifications are subject to change without notice.

2

PIN ASSIGNMENT COMPARISON



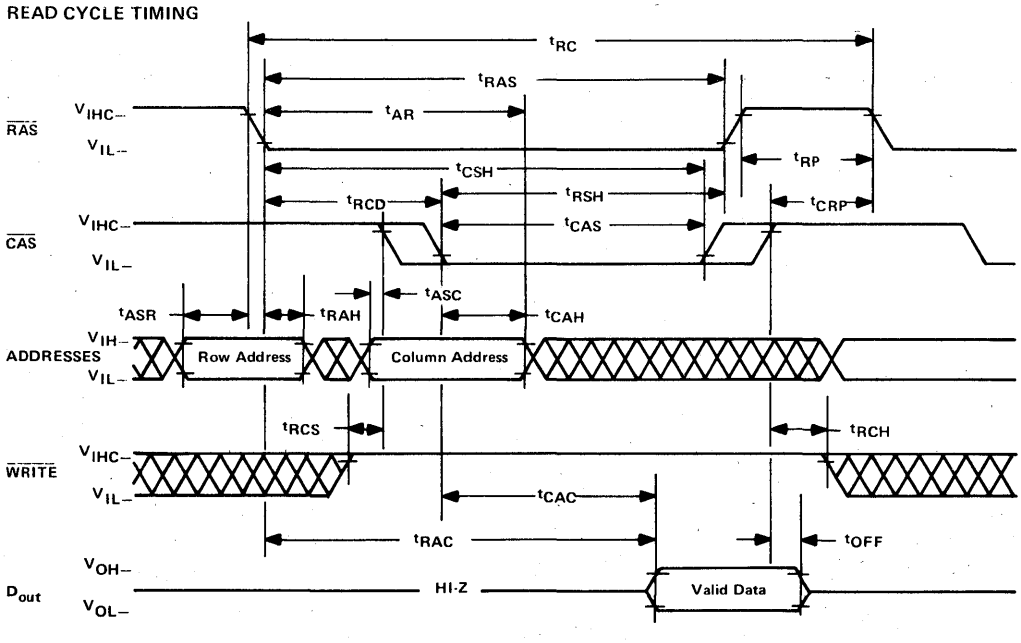
PIN VARIATIONS

PIN NUMBER	MCM4116	MCM4516	MCM6664
1	V_{BB} (–5 V)	$\overline{REFRESH}$	$\overline{REFRESH}$
8	V_{DD} (+12 V)	V_{CC}	V_{CC} (+5 V)
9	V_{CC} (+5 V)	N/C	A7

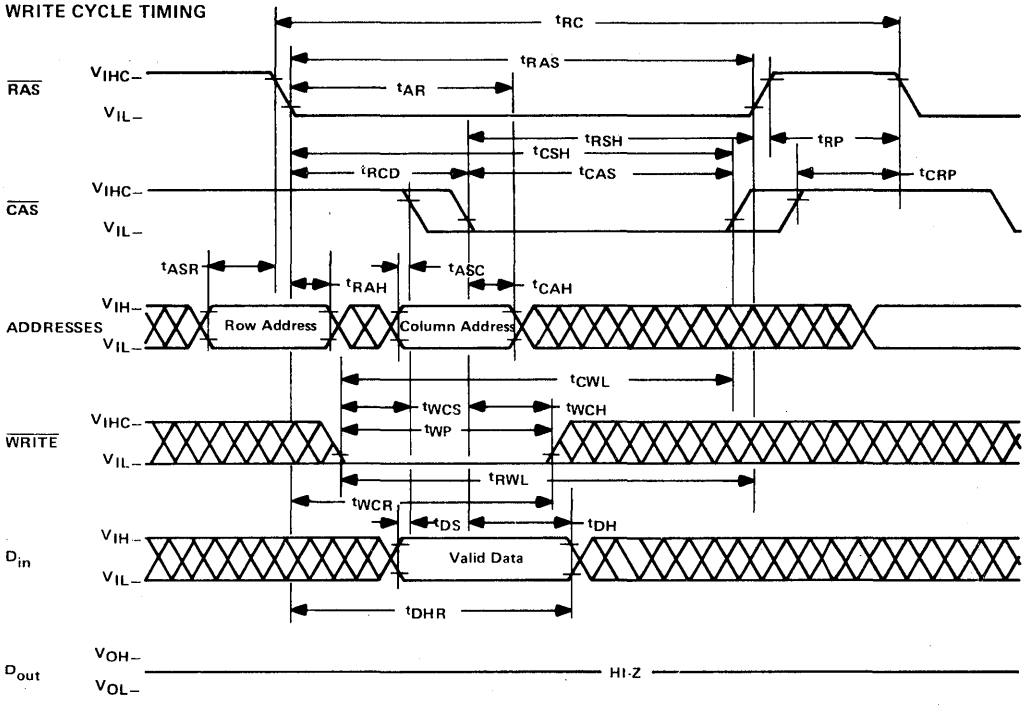
ON-CHIP REFRESH FEATURES/BENEFITS

- Reduce System Refresh Controller Design Problem
- Reduce System Parts Count
- Reduce System Noise Increasing System Reliability
- Reduce System Power During Refresh

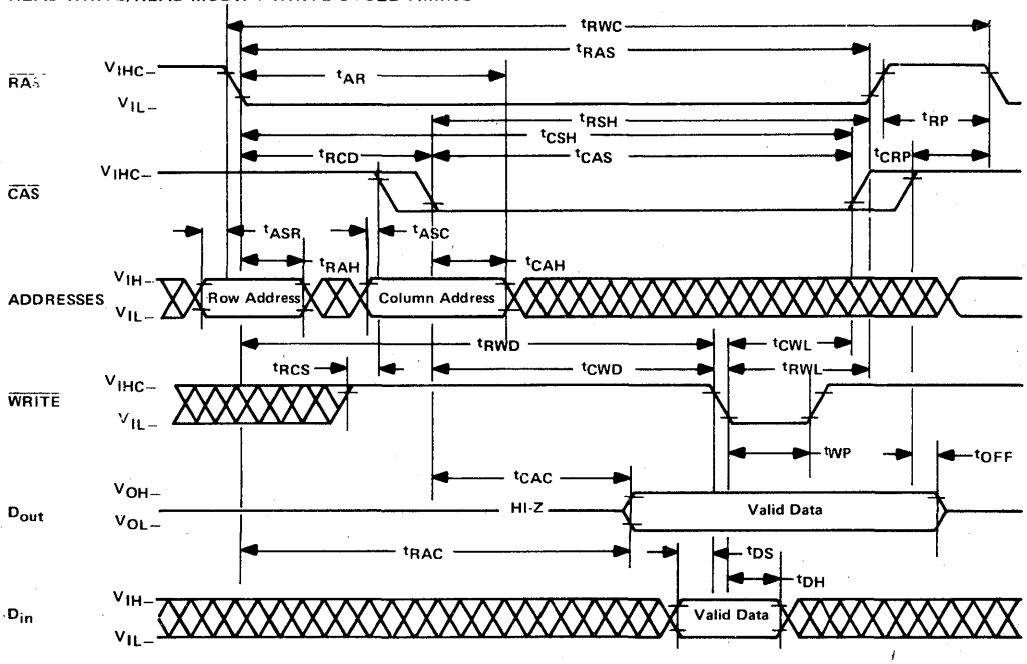
READ CYCLE TIMING



WRITE CYCLE TIMING

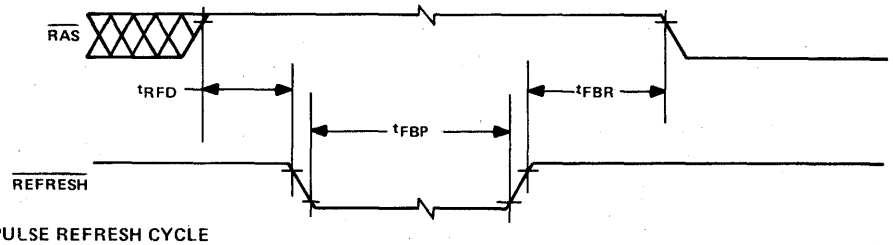


READ-WRITE/READ-MODIFY-WRITE CYCLE TIMING

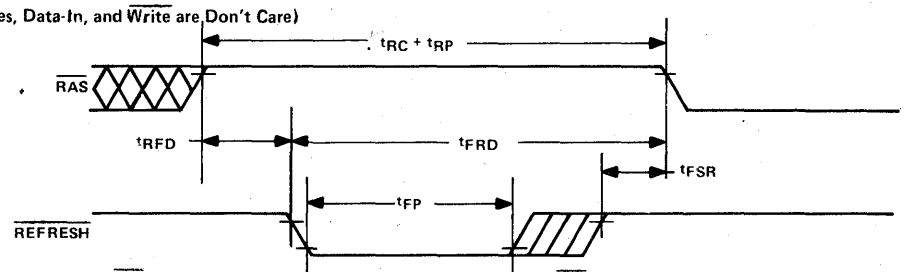


2

SELF REFRESH MODE (Battery Backup)
($\overline{CAS}$[1], Addresses, Data-In, and Write are Don't Care)

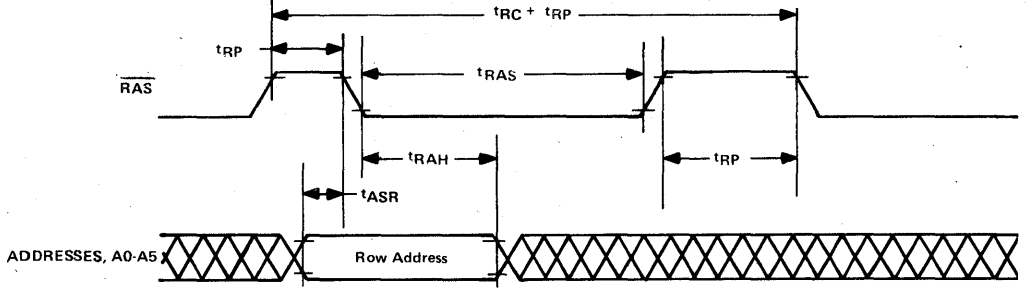


AUTOMATIC PULSE REFRESH CYCLE
($\overline{CAS}$[1], Addresses, Data-In, and $\overline{Write}$ are Don't Care)



[1]$\overline{CAS}$ controls the output data. If $\overline{CAS}$ remains low the previous output will remain valid. When $\overline{CAS}$ is brought high, the output will assume a high-impedance state.

RAS-ONLY REFRESH CYCLE
(Data-in and Write are Don't Care, $\overline{CAS}$ is HIGH)



MOTOROLA

MCM6604A

4096-BIT DYNAMIC RANDOM ACCESS MEMORY

The MCM6604A is a 4096-bit, high-speed, dynamic Random Access Memory designed for high-performance, low-cost applications in mainframe and buffer memories and peripheral storage. Organized as 4096 one-bit words and fabricated using Motorola's highly reliable N-channel silicon gate technology, this device optimizes speed, power, and density tradeoffs.

By multiplexing row and column address inputs, the MCM6604A requires only six address lines and permits packaging in Motorola's standard 16-pin dual in-line packages. Complete address decoding is done on chip with address latches incorporated.

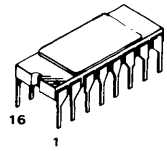
All inputs are TTL compatible, and the output is 3-state TTL compatible. The MCM6604A incorporates a one-transistor cell design and dynamic storage techniques, with each of the 64-row addresses requiring a refresh cycle every 2.0 milliseconds.

- Organized as 4096 Words of 1 Bit
- Maximum Access Time = 250 ns – MCM6604AL2, C2
  300 ns – MCM6604AL4, C4
  350 ns – MCM6604AL, C
- Minimum Read and Write Cycle Time =
  375 ns – MCM6604AL2, C2
  425 ns – MCM6604AL4, C4
  500 ns – MCM6604AL, C
- Low Power Dissipation
  500 mW Typical (Active)
  18 mW Typical (Standby)
- 3-State Output
- On-Chip Latches for Address, Chip Select, and Data In
- Power Supply Pins on Package Corners for Optimum Layout
- Standard 16-Pin Package
- Compatible with the Popular 2104/MK4096/4096/4027/MK4027

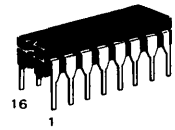
MOS

(N-CHANNEL, SILICON-GATE)

4096-BIT DYNAMIC RANDOM ACCESS MEMORY

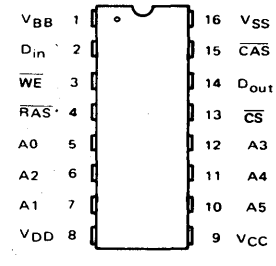


L SUFFIX
CERAMIC PACKAGE
CASE 690



C SUFFIX
FRIT-SEAL
CERAMIC PACKAGE
CASE 620

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{BB}*	V_{in}, V_{out}	−0.3 to +20	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Output Current (Short Circuit)	I_{out}	50	mAdc

*($V_{SS} - V_{DD} \geq 4.5$ V)

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. V_{BB} must be applied prior to V_{CC} and V_{DD}. V_{BB} must also be the last power supply switched off.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS} = Ground)

Parameter		Symbol	Min	Nom	Max	Unit
Supply Voltage		V_{DD}	11.4	12.0	12.6	Vdc
		V_{CC}	4.5	5.0	5.5	Vdc
		V_{BB}	-4.5	-5.0	-5.5	Vdc
Input High Voltage	An, $\overline{CS}$, D_{in}	V_{IH}	2.4	–	5.0	Vdc
	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$		2.7	–	5.0	
Input Low Voltage	All Inputs	V_{IL}	-1.0	–	0.8	Vdc

DC CHARACTERISTICS (V_{DD} = 12 V ±5%, V_{CC} = 5.0 V ±10%, V_{BB} = -5.0 V ±10%, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current, Any Input (V_{in} = 0 to 7.0 V)	I_{in}	–	–	10	μA
Output High Voltage (I_O = -5.0 mA)	V_{OH}	2.4	–	–	Vdc
Output Low Voltage (I_O = 2.0 mA)	V_{OL}	–	–	0.4	Vdc
Output Leakage Current (Output Disabled by $\overline{CS}$ Input)	I_{LO}	–	–	10	μA
Average Supply Current, Active Mode ($T_{cyc(W)}$ = min)	I_{DDA}	–	38	50	mA
	I_{CCA}	–	20	100	μA
	I_{BBA}	–	–	75	μA
Supply Current, Standby Mode	I_{DDS}	–	1.3	2.0	mA
	I_{CCS}	–	–	10	μA
	I_{BBS}	–	–	75	μA

EFFECTIVE CAPACITANCE (Full operating voltage and temperature range, periodically sampled rather than 100% tested.)

Characteristic		Symbol	Max	Unit
Input Capacitance	A0–A5	$C_{in(EFF)}$	10	pF
	$\overline{RAS}$, $\overline{CAS}$, D_{in}, $\overline{WE}$, $\overline{CS}$		7.0	
Output Capacitance		$C_{out(EFF)}$	8.0	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS
(Read, Write, and Read-Modify-Write Cycles)

RECOMMENDED AC OPERATING CONDITIONS (V_{DD} = 12 V ±5%, V_{CC} = 5.0 V ±10%, V_{BB} = -5.0 V ±10%, T_A = 0 to 70°C)

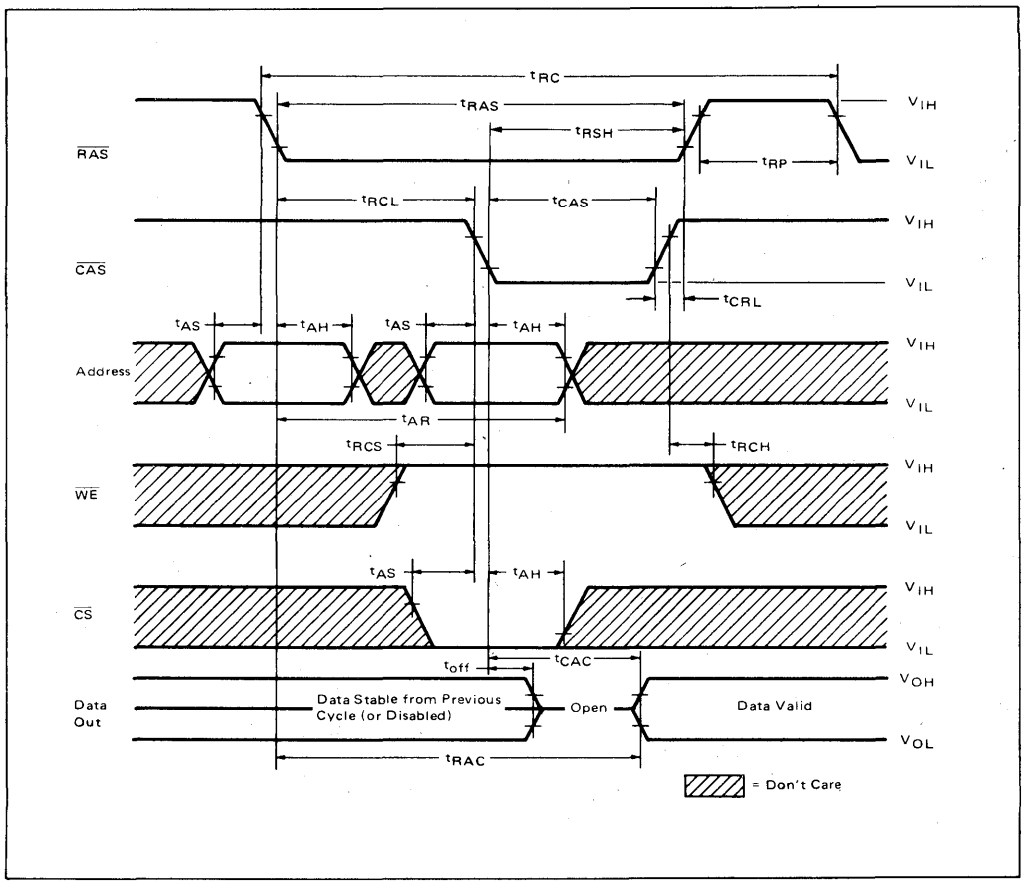
Parameter	Symbol	MCM6604AL, C		MCM6604AL2, C2		MCM6604AL4, C4		Unit
		Min	Max	Min	Max	Min	Max	
Random Read or Write Cycle Time	t_{RC}	500	–	375	–	425	–	ns
$\overline{RAS}$ Pulse Width	t_{RAS}	350	10,000	250	10,000	300	10,000	ns
Row Address Strobe Hold Time	t_{RSH}	200	–	140	–	170	–	ns
Row Address Strobe Precharge Time	t_{RP}	150	–	125	–	125	–	ns
Row to Column Strobe Lead Time (Note 1)	t_{RCL}	110	150	70	110	90	130	ns
$\overline{CAS}$ Pulse Width	t_{CAS}	200	10,000	140	10,000	170	10,000	ns
Column to Row Strobe Lead Time	t_{CRL}	-50	+50	-40	+40	-50	+50	ns
Address Setup Time	t_{AS}	0	–	0	–	0	–	ns
Address Hold Time	t_{AH}	100	–	60	–	80	–	ns
$\overline{RAS}$ Address Release Time	t_{AR}	250	–	170	–	210	–	ns
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	ns
Read Command Hold Time	t_{RCH}	100	–	60	–	80	–	ns
Write Command to Column Strobe Lead Time	t_{CWL}	200	–	140	–	170	–	ns
Write Command Hold Time (Note 2)	t_{WCH}	150	–	110	–	130	–	ns
Write Command Pulse Width	t_{WP}	200	–	140	–	170	–	ns
Data In Setup Time	t_{DS}	0	–	0	–	0	–	ns
Data In Hold Time	t_{DH}	150	–	110	–	130	–	ns
Refresh Period	t_{REF}	–	2.0	–	2.0	–	2.0	ms

1. If t_{RCL} is greater than the maximum recommended value shown in this table, t_{cyc} and t_{RAC} will increase by the amount that t_{RCL} exceeds the value shown.
2. The Write Command Hold Time is important only when normal random write cycles are being performed. During a read-write or a read-modify-write cycle, the limiting parameter is the Write Command Pulse Width.

AC CHARACTERISTICS ($t_T = t_r = t_f = 10$ ns, Load = 1 MC74H00 Series TTL Gate, $C_{L(EFF)} = 50$ pF)

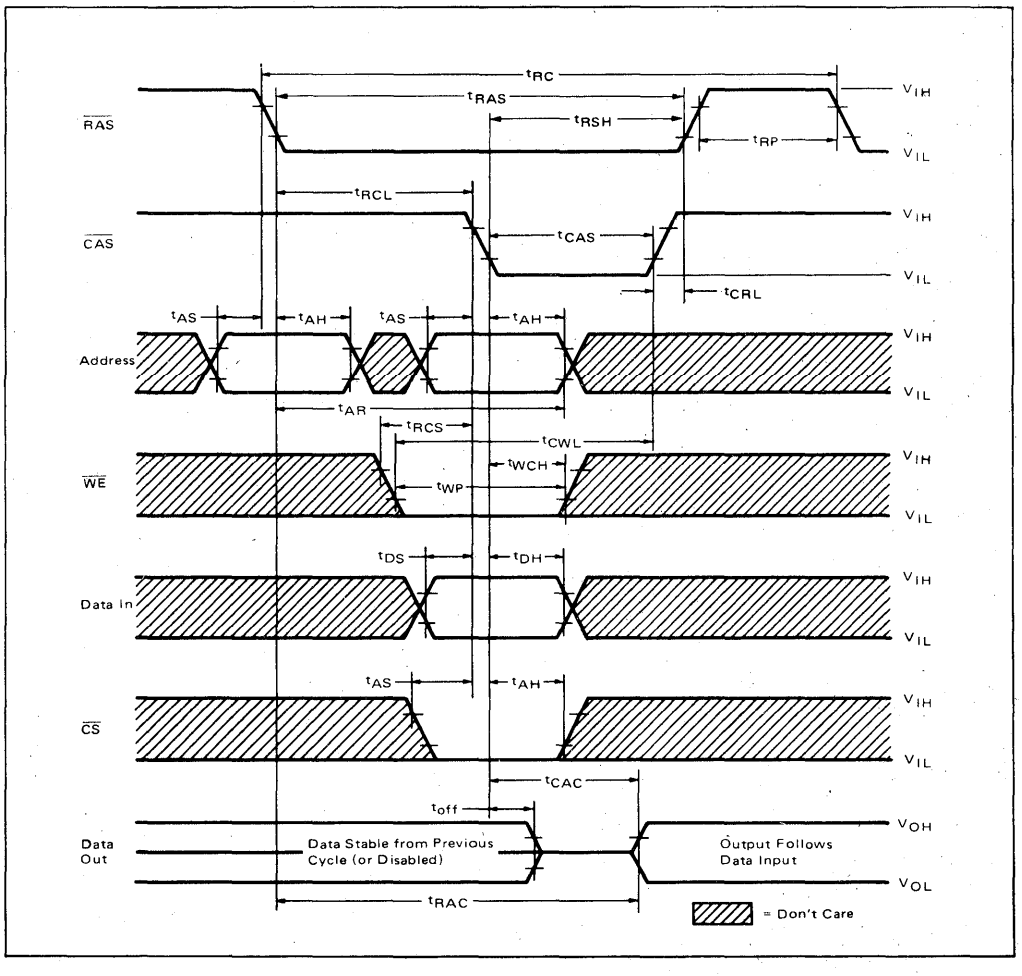
Characteristic	Symbol	MCM6604AL, C Max	MCM6604AL2, C2 Max	MCM6604AL4, C4 Max	Unit
Access Time from Row Address Strobe (110 ns ≤ $t_{RCL} + t_T$ ≤ 150 ns for MCM6604AL, C) (70 ns ≤ $t_{RCL} + t_T$ ≤ 110 ns for MCM6604AL2, C2) (90 ns ≤ $t_{RCL} + t_T$ ≤ 130 ns for MCM6604AL4, C4)	t_{RAC}	350	250	300	ns
Access Time from Column Address Strobe	t_{CAC}	200	140	170	ns
Output Buffer Turn-Off Delay	t_{off}	100	65	85	ns

READ CYCLE TIMING



2

WRITE CYCLE TIMING



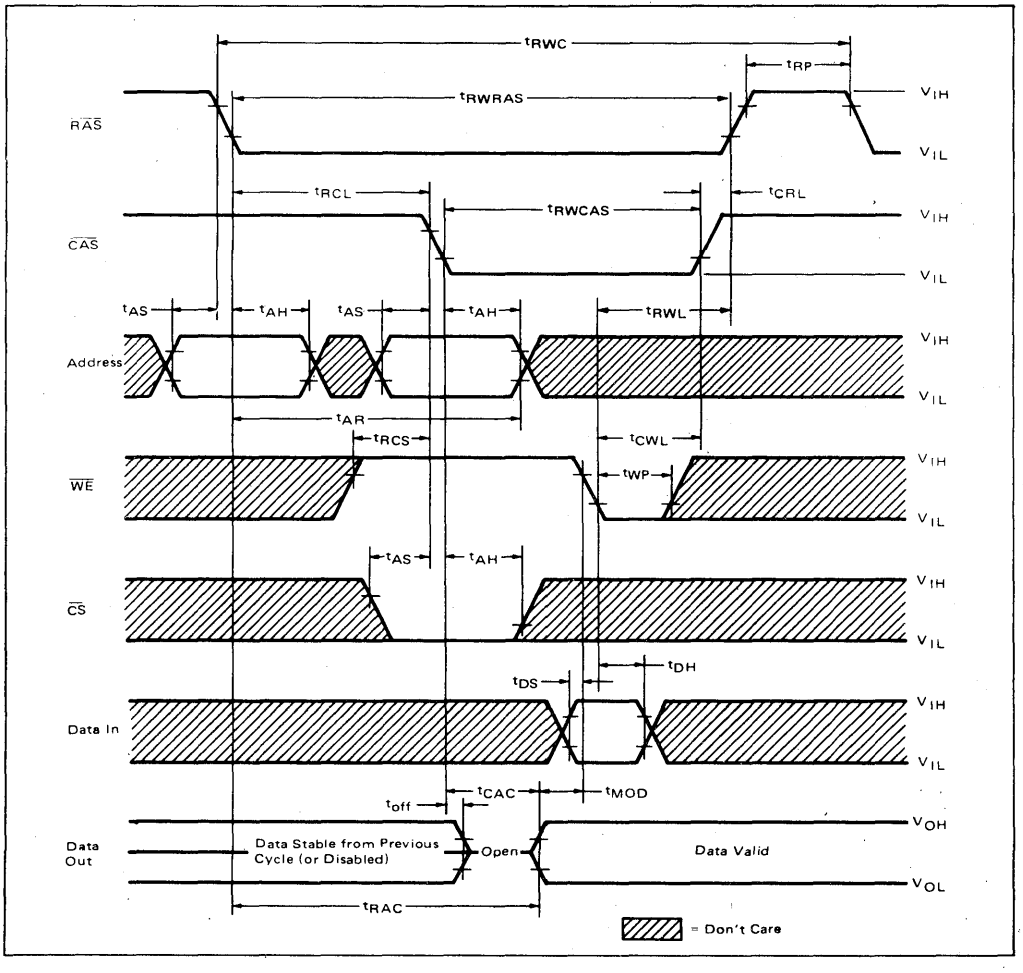
AC OPERATING CONDITIONS AND CHARACTERISTICS
(Read-Modify-Write Cycle)

RECOMMENDED AC OPERATING CONDITIONS (V_{DD} = 12 V ±5%, V_{CC} = 5.0 V ±10%, V_{BB} = -5.0 V ±10%, T_A = 0 to 70°C)

Note: Parameters not listed are the same as for a Read or Write Cycle.

Parameter	Symbol	MCM6604AL, C		MCM6604AL2, C2		MCM6604AL4, C4		Unit
		Min	Max	Min	Max	Min	Max	
Read-Modify-Write Cycle Time	t_{RWC}	700	–	515	–	595	–	ns
Row Address Strobe Pulse Width	t_{RWRAS}	550	10,000	390	10,000	470	10,000	ns
Column Address Strobe Pulse Width	t_{RWCAS}	400	10,000	280	10,000	340	10,000	ns
$\overline{RAS}$ Hold Time	t_{RWL}	200	–	140	–	170	–	ns
Modify Time	t_{MOD}	0	10,000	0	10,000	0	10,000	ns

READ – MODIFY – WRITE TIMING



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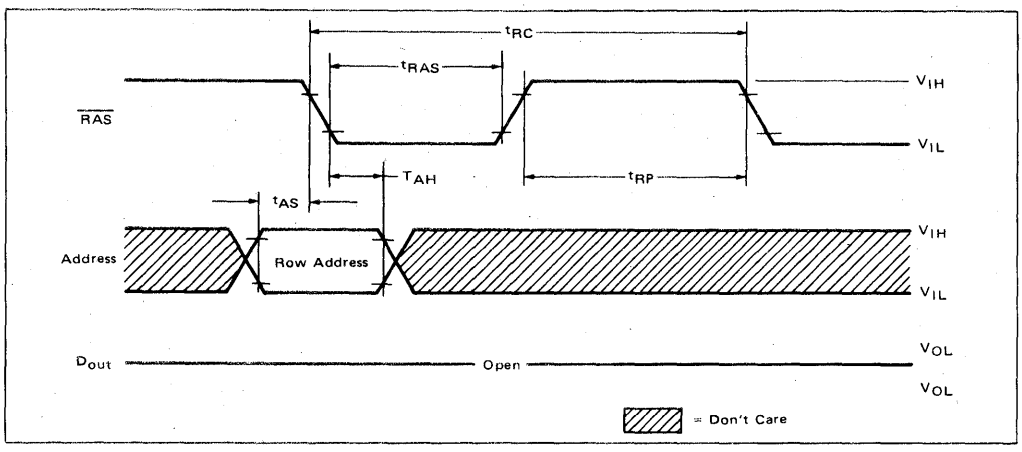
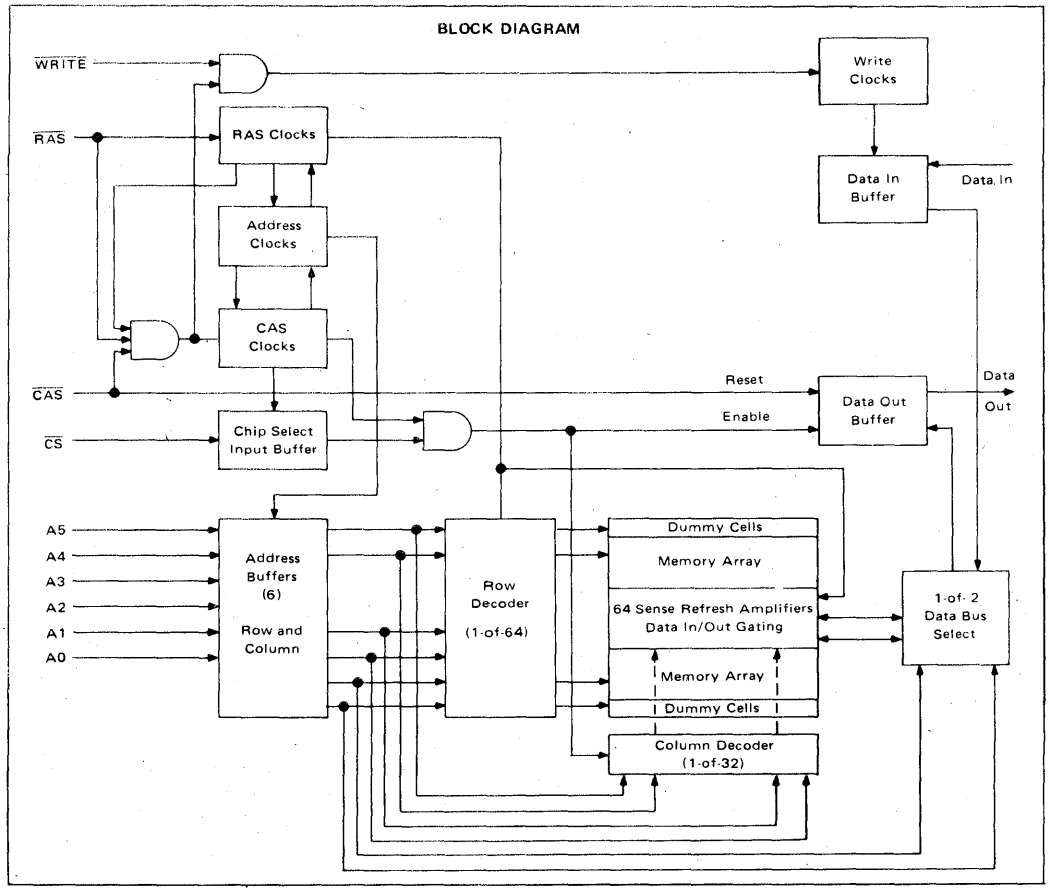
$\overline{RAS}$ ONLY REFRESH TIMING



BLOCK DIAGRAM



OPERATING CHARACTERISTICS

DATA OUTPUT

In order to simplify the memory system design and reduce the total package count, the MCM6604A contains an input data latch and a buffered output data latch. The state of the output latch and buffer at the end of a memory cycle will depend on the type of memory cycle performed and whether the chip is selected or unselected for that memory cycle.

A chip will be unselected during a memory cycle if:

(1) The chip receives both $\overline{RAS}$ and $\overline{CAS}$ signals, but no $\overline{Chip\ Select}$ signal.

(2) The chip receives a $\overline{CAS}$ signal but no $\overline{RAS}$ signal. With this condition, the chip will be unselected regardless of the state of $\overline{Chip\ Select}$ input.

If, during a read, write, or read-modify-write cycle, the chip is unselected, the output buffer will be in the high impedance state at the end of the memory cycle. The output buffer will remain in the high impedance state until the chip is selected for a memory cycle.

For a chip to be selected during a memory cycle, it must receive the following signals: $\overline{RAS}$, $\overline{CAS}$, and $\overline{Chip\ Select}$. The state of the output latch and buffer of a selected chip during the following type of memory cycles would be:

(1) Read Cycle – On the negative edge of $\overline{CAS}$, the output buffer will unconditionally go to a high impedance state. It will remain in this state until access time. At this time, the output latch and buffer will assume the logic state of the data read from the selected cell. This output state will be maintained until the chip receives the next $\overline{CAS}$ signal.

(2) Write Cycle – If the $\overline{WE}$ input is switched to a logic 0 before the $\overline{CAS}$ transition, the output latch and buffer will be switched to the state of the data input at the end of the access time. This logic state will be maintained until the chip receives the next $\overline{CAS}$ signal.

(3) Read-Modify-Write – Same as a read cycle.

DATA INPUT

Data to be written into a selected storage cell of the memory chip is first stored in the on-chip data latch. The gating of this latch is performed with a combination of the $\overline{WE}$ and $\overline{CAS}$ signals. The last of these signals to make a negative transition will strobe the data into the latch. If the $\overline{WE}$ input is switched to a logic 0 at the beginning of a write cycle, the falling edge of $\overline{CAS}$ strobes the data into the latch. The data setup and hold times are then referenced to the negative edge of $\overline{CAS}$.

If a read-modify-write cycle is being performed, the $\overline{WE}$ input would not make its negative transistion until after the $\overline{CAS}$ signal was enabled. Thus, the data would not be strobed into the latch until the negative transition of $\overline{WE}$. The data setup and hold times would now be referenced to the negative edge of the $\overline{WE}$ signal. The only other timing constraints for a write-type cycle is that both the $\overline{CAS}$ and $\overline{WE}$ signals remain in the logic 0 state for a sufficient time to accomplish the permanent storage of the data into the selected cell.

INPUT/OUTPUT LEVELS

All of the inputs to the MCM6604A are TTL compatible, except $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$. The latter control inputs require a slightly higher input voltage, V_{IH} = 2.7 V minimum, which can be met with memory address buffers such as the MC3459.

The inputs feature high impedance and low capacitance (< 10 pF) characteristics which will minimize the driver requirements in a memory system. The three-state data output buffer is TTL compatible and has sufficient current sink capability (2 mA) to drive one high-speed TTL load. The output buffer also has a separate V_{CC} pin so that it can be powered from the same supply as the logic being employed.

REFRESH

In order to ensure or maintain valid data, each of the 64 internal rows of the MCM6604A must be refreshed once every 2 ms. Any read, write, or read-modify-write cycle will refresh an entire internally selected row. However, if a write or read-modify-write cycle is used to perform a refresh cycle, the chip must be deselected.

The MCM6604A can also be refreshed by employing only the $\overline{RAS}$ cycle. This refresh mode will not shorten the refresh cycle time; the minimum switching time for $\overline{RAS}$ still holds. However, the system standby power can be reduced by approximately 30%. It should also be noted that, regardless of the type of refresh cycle employed, all of the minimum and maximum timing restrictions including address setup and hold times must be observed.

TIMING CONSIDERATIONS

The timing of $\overline{RAS}$ and $\overline{CAS}$ as well as their timing relationships must be understood by the designer in order to obtain maximum performance in a system. The $\overline{RAS}$ and $\overline{CAS}$ clocks have minimum and maximum pulse widths, t_{RAS} (t_{RWRAS}) and t_{CAS} (t_{RWCAS}), respectively. These clock limits must not be violated to ensure proper device operation and data integrity. Once a cycle has been initiated by driving $\overline{RAS}$ and/or $\overline{CAS}$ low, it must not be aborted prior to fulfilling the minimum clock signal pulse width(s). Also, a new cycle cannot be initiated until the minimum precharge time, t_{RP}, has been met.

The read access time (t_{ACC}) is a function of the row to column strobe lead time (t_{RCL}), the $\overline{CAS}$ transistion from high to low (t_f), and the access time from column address

strobe (t_{CAC}) as noted in the following equation:

$$t_{ACC} = t_{RCL} + t_f + t_{CAC} \quad (1)$$

If the $t_{RCL} + t_f$ time is less than or equal to the specified t_{RCL} maximum limit, then the device access time becomes:

$$t_{ACC} = t_{RAC} \text{ (access time from the leading edge of } \overline{RAS}) \quad (2)$$

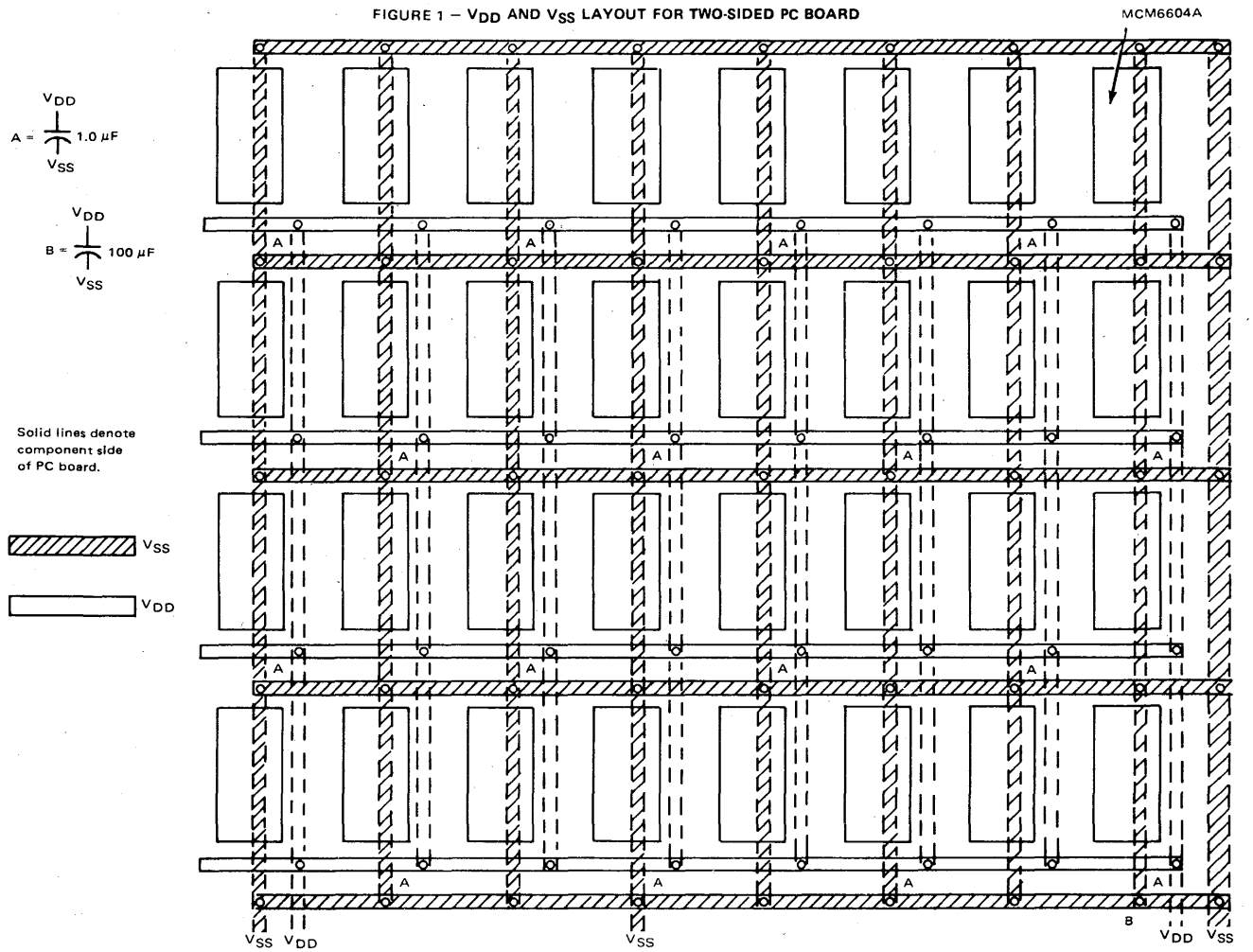
Note from the ac electrical characteristics that t_{RAC} is specified for a given timing skew of t_{RCL}; for the MCM6604AL, the t_{RAC} is 350 ns maximum for 110 ns $\leqslant t_{RCL} + t_f \leqslant$ 150 ns. The 40 ns variation in the falling edge of $\overline{CAS}$, for a given t_{RAC} maximum, is given to allow for system timing skew in the generation of $\overline{CAS}$. This will ensure minimum system access time since the timing skew of $\overline{CAS}$ has been accounted for at the device.

The gating of chip select ($\overline{CS}$) is also designed to minimize system access time. Note from the timing diagrams that $\overline{CS}$ does not have to be valid until the leading edge of $\overline{CAS}$. Since the memory device does not have to be selected at the start of a memory cycle, the system decode time for $\overline{CS}$ does not enter into the system access time.

The minimum overlap of $\overline{RAS}$ and $\overline{CAS}$ during a memory cycle is defined by t_{RSH}. A minimum overlap is required to keep the write control logic on for a sufficient time to ensure adequate charge or discharge of the selected storage capacitor during a write cycle.

The termination of the $\overline{RAS}$ and $\overline{CAS}$ down time is defined by t_{CRL}. This parameter defines the maximum lead (-) or lag (+) time that the trailing edge of $\overline{CAS}$ can have with respect to the trailing edge of $\overline{RAS}$. Note that for a memory system requiring minimum cycle time, $\overline{CAS}$ may lead $\overline{RAS}$ by the specified amount, although $\overline{CAS}$ cannot lag $\overline{RAS}$. This restriction must be placed on t_{CRL} for minimum cycle time since t_{RSH} would be violated; $\overline{CAS}$ can lag $\overline{RAS}$ for the specified maximum time provided the minimum t_{RSH} time is not violated.

FIGURE 1 – V_{DD} AND V_{SS} LAYOUT FOR TWO-SIDED PC BOARD



MOTOROLA

MCM6605A

4096-BIT DYNAMIC RANDOM ACCESS MEMORY

The MCM6605A is a 4096-bit high-speed dynamic Random Access Memory designed for high-performance, low-cost applications in mainframe and buffer memories and peripheral storage. Organized as 4096 one-bit words, these memories are fabricated using selective oxidation N-channel silicon gate technology to optimize device speed, power and density tradeoffs.

All address and control inputs are TTL compatible except for a single high-level clock (Chip Enable). Complete address decoding is done on chip and address latches are incorporated for ease of use. Refresh of the entire memory can be accomplished by sequentially cycling through addresses A0-A4 (32 cycles) a maximum of every 2.0 milliseconds.

The MCM6605A uses a three-transistor memory cell to simplify internal sense amplifier requirements. Output data is inverted with respect to input data. The outputs are 3-state TTL configuration and require no external sense amplifier. Outputs are in the high impedance (floating) state when either the Chip Enable is in the low state or the Chip Select is in the high state.

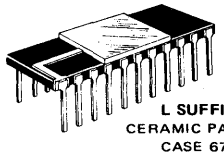
- Organized as 4096 Words of 1 Bit

	L1, P1	L2,P2	L, P
• Maximum Access Time =	150 ns	200 ns	300 ns
• Minimum Read Cycle Time =	290 ns	360 ns	470 ns
• Minimum Write Cycle Time =	390 ns	490 ns	590 ns
• Minimum Read Modify Write Cycle Time =	390 ns	490 ns	590 ns

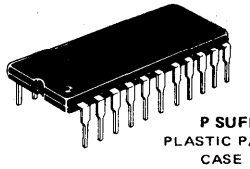
- Low Power Dissipation
  335 mW Typical (Active)
  2.6 mW Typical (Standby with Refresh)
- Easy Refresh – Only 32 Cycles Every 2.0 ms
- TTL Compatible
- 3-State Output
- Address Latches On Chip
- Power Supply Pins on Package Corners for Layout Simplification
- Typical Applications:
  Main Memory
  Buffer Memory
  Peripheral Storage

MOS
(N-CHANNEL, SILICON-GATE)

4096-BIT DYNAMIC RANDOM ACCESS MEMORY

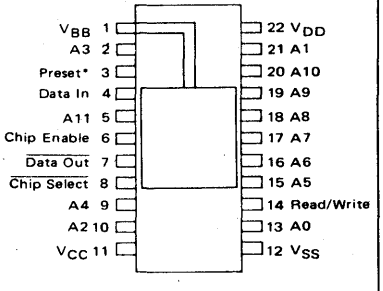


L SUFFIX
CERAMIC PACKAGE
CASE 677



P SUFFIX
PLASTIC PACKAGE
CASE 708

PIN ASSIGNMENT



*See Applications Information

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{BB}	V_{in}, V_{out}	-0.3 to +20	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS (Referenced to V_{SS}).

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{DD}	11.4	12	12.6	Vdc
	V_{CC}	4.5	5.0	5.5	Vdc
	V_{SS}	0	0	0	Vdc
	V_{BB}	-5.25	-5.0	-4.75	Vdc
Logic Levels Input High Voltage (A_n, D_{in}, R/W, $\overline{CS}$)	V_{IH}	3.0	–	V_{DD} + 0.6	Vdc
Input Low Voltage (A_n, D_{in}, R/W, $\overline{CS}$)	V_{IL}	-1.0	–	0.8	Vdc
Chip Enable High Voltage	V_{CEH}	V_{DD} - 0.6	–	V_{DD} + 0.6	Vdc
Chip Enable Low Voltage	V_{CEL}	-1.0	–	0.8	Vdc

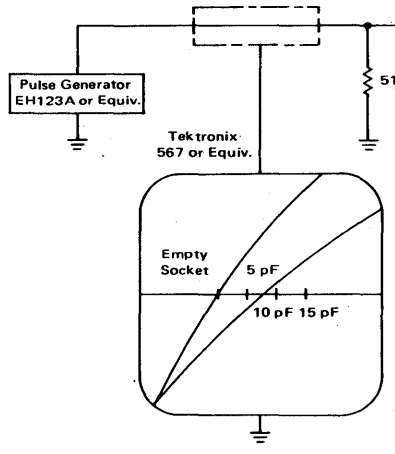
DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (A_n, D_{in}, R/W, $\overline{CS}$, *Preset*) (V_{in} = 0 to V_{DD} + 1.0 V)	I_{in}	–	–	10	μA
Input Chip Enable Current (V_{in} = 0 to V_{DD} + 1.0 V)	I_{ICE}	–	–	10	μA
Output High Voltage (I_O = -100 μA)	V_{OH}	2.4	–	V_{CC}	Vdc
Output Low Voltage (I_O = 2.0 mA)	V_{OL}	V_{SS}	–	0.45	Vdc
Output Leakage Current (V_O = 0.45 V to V_{CC}, CE = V_{CEL}, or $\overline{CS}$ = V_{IH})	I_{LO}	–	–	10	μA
Average Supply Current, Active Mode ($T_{cyc(W)}$ = min)	I_{DDA}	–	28	36	mA
	I_{CCA}	–	0.05	1.0	mA
	I_{BBA}	–	–	100	μA
Supply Current, Standby Mode (CE = 0.45 V)	I_{DDS}	–	1.0	20	μA
	I_{CCS}	–	–	10	μA
	I_{BBS}	–	1.0	20	μA

EFFECTIVE CAPACITANCE (Test Circuit of Figure 1, full operating voltage and temperature range, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Capacitance (A_n, D_{in}, R/W, $\overline{CS}$, Preset)	$C_{in(EFF)}$	–	4.0	5.0	pF
Chip Enable Capacitance	$C_{CE(EFF)}$	–	25	30	pF
Output Capacitance	$C_{out(EFF)}$	–	4.0	5.0	pF

FIGURE 1 – MEASUREMENT OF EFFECTIVE CAPACITANCE



Effective capacitance is determined by comparing the rise time of the voltage waveform at a particular pin to that measured with known values of capacitance. Scope calibration points are determined by using the rise times obtained with the empty socket and standard capacitor values as references.

The device under test (DUT) is inserted into the test socket and normal operating power supplies applied. All input pins, except that being measured, are grounded. The effective capacitance of the desired pin can then be read directly from the scope.

Pin	R	Input Pulse	Measurement Level
CE	67 Ω	16 V	12 V
Input/Output	100 Ω	6.0 V	4.0 V

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.)

OPERATING MODES

Mode	Control States		Output
	R/W	$\overline{CS}$	
Active (CE = High)			
Read Only	H	L	Valid
Read/Write	H → L	L	Valid
Write Only	L	L	Valid
Read Refresh	H → L	L → H	Valid → Floating
Refresh Only	L	H	Floating
Chip Disable (Unselected)	H	H	Floating
Standby (CE = Low)	X	X	Floating

X = Don't Care

RECOMMENDED AC OPERATING CONDITIONS (Read, Write, and Read Modify Write Cycles)

Parameter		Symbol	Min	Max	Unit
Address Setup Time		t_{AS}	0	–	ns
Address Hold Time		t_{AH}	60	–	ns
CE Pulse Transition Time		t_T	10	100	ns
CE Off Time	MCM6605AL,P/L2,P2	t_{SB}	120	–	ns
	MCM6605AL1,P1		90	–	
Chip Select Delay Time		t_{CSD}	–	70	ns
Chip Select Hold Time		t_{CSH}	0	–	ns
Read Write Delay Time		t_{RWD}	–	70	ns
Read Write Hold Time		t_{RWH}	0	–	ns
Time Between Refresh		t_{REF}	–	2.0	ms

AC CHARACTERISTICS

[All timing with t_T = 20 ns; Load = 1 TTL Gate (MC74H00 Series), C_L = 50 pF (effective)]

READ CYCLE (R/W = V_{IH}, $\overline{CS}$ = V_{IL})

Characteristic	Symbol	MCM6605AL,P		MCM6605AL1,P1		MCM6605AL2,P2		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	$t_{cyc(R)}$	470	–	290	–	360	–	ns
Chip Enable On Time	t_{CE}	310	2000	160	2000	200	2000	ns
Chip Enable to Output Delay	t_{CO}	–	280	–	130	–	180	ns
Read Access Time	t_{acc}	–	300	–	150	–	200	ns

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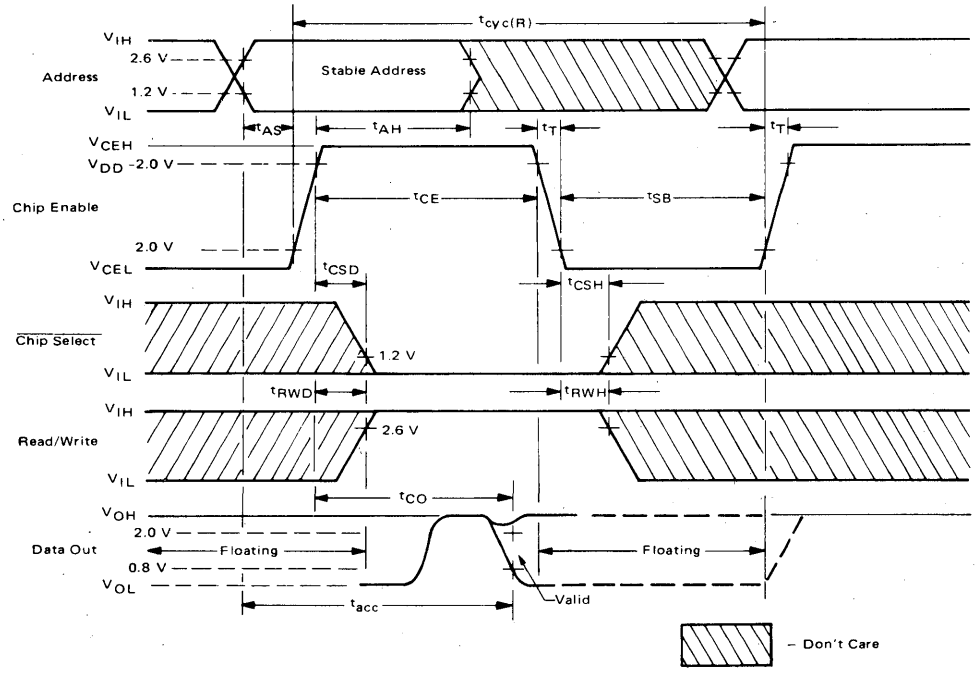
READ CYCLE TIMING

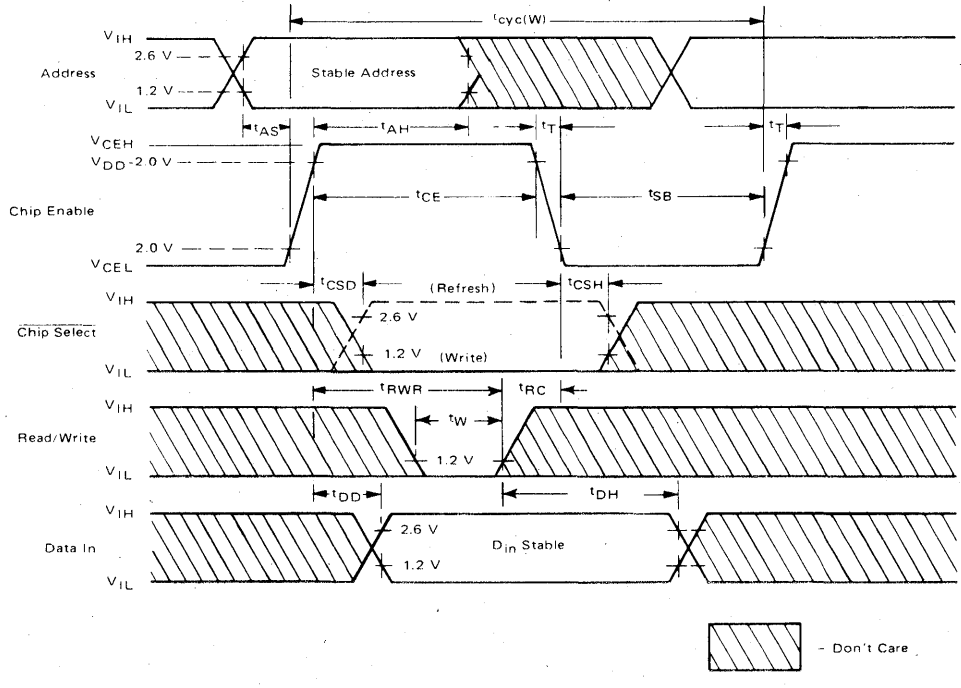


WRITE CYCLE ($R/\overline{W} = V_{IL}$, $\overline{CS} = V_{IL}$)
REFRESH CYCLE ($R/\overline{W} = V_{IL}$, $\overline{CS} = V_{IH}$)

Characteristic	Symbol	MCM6605AL,P		MCM6605AL1,P1		MCM6605AL2,P2		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	$t_{cyc(W)}$	590	–	390	–	490	–	ns
Chip Enable On Time	t_{CE}	430	2000	260	2000	330	2000	ns
Read-Write Release Time	t_{RWR}	410	2000	240	2000	310	2000	ns
Write Pulse Width	t_W	210	–	160	–	160	–	ns
Read-Write to Chip Enable Separation Time	t_{RC}	0	–	0	–	0	–	ns
Data Delay Time*	t_{DD}	–	70	–	70	–	70	ns
Data Hold Time	t_{DH}	50	–	20	–	50	–	ns

*If a write pulse (t_W) is employed on the R/W line during a write cycle, then the input data setup time is measured from the leading edge of the write pulse. The t_{DS} time is the same as that of the read-modify-write cycle.

WRITE AND REFRESH CYCLE TIMING

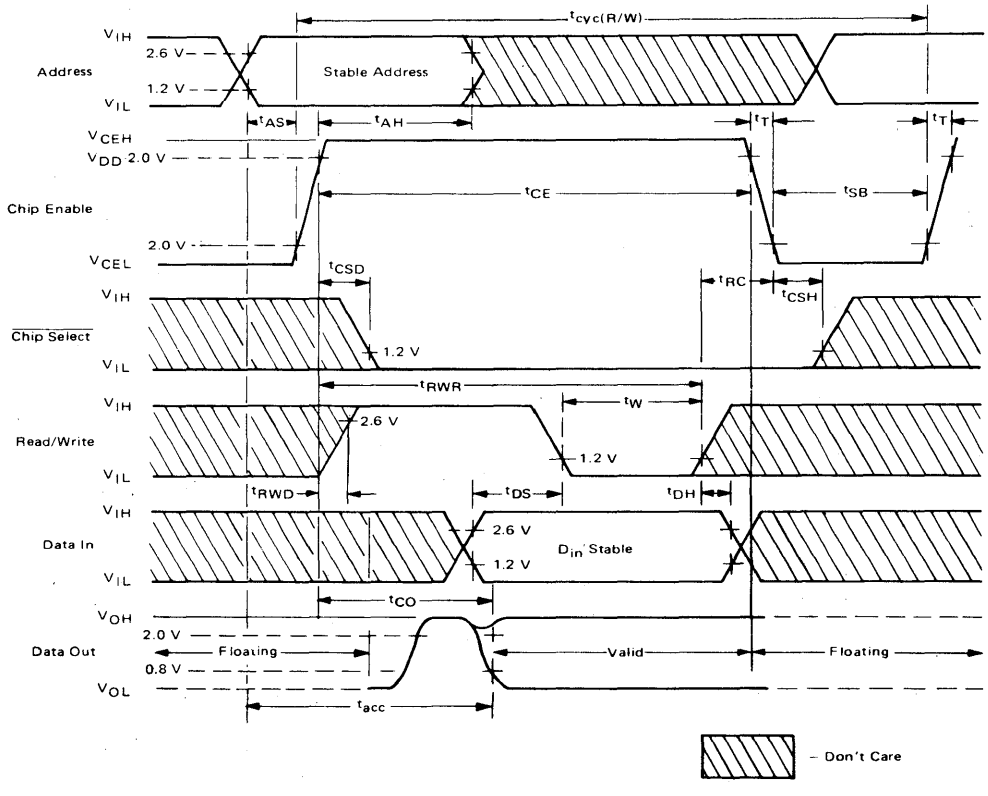


READ-MODIFY-WRITE (R/W = $V_{IH} \rightarrow V_{IL}$, $\overline{CS} = V_{IL}$)
READ REFRESH (See Note 1)

Characteristic	Symbol	MCM6605AL,P		MCM6605AL1,P1		MCM6605AL2,P2		Unit
		Min	Max	Min	Max	Min	Max	
Read-Modify-Write Cycle Time	$t_{cyc(R/W)}$	590	–	390	–	490	–	ns
Chip Enable On Time	t_{CE}	430	2000	260	2000	330	2000	ns
Read-Write Release Time	t_{RWR}	410	2000	240	2000	310	2000	ns
Write Pulse Width	t_W	210	–	160	–	160	–	ns
Data Setup Time	t_{DS}	0	–	0	–	0	–	ns
Data Hold Time	t_{DH}	50	–	20	–	50	–	ns
Read-Write to Chip Enable Separation Time	t_{RC}	0	–	0	–	0	–	ns
Chip Enable to Output Delay	t_{CO}	–	280	–	130	–	180	ns
Read Access Time	t_{acc}	–	300	–	150	–	200	ns

Note 1: A read refresh cycle is possible by bringing $\overline{CS}$ high after output data is valid and then bringing R/W low to the write position.

READ MODIFY WRITE TIMING



TYPICAL CHARACTERISTICS CURVES

FIGURE 2 – ACCESS TIME versus V_{DD}

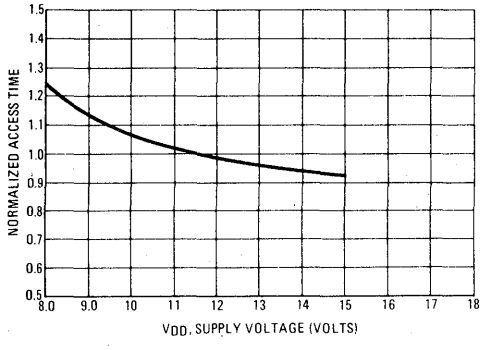


FIGURE 3 – ACCESS TIME versus AMBIENT TEMPERATURE

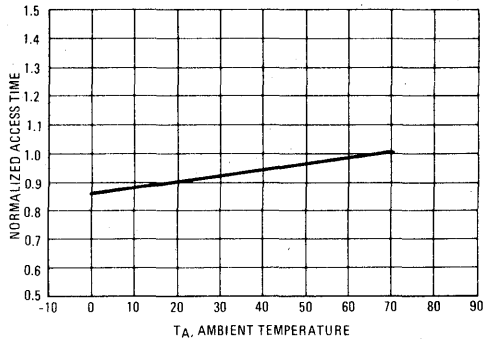


FIGURE 4 – I_{DD} SUPPLY CURRENT versus V_{DD}

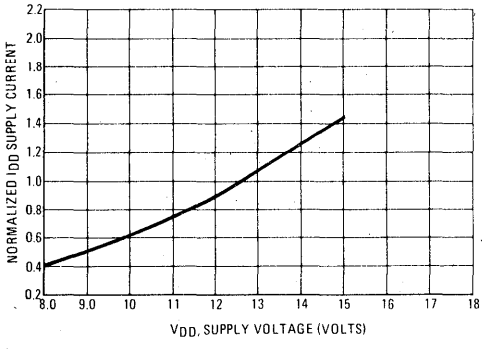


FIGURE 5 – I_{DD} SUPPLY CURRENT versus CYCLE TIME

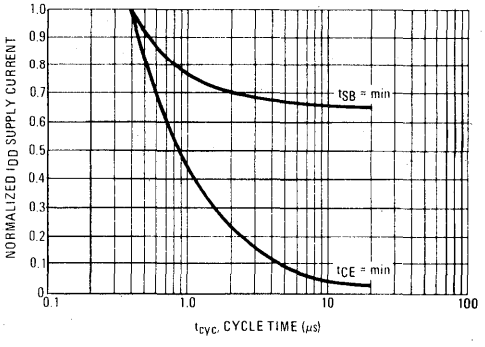


FIGURE 6 – I_{DD} SUPPLY CURRENT versus AMBIENT TEMPERATURE

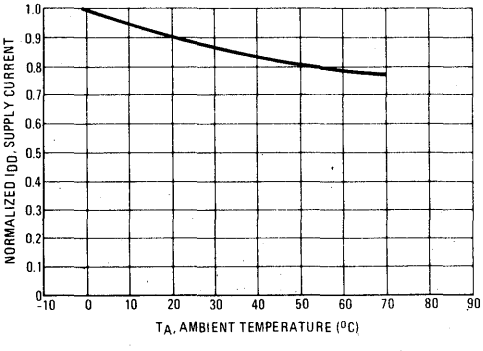
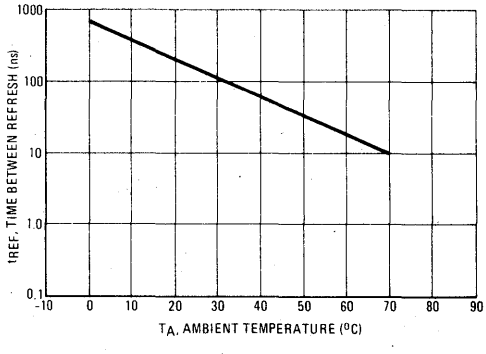


FIGURE 7 – REFRESH TIME versus AMBIENT TEMPERATURE



TYPICAL SUPPLY CURRENT TRANSIENT WAVEFORMS

FIGURE 8 – CHIP ENABLE VOLTAGE

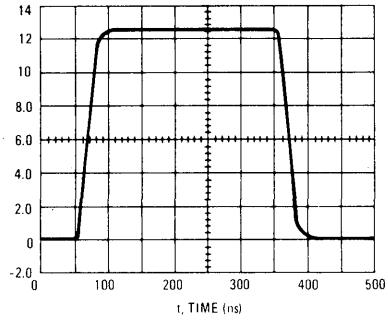


FIGURE 9 – i_{DD} SUPPLY CURRENT

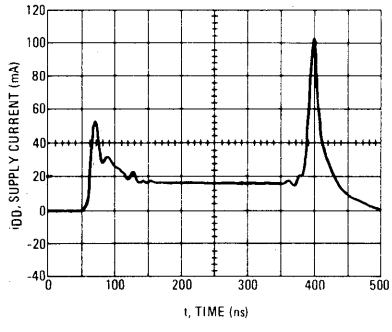


FIGURE 10 – i_{CC} SUPPLY CURRENT

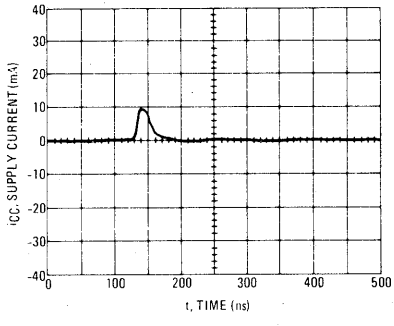


FIGURE 11 – i_{BB} SUPPLY CURRENT

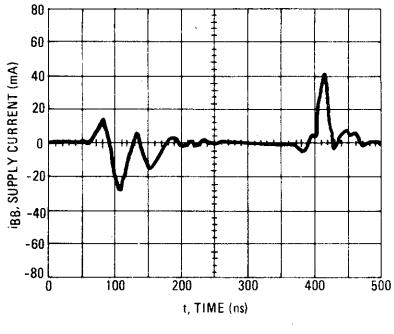
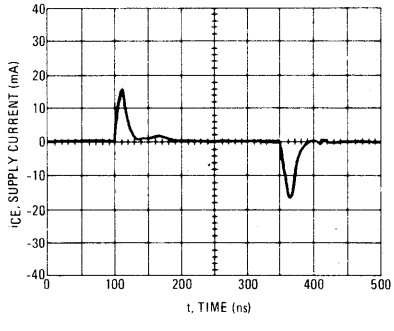
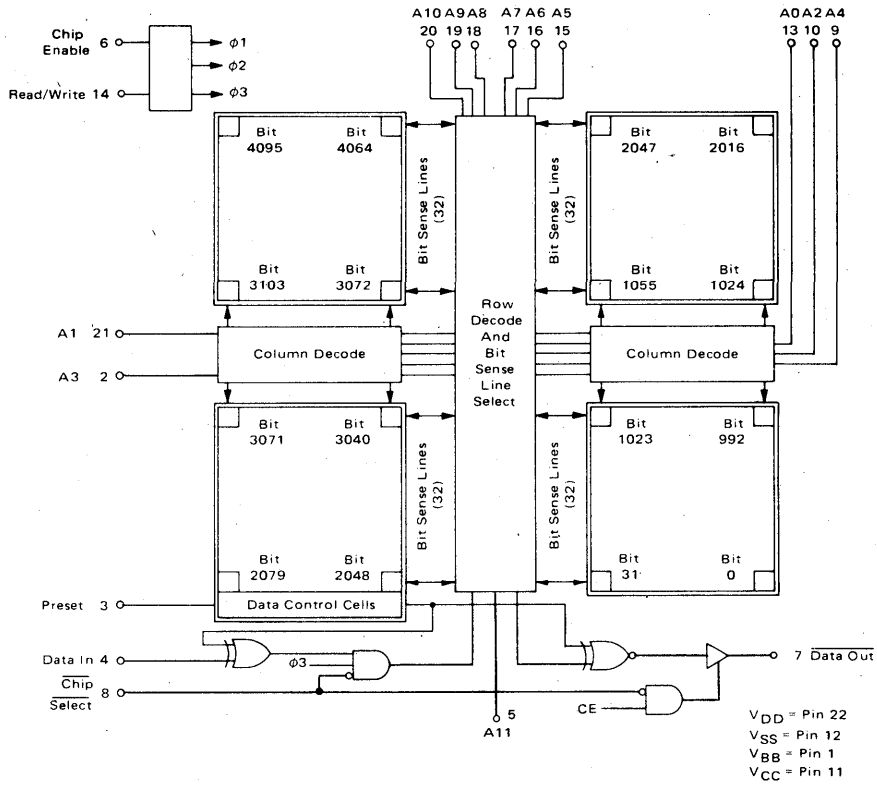


FIGURE 12 – i_{CE} SUPPLY CURRENT



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The MCM6605A 4096-bit dynamic RAM uses a three transistor storage cell in an inverting cell configuration. The single high-level clock (Chip Enable) starts an internal three-phase clock generator which controls the read and write functions of the device. The $\phi 1$ signal, which is high when CE is low (standby mode), preconditions the nodes in the dynamic RAM in preparation for a memory cycle. The $\phi 2$ signal, which comes on as CE goes high, is the read control and transfers data from storage onto bit sense lines. The $\phi 3$ signal, which comes after $\phi 2$ only during a write or refresh cycle, transfers data from the bit sense lines back into storage. The $\phi 3$ signal occurs only if the R/W input is low.

To perform a read cycle, CE is brought high to initiate a $\phi 2$ signal and latch the input addresses. The column decoders select one column in each of the four storage quadrants (see the block diagram) and transfers data from storage onto the 128 bit sense lines. The row decoder selects one of these 128 bit sense lines for read and write operations. During the $\phi 2$ signal, the data on this selected bit sense line is Exclusive ORed with the state of the appropriate data control cell to supply the correct output data. After this data is received by the external system, CE may be brought low to the standby position. This assumes that the R/W signal is held high to prevent an internal $\phi 3$ being generated.

To perform a write or refresh operation, CE is brought high and everything is identical to a read operation up until the 128 bit sense lines are charged with the selected columns of stored data. When R/W is brought low (if it is not already there), a $\phi 3$ signal is generated after $\phi 2$ is over. The $\phi 3$ signal takes the data from the 128 bit sense lines and returns it to the 128 storage locations it came from. Because of the design of the memory array, this $\phi 2$-$\phi 3$, read-write operation inverts the data. Therefore, one extra row of memory cells, called data control cells, is used to

keep track of the polarity of stored data in order to be able to correctly recover it. During the write operation, the input data is Exclusive ORed with these control cells before being stored in the array. A refresh cycle does not modify any of the bit sense lines, but simply returns the data (now inverted) into storage.

All timing signals for the MCM6605A are specified around these operations. The following is a brief description of the input pins and relevant timing requirements.

Chip Enable – CE is a single high level clock which initiates all memory cycles. CE can remain low as long as desired for specific applications as long as the 2.0 ms refresh requirements are met.

Chip Select – This signal controls only the I/O buffers. When $\overline{CS}$ is high, the input is disconnected and the output is in the 3-state high-impedance state. A refresh cycle is, therefore, a write cycle with $\overline{CS}$ high. $\overline{CS}$ has no critical timing with respect to any other signal except that there is a finite delay between activation and data out.

Read/Write – When high, R/W inhibits the internal $\phi 3$ signal, thereby keeping the memory from writing. When R/W is low, a $\phi 3$ will occur soon after $\phi 2$ is finished. For a read cycle, R/W should be high within t_{RWD} of CE to insure that a $\phi 3$ does not start. The only timing requirement on the R/W input for writing is a minimum write pulse defined as the overlap of $\overline{CS}$, CE, and R/W. Refresh cycles require that $\overline{CS}$ be high to inhibit the input buffer before a $\phi 3$ occurs. Thus $\overline{CS}$ should be high within t_{CSD} for a refresh cycle, or before R/W goes low for a read-refresh cycle.

Data In – The input data must be valid for a sufficient time to override the data stored on the selected bit sense line. It must remain valid for the "write pulse" defined under Read/Write. Signals on the D_{in} pin are ignored when either $\overline{CS}$ or R/W is high, or CE is low.

Data Out – Output data is inverted from input data and is valid t_{acc} after CE goes high. The data will remain valid as long as CE is high and $\overline{CS}$ remains low. With either CE low or $\overline{CS}$ high, the output is in a high-impedance state. The data output is initially precharged high when CE goes high and is then either discharged to ground or left high depending on the stored data. This precharging followed by valid data occurs regardless of the state of the R/W input, making the write cycle actually a read-write cycle. The output will also try to precharge during a refresh cycle but will be kept at high impedance by the $\overline{CS}$ being high. If $\overline{CS}$ is originally low and is then brought high (within the t_{CSD} specification) the output may start to precharge before being cut off and returned to high impedance.

Addresses – The addresses are latched when CE goes high, and may be removed after an appropriate hold time.

V_{SS} – Circuit ground.

V_{BB} – The reverse bias substrate supply. Forward biasing this supply with respect to V_{SS} will destroy the memory device.

V_{DD} – Positive supply voltage.

V_{CC} – Output buffer supply. This supply goes only to the data output buffer and draws current only when driving an output load high.

Preset – This pin should be tied to ground. During device testing Preset can be used to preset the data control cells to a logic zero. One 200 ns, 12 V pulse will set all 32 cells simultaneously. Preset has no system use; its only purpose is to ensure a good logic level in the control cells after first power up. In system use, this good logic level will come naturally after the first few refresh cycles.

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APPLICATIONS INFORMATION

Power Supplies

The MCM6605A is a dynamic RAM which has essentially zero power drain when in the standby (CE low) mode. When operating, the V_{DD} supply may experience transients in the order of 100 mA for a short time (Figure 9). The V_{BB} supply, which has very low dc drain while operating, may see transients of about 40 mA during the edges of CE. Therefore, appropriate bypassing of both supplies is recommended. This bypassing has been simplified by the location of the power supply pins on the corners of the package.

The V_{CC} line supplies only the input leakage of a TTL load on Data Out and should never exceed about 100 μA, presenting little bypassing requirement.

Power dissipation for a system of N chips is much lower than N times the 335 mW typical dissipation for a *full speed operating chip. This is because the unselected* rows in a memory array card are operating in the standby mode of near zero dissipation. This zero standby power is actually unachievable because of the requirements for refresh. Therefore, power dissipation for an array of N X M chips operating at t_1 cycle time, t_{REF} refresh increment, and maximum CE down time between cycles is:

$$P_D \approx M\left(\frac{490\ ns}{t_1\ ns}\right)335\ mW + (N-1)\ (M)\left(\frac{15.7}{t_{REF}\ \mu s}\right)335\ mW$$

For a 550-ns-cycle-time, 64 k by 16 system (16 by 16 chip array) with refresh at 2.0 ms, the approximate power dissipation is:

$$P_D \approx 16\left(\frac{490}{550}\right)335 + (15)\ (16)\left(\frac{15.7}{2000}\right)335$$

$$\approx 4775\ mW + 630\ mW = 5.4\ W$$

A similar one megabyte system, eight bytes wide, would have a dissipation of only 24 W. If the low standby power capability were not used, over 600 W would be dissipated.

Refresh

The MCM6605A is refreshed by performing a refresh (or write) cycle on each of the 32 combinations of the least significant address bits (A0-A4) within a 2.0 ms time period. (A5-A11 must remain constant at proper logic levels.) This refresh can be done in a burst mode (32 cycles starting every 2.0 ms) or in a distributed mode where one cycle is done every 62.5 μs.

A refresh abort can be accomplished by treating a refresh cycle as a read-modify-write cycle with $\overline{CS}$ high. This type of cycle can be aborted any time until the R/W signal has been brought low to allow a $\phi 3$ clock to begin.

Non-Volatile Storage

In many digital systems, it is extremely important to retain data during emergencies such as power failure. Unfortunately, however, most random access read/write semiconductor memories such as the MCM6605A are volatile. That is, if power is removed from the semiconductor memory, stored information is lost. Therefore, non-volatility for a specified period of time becomes highly desirable — as a necessity to maintain irreplaceable information or as a convenience to avoid the time consuming and troublesome task of having to reload the memory.

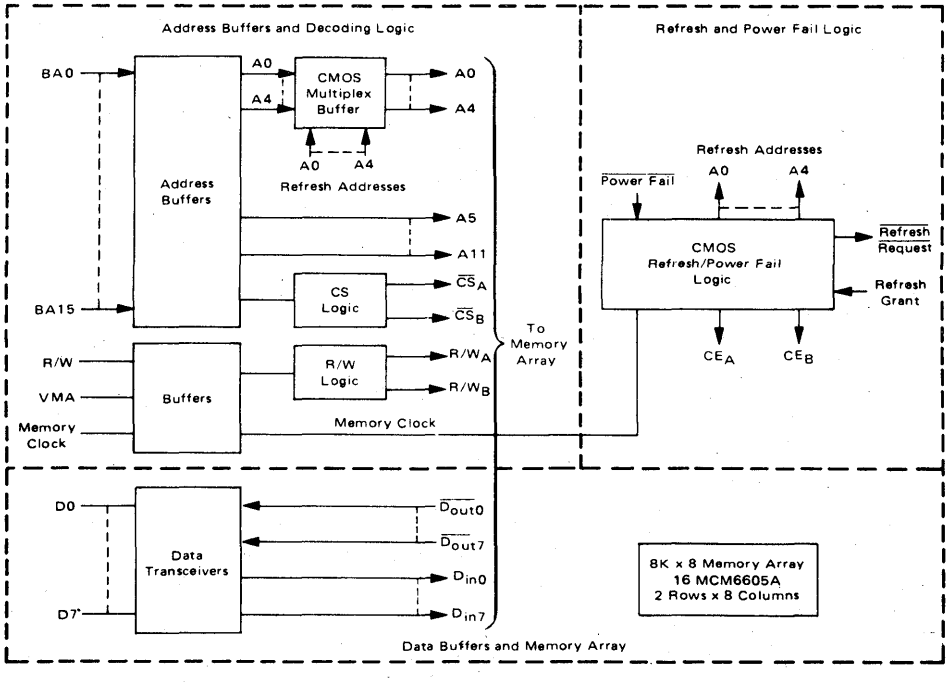
The extremely low standby power dissipation of the MCM6605A makes it ideal for main memory applications requiring battery backup for non-volatility. For example, the MCM6605A can be employed in an 8K byte non-volatile main memory system application for microprocessors. The memory system can be partitioned into three major sections as illustrated in Figure 13. The first section contains the address buffers and the Read/Write and Chip Select decoding logic. The second section consists of the data bus buffering transceivers and the memory array (which consists of 16 MCM6605As) organized into two rows of 4K bytes each.

The third section of the block diagram comprises refresh and control logic for the memory system. This logic interfaces the timing of the refresh handshaking with the microprocessor (MPU) clock circuitry. It handles requests for refresh, the generation of refresh addresses, the synchronization of a $\overline{\text{Power Fail}}$ signal, the multiplexing of the external Memory Clock with the internal clock (used during standby), and the generation of a -5 V supply on the board using a charge-pump method.

The refresh control logic is illustrated in Figure 14. It handles the refreshing of the memory during both operating and standby modes. The timing for this logic is given in Figure 15. Figure 16 gives the memory timing for the standby mode only. Decoding of the memory clock (CE_A and CE_B) and the circuitry to synchronize the $\overline{\text{Power Fail}}$ signal are shown in Figure 17, with the timing given in Figure 18.

The memory device clock (CE_A and CE_B) during standby is created by a monostable multivibrator (MC14528) and buffered from the memory array by three MC14503 buffers in parallel. This clock is multiplexed with the $\overline{\text{Memory Clock}}$ by use of the three-state feature of the

FIGURE 13 – NON-VOLATILE MEMORY SYSTEM BLOCK DIAGRAM



MC14503. The $\overline{\text{Memory Clock}}$ (used during normal operation) is translated to 12 V levels by use of an MC3460 Clock Driver. Decoding of the CE_A and CE_B signals (i.e., clocking only the memory bank addressed) to conserve power is accomplished by the logic within the MC3460.

Since the $\overline{\text{Power Fail}}$ signal will occur asynchronously with both the $\overline{\text{Memory Clock}}$ and the refreshing operation (Refresh Clock), it is necessary to synchronize the $\overline{\text{Power Fail}}$ signal to the rest of the system in order to avoid aborting a memory access cycle or a refresh cycle. An MC14027 dual flip-flop is used as the basic synchronization device. The leading edge of the Refresh Clock triggers a 3 μs monostable multivibrator which is used as a refresh pretrigger. The trailing edge of this pretrigger triggers a 500 ns monostable which creates the CE pulse during standby operation. The 3 μs pretrigger signal is used to set half of the MC14027 flip-flop, the output of which, (B), then inhibits a changeover from the standby to the operating modes (or vice versa). This logic prevents the system from aborting a refresh cycle should the $\overline{\text{Power Fail}}$ signal change states just prior to or during a refresh cycle. The trailing edge of the 500 ns monostable clears the MC14027 flip-flop, enabling the second flip-flop in the package. The state of $\overline{\text{Power Fail}}$ and Power Fail is applied to the K and J inputs of this second flip-flop and is synchronized by clocking with $\overline{\text{Memory Clock}}$. The outputs of this flip-flop, labeled Bat and $\overline{\text{Bat}}$, lock the system into the refresh mode and multiplex in the internal clock for standby operation when Bat = "1". The voltage to logic not required for the refresh only mode of operation is removed to conserve power.

By using CMOS for the refresh logic and capacitance drivers, and a low current refresh oscillator, the standby current required for the 8K byte system is extremely small, as noted in Table 1. This low standby current requirement can be easily supplied for several days with standard type +12 V batteries. For more detailed information on this sytem and a large mainframe memory system, see Application Notes AN-732 and AN-740.

2

FIGURE 14 – REFRESH CONTROL LOGIC

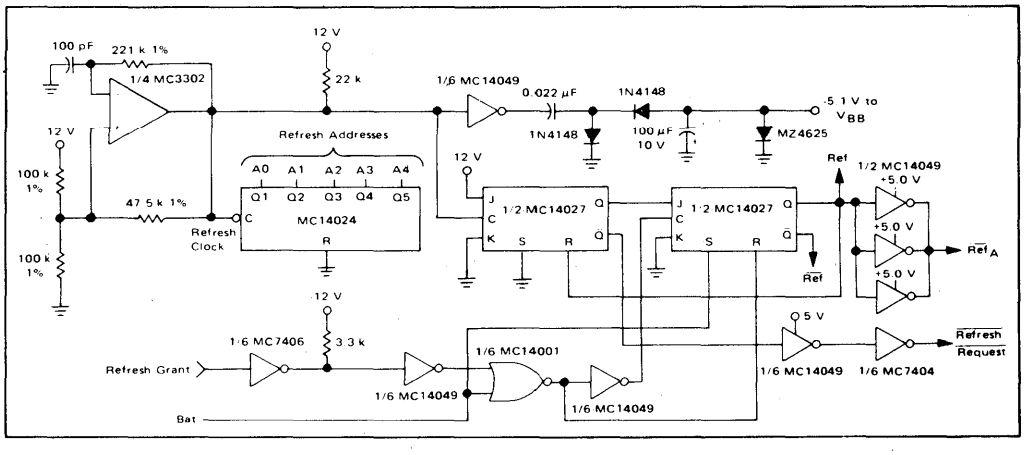


FIGURE 15 – REFRESH TIMING

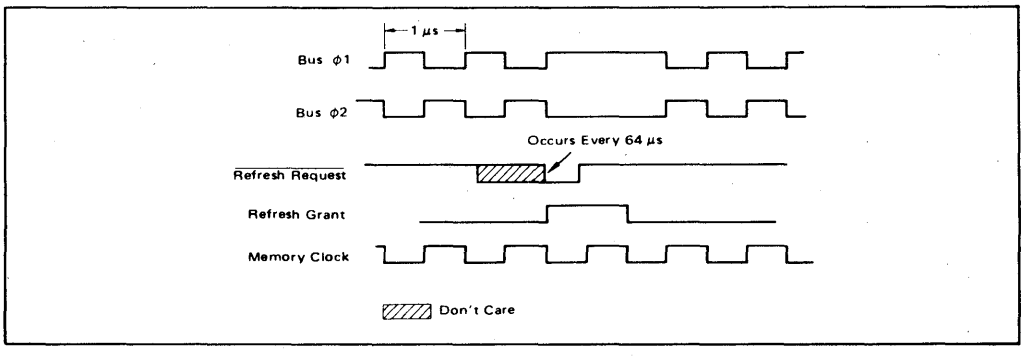


FIGURE 16 – MEMORY TIMING IN STANDBY MODE

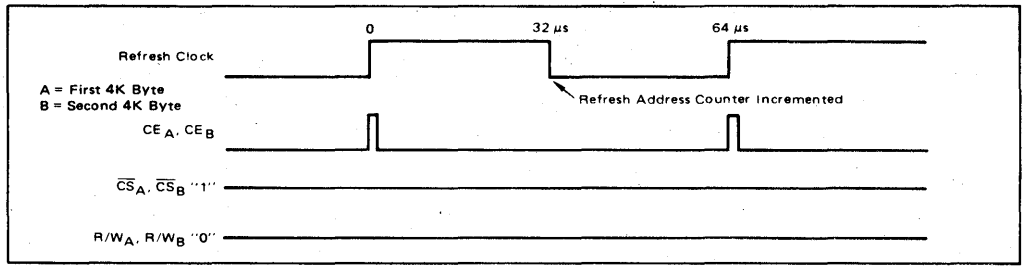


FIGURE 17 – POWER FAIL LOGIC AND CHIP ENABLE DRIVER

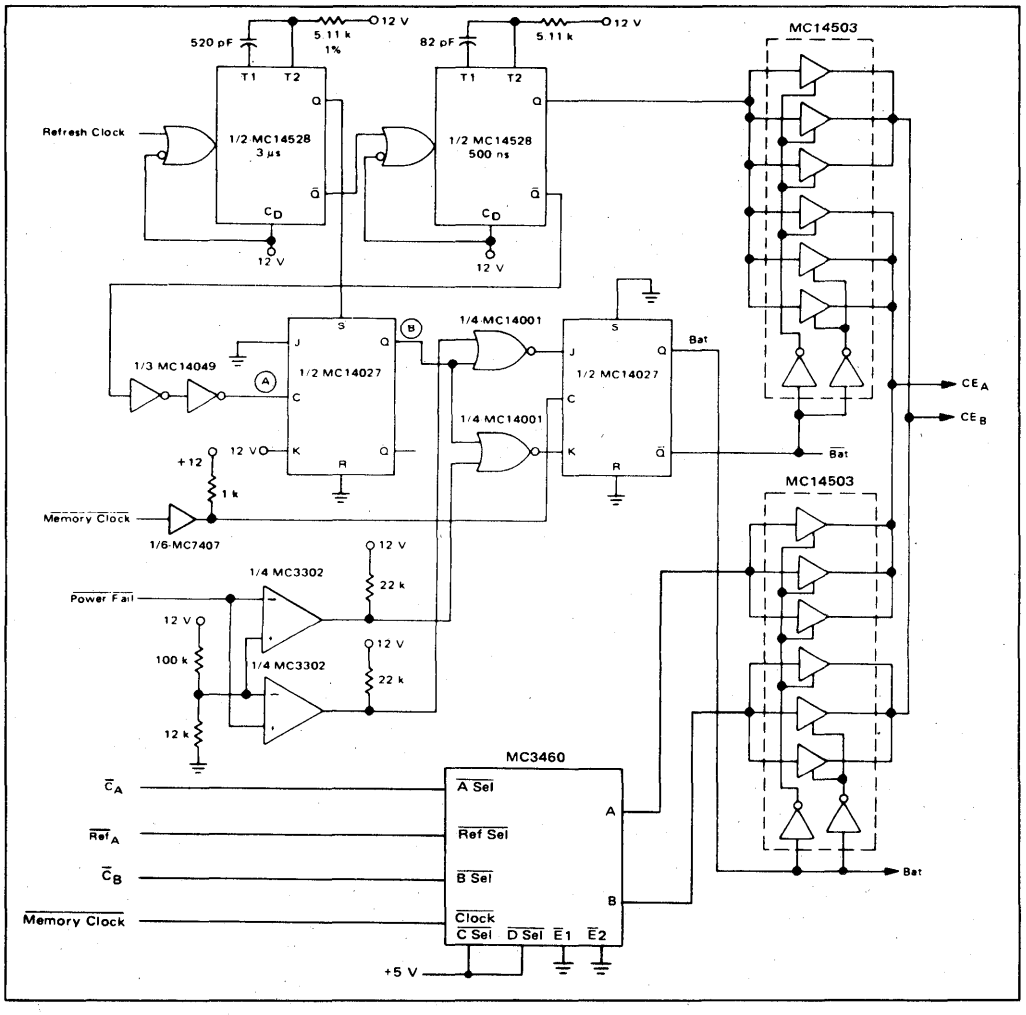


FIGURE 18 – POWER UP/DOWN SYNCHRONIZATION

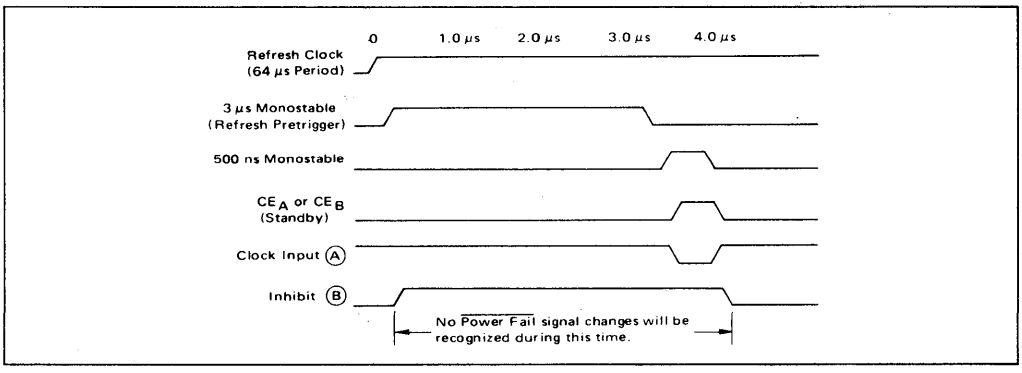


TABLE 1 – STANDBY MODE CURRENT ALLOCATION

Circuit Section	Typical Current
+12 V Current (V_{DD}) for 16 MCM6605A's	5 mA
Charge Pump	3 mA
Comparator	2 mA
Capacitance Drivers	4 mA
Total	14 mA

MOTOROLA

MCM6641
MCM66L41

MOS

(N-CHANNEL, SILICON-GATE)

4096-BIT STATIC
RANDOM ACCESS MEMORIES

2

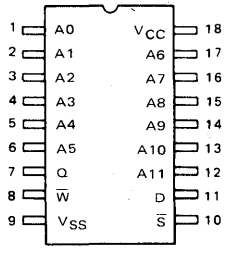
4096-BIT STATIC RANDOM ACCESS MEMORIES

The MCM6641 series 4096 × 1-bit random access memory is fabricated with high density, high reliability N-channel silicon-gate technology. For ease of use, the device operates from a single 5-volt power supply, is directly compatible with TTL and DTL, and requires no clocks or refreshing because of fully static operation. The fully static operation allows chip selects to be tied low further simplifying system timing. Data access is particularly simple, since address setup times are not required. The output data has the same polarity as the data input.

The MCM6641 is designed for memory applications where simple interfacing is the design objective, and is assembled in 18 pin dual in-line packages with the industry standard pin-outs.

- Single ±10% +5 V Supply
- Fully Static Operation—No Clock, Timing Strobe, Pre-Charge, or Refresh Required
- Industry Standard 18-Pin Configuration
- Fully TTL Compatible
- Common Data Input and Output Capability
- Three-State Outputs for OR-Tie Capability
- Power Dissipation MCM6641 Less Than 550 mW (Maximum)
  MCM66L41 Less Than 385 mW (Maximum)
- Standby Power Dissipation Less Than 125 mW (Typical)
- Plug-in Replacement for TMS4044

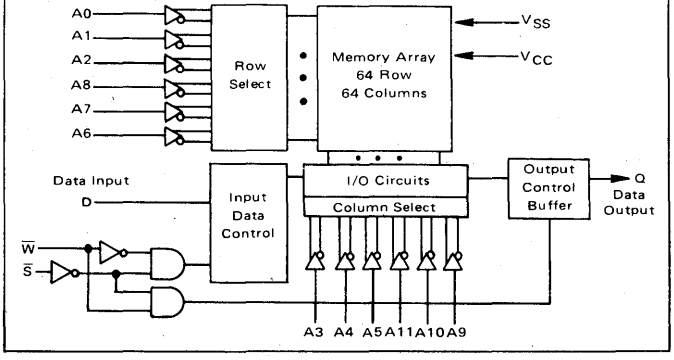
PIN ASSIGNMENT



MAXIMUM ACCESS TIME/MINIMUM CYCLE TIME

MCM6641-20 MCM66L41-20	200 ns	MCM6641-30 MCM66L41-30	300 ns
MCM6641-25 MCM66L41-25	250 ns	MCM6641-45 MCM66L41-45	450 ns

BLOCK DIAGRAM



PIN NAMES

A0–A11	Address Input
D	Data Input
Q	Data Output
S	Chip Select
VCC	Power Supply (+5 V)
VSS	Ground
W	Write Enable

TRUTH TABLE

S	W	D	Q	Mode
H	X	X	HI-Z	Not Selected
L	L	L	HI-Z	Write "0"
L	L	H	HI-Z	Write "1"
L	H	X	Output data	Read

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Value	Unit
Temperature Under Bias	-10 to +80	°C
Voltage on Any Pin With Respect to V_{SS}	-0.5 to +7.0	Vdc
DC Output Current	20	mA
Power Dissipation	1.0	Watt
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	-65 to +150	°C

Note: 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to +70°C)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	MCM6641			MCM66L41			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Load Current (All Input Pins, V_{in} = 0 to 5.5 V)	I_{LI}	–	–	10	–	–	10	μA
Output Leakage Current ($\overline{S}$ = 2.4 V, V_{in} = 0.4 to V_{CC})	$\|I_{LO}\|$	–	–	10	–	–	10	μA
Power Supply Current (V_{CC} = 5.5 V, I_{out} = 0 mA, T_A = 0°C)	I_{CC}	–	80	100	–	55	70	mA
Input Low Voltage	V_{IL}	-0.5	–	0.8	-0.5	–	0.8	V
Input High Voltage	V_{IH}	2.0	–	6.0	2.0	–	6.0	V
Output Low Voltage I_{OL} = 2.1 mA	V_{OL}	–	0.15	0.4	–	0.15	0.4	V
Output High Voltage I_{OH} = 1.0 mA	V_{OH}	2.4	–	–	2.4			V
Output Short Circuit Current	I_{OS}(2)	–	–	40	–	–	40	mA

Typical values are at V_{CC} = 5.0 V, T_A = 25°C

Note: 2. Duration not to exceed 30 seconds.

CAPACITANCE

(f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	5.0	pF
Output Capacitance (V_{out} = 0 V)	C_{out}	10	pF

STANDBY OPERATION

(Typical Supply Values)

Device	Supply	Operating	Standby	Max Standby Power
MCM6641	V_{CC}	+5 V	+2.4 V	225 mW
MCM66L41	V_{CC}	+5 V	+2.4 V	150 mW

The MCM6641 series is offered in an 18-pin dual-in-line ceramic (JL suffix) and plastic (NL suffix) packages designed for insertion in mounting-hole rows on 300-mil centers. The series is designed for operation from 0°C to 70°C.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.)

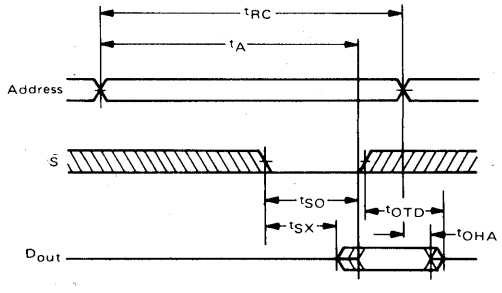
Input Pulse Levels . . . . . 0.8 Volt to 2.0 Volts
Input Rise and Fall Times . . . . . 10 ns
Input and Output Timing Levels . . . . . 1.5 Volts
Output Load . . . . . 1 TTL Gate and C_L = 100 pF

AC OPERATING CONDITIONS AND CHARACTERISTICS
Read (Note 3), Write (Note 4) Cycles

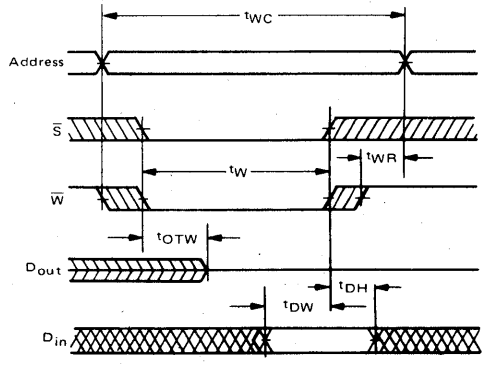
RECOMMENDED AC OPERATING CONDITIONS (T_A = 0 to 70°C, V_{CC} = 5.0 V ± 10%)

Parameter	Symbol	MCM6641-20 MCM66L41-20		MCM6641-25 MCM66L41-25		MCM6641-30 MCM66L41-30		MCM6641-45 MCM66L41-45		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	200	–	250	–	300	–	450	–	ns
Access Time	t_A	–	200	–	250	–	300	–	450	ns
Chip Selection to Output Valid	t_{SO}	–	70	–	85	–	100	–	120	ns
Chip Selection to Output Active	t_{SX}	10	–	10	–	10	–	10	–	ns
Output 3-State From Deselection	t_{OTD}	–	40	–	60	–	80	–	100	ns
Output Hold From Address Change	t_{OHA}	50	–	50	–	50	–	50	–	ns
Write Cycle Time	t_{WC}	200	–	250	–	300	–	450	–	ns
Write Time	t_W	100	–	125	–	150	–	200	–	ns
Write Release Time	t_{WR}	0	–	0	–	0	–	0	–	ns
Output 3-State From Write	t_{OTW}	–	40	–	60	–	80	–	100	ns
Data to Write Time Overlap	t_{DW}	100	–	125	–	150	–	200	–	ns
Data Hold From Write Time	t_{DH}	0	–	0	–	0	–	0	–	ns

READ CYCLE TIMING (Note 5)



WRITE CYCLE TIMING (Note 6)



Notes: 3. A Read occurs during the overlap of a low $\overline{S}$ and a high $\overline{W}$.
4. A Write occurs during the overlap of a low $\overline{S}$ and a low $\overline{W}$.
5. $\overline{W}$ is high for a Read cycle.
6. If the $\overline{S}$ low transition occurs simultaneously with the $\overline{W}$ low transition, the output buffers remain in a high impedance rate.

MOTOROLA

MCM6664

Product Preview

MOS
(N-CHANNEL, SILICON-GATE)
65,536-BIT DYNAMIC RAM

2

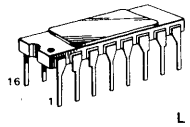
65,536-BIT DYNAMIC RAM

The MCM6664 is a 65,536 bit, high-speed, dynamic Random-Access Memory. Organized as 65,536 one-bit words and fabricated using HMOS high-performance N-channel silicon-gate technology. This new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

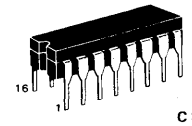
By multiplexing row- and column-address inputs, the MCM6664 requires only eight address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by $\overline{CAS}$ allowing for greater system flexibility.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM6664 incorporates a one-transistor cell design and dynamic storage techniques. In addition to the $\overline{RAS}$-only refresh mode, refresh control function available on pin 1 provides automatic and self-refresh modes.

- Organized as 65,536 Words of 1 Bit
- Single +5 V Operation
- Fast 150 ns Operation
- Low Power Dissipation
  250 mW Maximum (Active)
  30 mW Maximum (Standby)
- Three-State Data Output
- Internal Latches for Address and Data Input
- Early-Write Output Capability
- 16K Compatible 128-Cycle, 2 ms Refresh
- Control on Pin 1 for Automatic and Self Refresh
- $\overline{RAS}$-only Refresh Mode
- $\overline{CAS}$ Controlled Output Providing Latched or Unlatched Data
- Upward Pin Compatible from the 16K RAM (MCM4116)

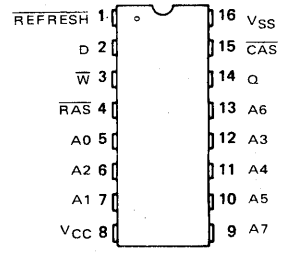


L SUFFIX
CERAMIC PACKAGE
CASE 690



C SUFFIX
FRIT-SEAL
CERAMIC PACKAGE
CASE 620

PIN ASSIGNMENT



OUTPUT BUFFER TRUTH TABLE

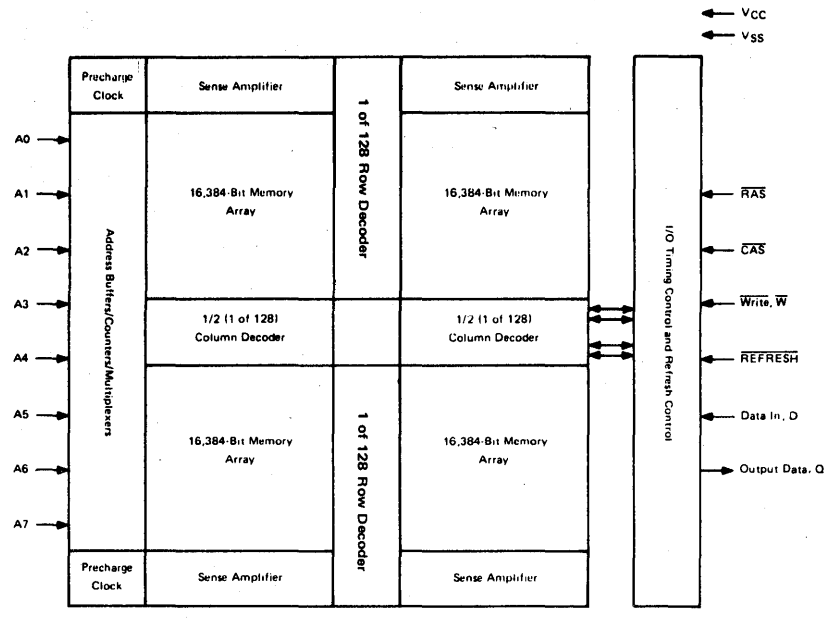
Internal Early Write	$\overline{CAS}$	Refresh Control (CAS Internal)		Output Buffer
H	X	X	(X)	Hi-Z
X	H	X	(X)	Hi-Z
L	L	L	(H)	Maintains Previous Data
L	L	H	(L)	Active

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

This is advance information and specifications are subject to change without notice.

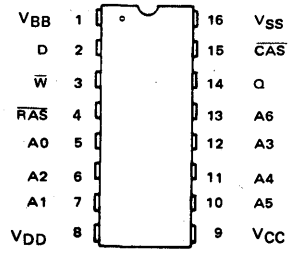
2

BLOCK DIAGRAM

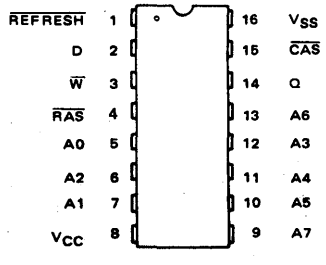


4116 TO 6664 COMPARISON

MCM4116



MCM6664



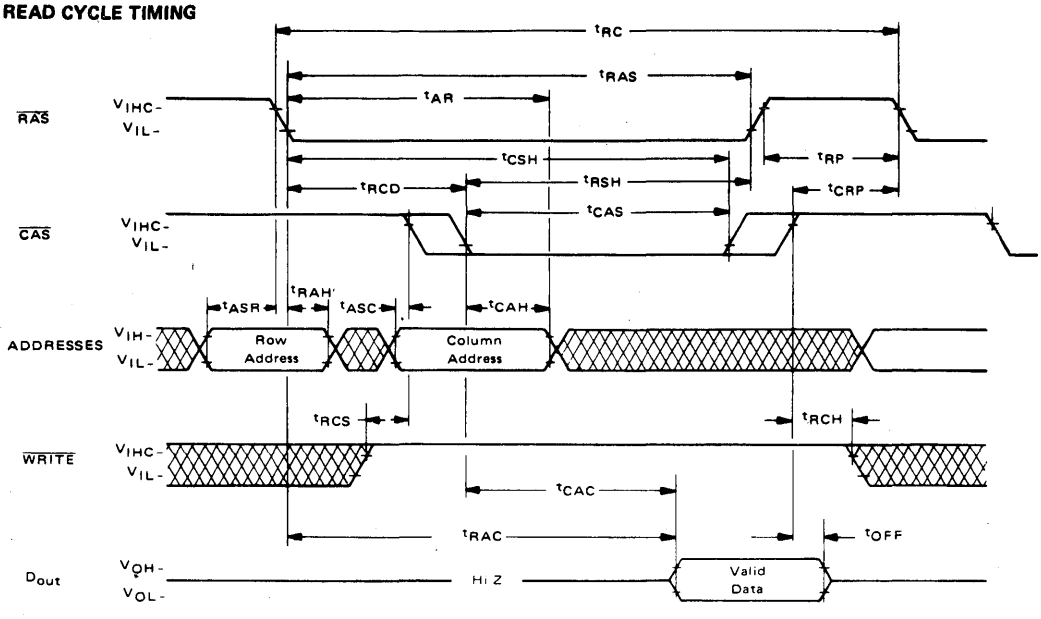
PIN VARIATIONS

PIN NUMBER	MCM4116	MCM6664
1	V_{BB} (–5 V)	$\overline{REFRESH}$
8	V_{DD} (+12 V)	V_{CC} (+5 V)
9	V_{CC} (+5 V)	A7

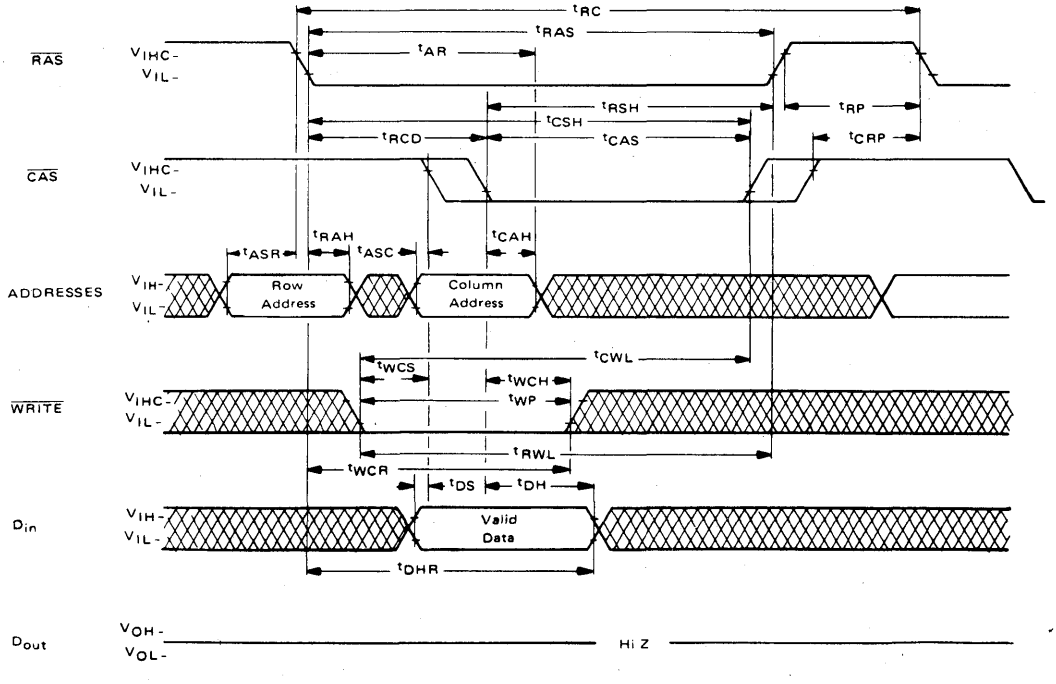
On-Chip Refresh Features/Benefits

- Reduce System Refresh Controller Design Problem
- Reduce System Parts Count
- Reduce System Noise Increasing System Reliability
- Reduce System Power During Refresh

READ CYCLE TIMING

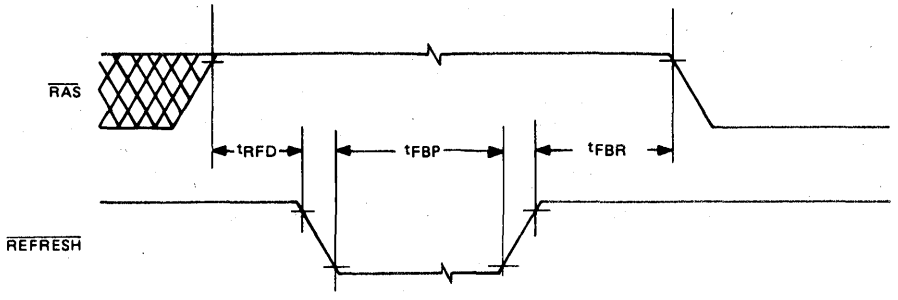


WRITE CYCLE TIMING

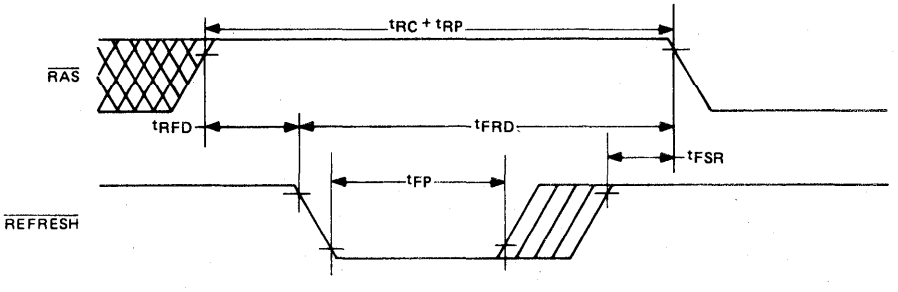


2

SELF REFRESH MODE (Battery Backup)
($\overline{CAS}$[1], Addresses, Data-In, and $\overline{Write}$ are Don't Care)

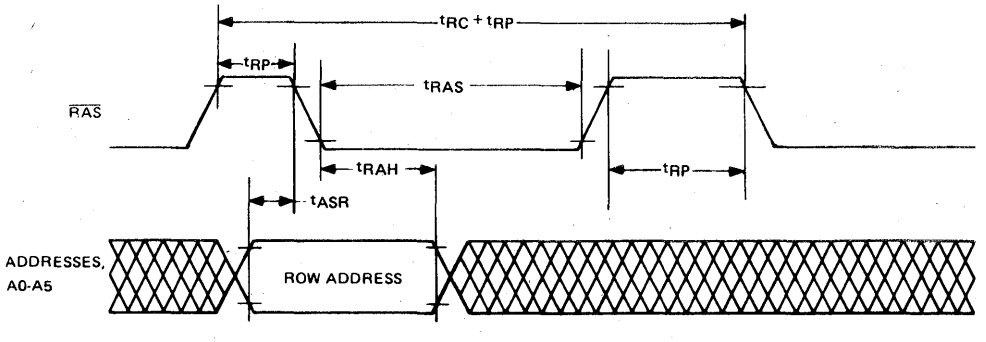


AUTOMATIC PULSE REFRESH CYCLE
($\overline{CAS}$[1], Addresses, Data-In, and $\overline{Write}$ are Don't Care)

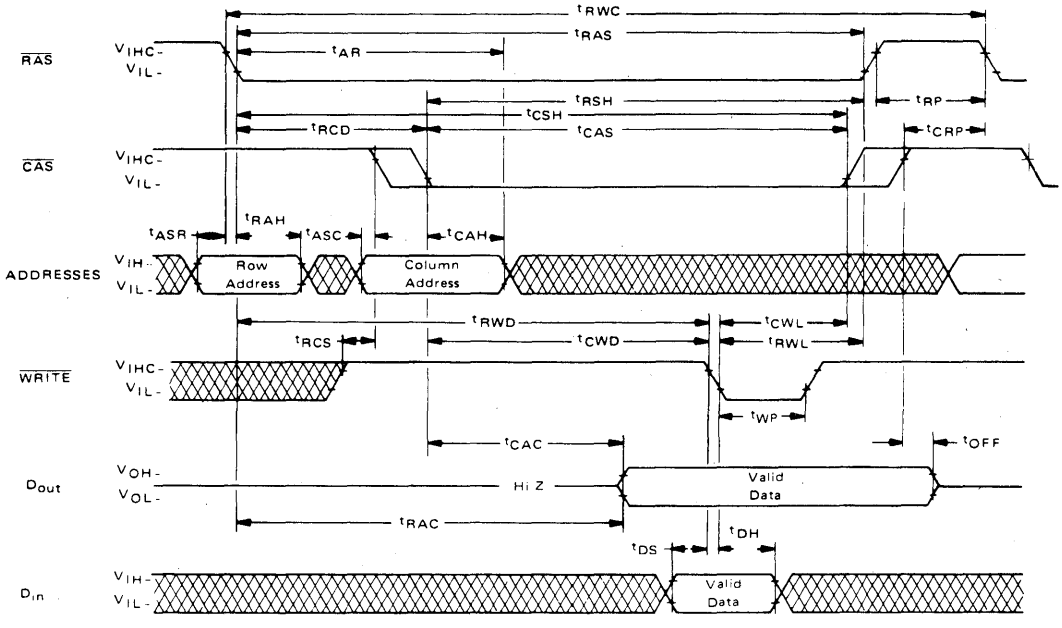


[1] $\overline{CAS}$ controls the output data. If $\overline{CAS}$ remains low the previous output will remain valid. When $\overline{CAS}$ is brought high, the output will assume a high-impedance state.

RAS-ONLY REFRESH CYCLE
(Data-in and $\overline{Write}$ are Don't Care, $\overline{CAS}$ is HIGH)



READ-WRITE/READ-MODIFY-WRITE CYCLE



MOTOROLA

MCM6810
1.0 MHz
MCM68A10
1.5 MHz
MCM68B10
2.0 MHz

MOS
(N-CHANNEL, SILICON-GATE)
128 X 8-BIT STATIC RANDOM ACCESS MEMORY

2

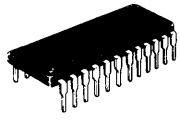
128 X 8-BIT STATIC RANDOM ACCESS MEMORY

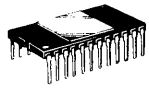
The MCM6810 is a byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of static operation.

The memory is compatible with the M6800 Microcomputer Family, providing random storage in byte increments. Memory expansion is provided through multiple Chip Select inputs.

- Organized as 128 Bytes of 8 Bits
- Static Operation
- Bidirectional Three-State Data Input/Output
- Six Chip Select Inputs (Four Active Low, Two Active High)
- Single 5-Volt Power Supply
- TTL Compatible
- Maximum Access Time = 450 ns — MCM6810
  360 ns — MCM68A10
  250 ns — MCM68B10

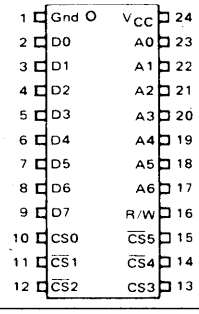
P SUFFIX
PLASTIC PACKAGE
CASE 709





L SUFFIX
CERAMIC PACKAGE
CASE 716

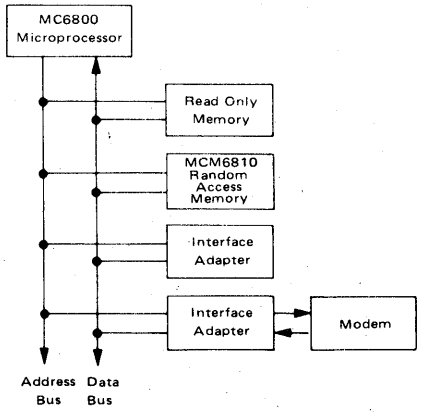
PIN ASSIGNMENT



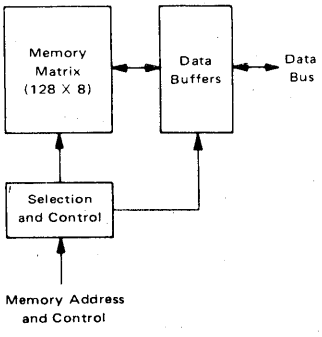
ORDERING INFORMATION

Speed	Device	Temperature Range
1.0 MHz	MC6810P, L	0 to 70°C
	MC6810CP, CL	-40 to +85°C
MIL-STD-883B	MC6810BJCS	-55 to +125°C
MIL-STD-883C	MC6810CJCS	
1.5 MHz	MC68A10P, L	0 to +70°C
	MC68A10CP, CL	-40 to +85°C
2.0 MHz	MC68B10P, L	0 to +70°C

M6800 MICROCOMPUTER FAMILY
BLOCK DIAGRAM



MCM6810 — RANDOM ACCESS MEMORY
BLOCK DIAGRAM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	T_L to T_H 0 to 70 -40 to 85 -55 to 125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Thermal Resistance	θ_{JA}	82.5	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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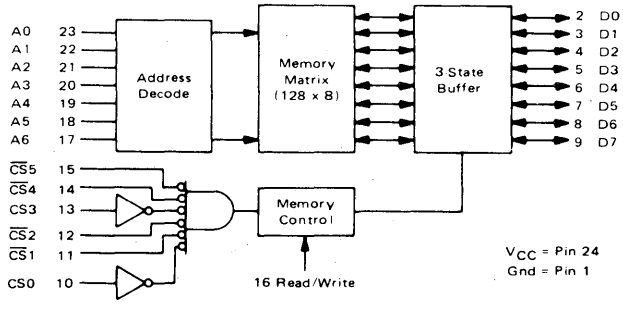
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = T_L to T_H unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Current (A_n, R/W, CS_n, $\overline{CS_n}$) (V_{in} = 0 to 5.25 V)		I_{in}	–	–	2.5	μAdc
Output High Voltage (I_{OH} = -205 μA)		V_{OH}	2.4	–	–	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)		V_{OL}	–	–	0.4	Vdc
Output Leakage Current (Three-State) (CS = 0.8 V or $\overline{CS}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)		I_{TSI}	–	–	10	μAdc
Supply Current (V_{CC} = 5.25 V, all other pins grounded)	1.0 MHz 1.5, 2.0 MHz	I_{CC}	–	–	80 100	mAdc
Input Capacitance (A_n, R/$\overline{W}$, CS_n, $\overline{CS_n}$) (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)		C_{in}	–	–	7.5	pF
Output Capacitance (D_n) (V_{out} = 0, T_A = 25°C, f = 1.0 MHz, CSØ = 0)		C_{out}	–	–	12.5	pF

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Input High Voltage	V_{IH}	2.0	–	5.25	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.8	Vdc

BLOCK DIAGRAM



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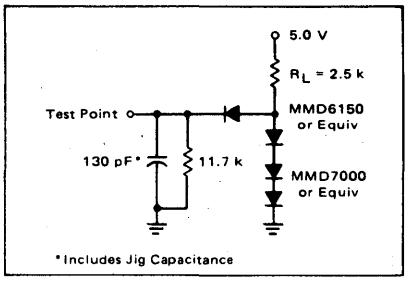
AC TEST CONDITIONS

Condition	Value
Input Pulse Levels	0.8 V to 2.0 V
Input Rise and Fall Times	20 ns
Output Load	See Figure 1

FIGURE 1 – AC TEST LOAD

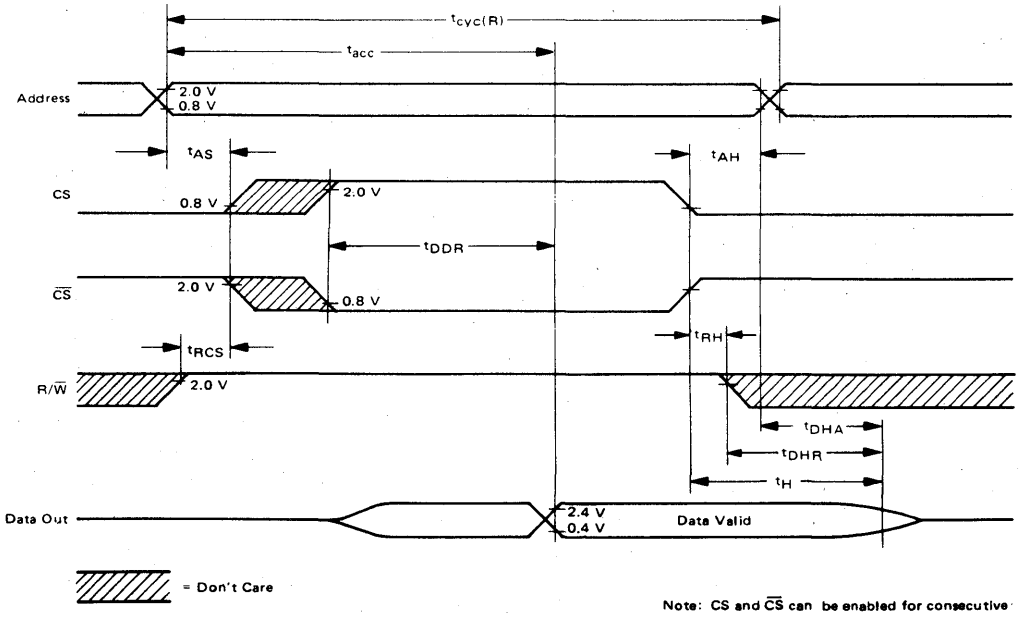


AC OPERATING CONDITIONS AND CHARACTERISTICS

READ CYCLE (V_{CC} = 5.0 V ± 5%, V_{SS} = 0, T_A = T_L to T_H unless otherwise noted.)

Characteristic	Symbol	MCM6810		MCM68A10		MCM68B10		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	$t_{cyc(R)}$	450	–	360	–	250	–	ns
Access Time	t_{acc}	–	450	–	360	–	250	ns
Address Setup Time	t_{AS}	20	–	20	–	20	–	ns
Address Hold Time	t_{AH}	0	–	0	–	0	–	ns
Data Delay Time (Read)	t_{DDR}	–	230	–	220	–	180	ns
Read to Select Delay Time	t_{RCS}	0	–	0	–	0	–	ns
Data Hold from Address	t_{DHA}	10	–	10	–	10	–	ns
Output Hold Time	t_H	10	–	10	–	10	–	ns
Data Hold from Read	t_{DHR}	10	80	10	60	10	60	ns
Read Hold from Chip Select	t_{RH}	0	–	0	–	0	–	ns

READ CYCLE TIMING

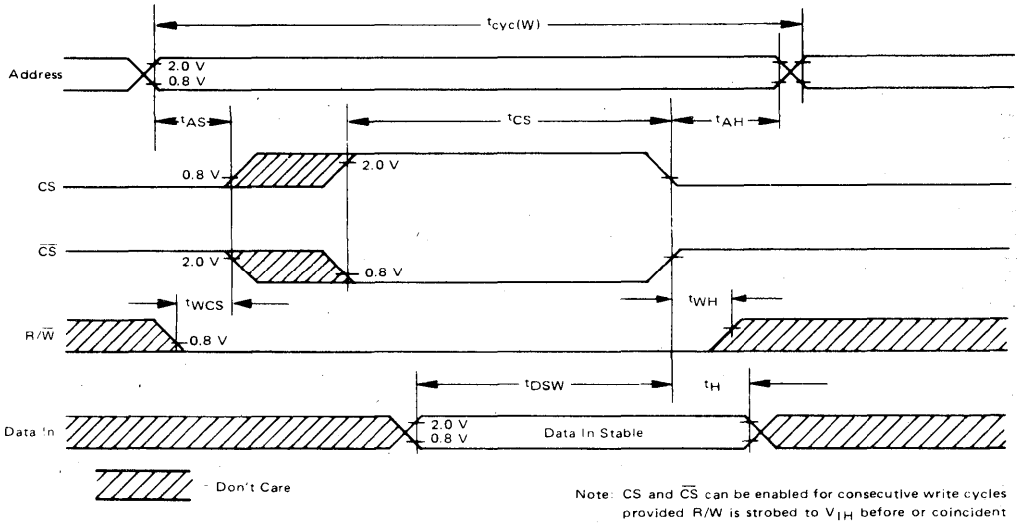


Note: CS and $\overline{CS}$ can be enabled for consecutive read cycles provided R/W remains at V_{IH}.

WRITE CYCLE (V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = T_L to T_H unless otherwise noted.)

Characteristic	Symbol	MCM6810		MCM68A10		MCM68B10		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	$t_{cyc(W)}$	450	–	360	–	250	–	ns
Address Setup Time	t_{AS}	20	–	20	–	20	–	ns
Address Hold Time	t_{AH}	0	–	0	–	0	–	ns
Chip Select Pulse Width	t_{CS}	300	–	250	–	210	–	ns
Write to Chip Select Delay Time	t_{WCS}	0	–	0	–	0	–	ns
Data Setup Time (Write)	t_{DSW}	190	–	80	–	60	–	ns
Input Hold Time	t_H	10	–	10	–	10	–	ns
Write Hold Time from Chip Select	t_{WH}	0	–					

WRITE CYCLE TIMING



Note: CS and $\overline{CS}$ can be enabled for consecutive write cycles provided R/W is strobed to V_{IH} before or coincident with the Address change, and remains high for time t_{AS}.

MOTOROLA

MCM2532
MCM25A32

Advance Information

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4096 X 8-BIT UV ERASABLE PROM

The MCM2532/25A32 is a 32,768-bit Erasable and Electrically Reprogrammable PROM designed for system debug usage and similar applications requiring nonvolatile memory that could be reprogrammed periodically. The transparent window in the package allows the memory content to be erased with ultraviolet light.

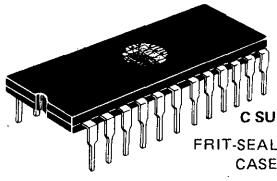
For ease of use, the device operates from a single power supply and has a static power-down mode. Pin-for-pin mask programmable ROMs are available for large volume production runs of systems initially using the MCM2532.

- Single +5 V Power Supply
- Organized as 4096 Bytes of 8 Bits
- Automatic Power-Down Mode (Standby)
- Fully Static Operation (No Clocks)
- TTL Compatible During both Read and Program
- Maximum Access Time = 450 ns MCM 2532
  350 ns MCM25A32
- Pin Compatible with MCM68A332 Mask Programmable ROMs

MOS

(N-CHANNEL, SILICON-GATE)

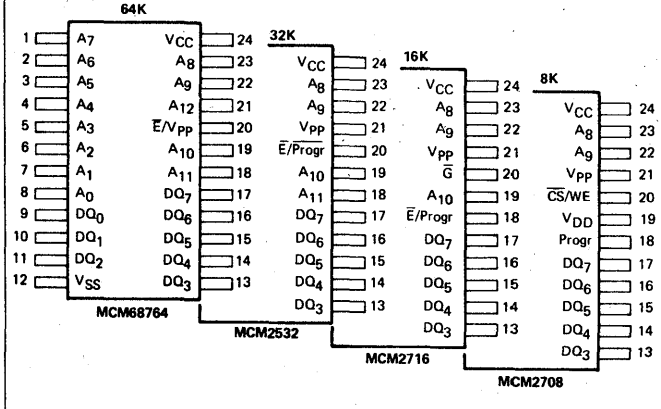
4096 X 8-BIT
UV ERASABLE PROM



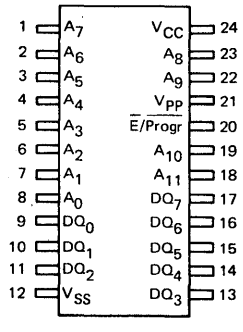
C SUFFIX
FRIT-SEAL PACKAGE
CASE 623A

L SUFFIX SIDEBRAZE CERAMIC PACKAGE
ALSO AVAILABLE — CASE 716

MOTOROLA'S PIN COMPATIBLE EPROM FAMILY
(INDUSTRY STANDARD PINOUTS)



PIN ASSIGNMENT



*PIN NAMES	
A	Address
DQ	Data Input/Output
$\overline{E}$/Progr	Dual Function $\overline{\text{Enable}}$ (Power-down/$\overline{\text{Program}}$ Pulse)
V_{CC}	+5 V Supply
V_{PP}	+25 V Program Voltage
V_{SS}	Ground

*New Industry standard nomenclature

This is advance information and specifications are subject to change without notice.

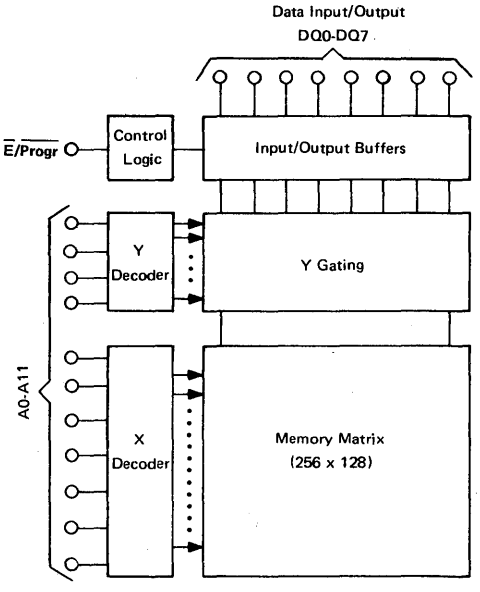
Mode	PIN NUMBER				
	9-11, 13-17 DQ	12 V_{SS}	20 $\overline{E}/\overline{Progr}$	21 V_{PP}	24 V_{CC}
Read	Data out	V_{SS}	V_{IL}	0 to 5 V	V_{CC}
Output Disable	Hi-Z	V_{SS}	V_{IH}	0 to 25 V	V_{CC}
Standby	Hi-Z	V_{SS}	V_{IH}	0 to 5 V	V_{CC}
Program	Data in	V_{SS}	Pulsed V_{IH} to V_{IL}	V_{PPH}	V_{CC}
Program Verify	Data out	V_{SS}	V_{IL}	0 to 5 V	V_{CC}
Program Inhibit	Hi-Z	V_{SS}	V_{IH}	V_{PPH}	V_{CC}

ABSOLUTE MAXIMUM RATINGS (1)

Rating	Value	Unit
Temperature Under Bias	−10 to +80	°C
Storage Temperature	−65 to +125	°C
All Input/Output Voltages with Respect to V_{SS}	+6 to −0.3	Vdc
V_{PP} Supply Voltage with Respect to V_{SS}	+28 to −0.3	Vdc

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

BLOCK DIAGRAM



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DC OPERATING CONDITIONS AND CHARACTERISTICS

(Fully operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC READ OPERATING CONDITIONS (T_A = 0° to +70°C)

Parameter		Symbol	Min	Nom	Max	Unit
Supply Voltage*	MCM2732	V_{CC}	4.75	5.0	5.25	Vdc
	MCM27A32		4.5	5.0	5.5	Vdc
		V_{PP}	0	5.0	V_{CC} +0.6	Vdc
Input High Voltage		V_{IH}	2.2	–	V_{CC} +1.0	Vdc
Input Low Voltage		V_{IL}	−0.1	–	0.65	Vdc

READ OPERATION DC CHARACTERISTICS

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address and $\overline{E}$ Input Sink Current	V_{in} = 5.25 V	I_{in}	–	–	10	μA
Output Leakage Current	V_{out} = 5.25 V	I_{LO}	–	–	10	μA
V_{CC} Supply Current* (Standby)	$\overline{E} = V_{IH}$	I_{CC1}	–	10	25	mA
V_{CC} Supply Current* (Active)	$\overline{E} = V_{IL}$	I_{CC2}	–	50	160	mA
V_{PP} Supply Current*	V_{PP} = 5.85 V	I_{PP1}	–	–	400	μA
	V_{PP} = 0 V		–	–	0	μA
Output Low Voltage	I_{OL} = 2.1 mA	V_{OL}	–	–	0.45	V
Output High Voltage	I_{OH} = −400 μA	V_{OH}	2.4	–	–	V

*V_{CC} must be applied simultaneously or prior to V_{PP}. V_{CC} must also be switched off simultaneously with or after V_{PP}. With V_{PP} connected directly to V_{CC} during the read operation, the supply current would be the sum of I_{PP1} and I_{CC}. The additional 0.6 V tolerance on V_{PP} makes it possible to use a driver circuit for switching the V_{PP} supply from V_{CC} in Read mode to +25 V for programming. Typical values are for T_A = 25°C and nominal supply voltages.

CAPACITANCE

(f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	4.0	6.0	pF
Output Capacitance (V_{out} = 0 V)	C_{out}	8.0	12	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = IΔt/ΔV.

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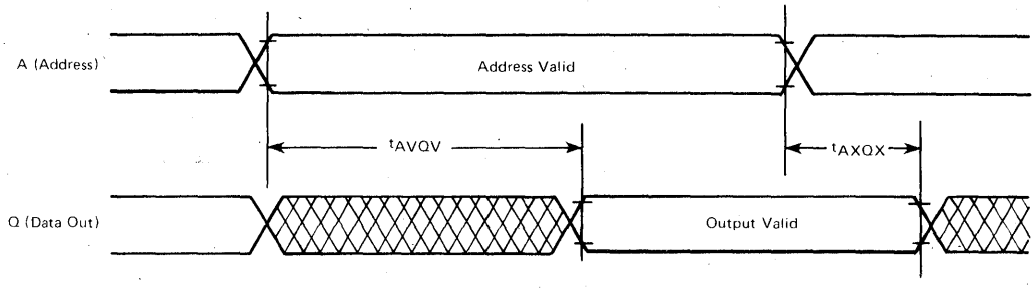
AC READ OPERATING CONDITIONS AND CHARACTERISTICS

(T_A = 0 to +70°C, V_{CC} and V_{PP} = 5.0 V (± 10% MCM25A32, ±5% MCM2532) unless otherwise noted)

Input Pulse Levels . . . . . 0.65 Volt to 2.2 Volts
Input Rise and Fall Times . . . . . 20 ns
Input and Output Timing Levels . . . . . 0.8/2.0 Volts
Output Load . . . . . 1 TTL Gate and C_L = 100 pF

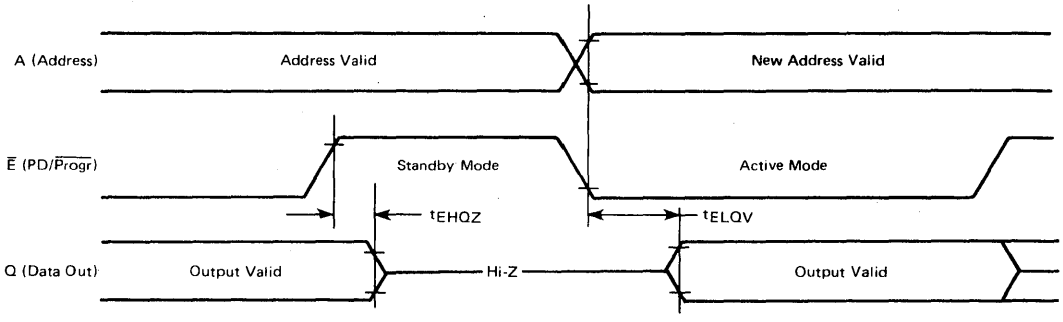
Characteristic	Symbol	MCM27A32		MCM2732		Unit
		Min	Max	Min	Max	
Address Valid to Output Valid ($\overline{E}$/$\overline{Progr}$ = V_{IL})	t_{AVQV}	–	350	–	450	ns
$\overline{E}$ to Output Valid	t_{ELQV}	–	350	–	450	ns
$\overline{E}$ to Hi-Z Output	t_{EHQZ}	0	100	0	100	ns
Data Hold from Address ($\overline{E}$ = V_{IL})	t_{AXQX}	0		0		ns

READ MODE TIMING DIAGRAMS ($\overline{E}$ = V_{IL})



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

STANDBY MODE



DC PROGRAMMING CONDITIONS AND CHARACTERISTICS

(T_A = 0 to +70°C)

RECOMMENDED PROGRAMMING OPERATION CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}, V_{PPL}	4.75	5.0	5.25	Vdc
	V_{PPH}	24	25	26	Vdc
Input High Voltage for Data	V_{IH}	2.2	–	V_{CC} +1	Vdc
Input Low Voltage for Data	V_{IL}	–0.1	–	0.65	Vdc

*V_{CC} must be applied simultaneously or prior to V_{PP}. V_{CC} must also be switched off simultaneously with or after V_{PP}. The device must not be inserted into or removed from a board with V_{PP} at +25 V. V_{PP} must not exceed the +26 V maximum specifications.

PROGRAMMING OPERATION DC CHARACTERISTICS

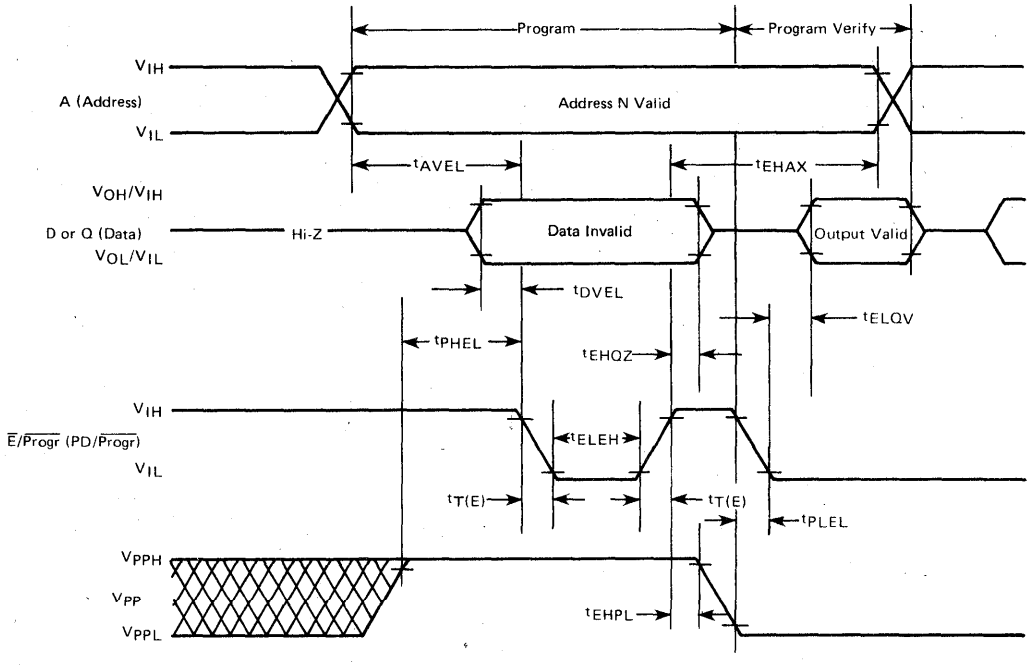
Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address and Ē/Progr Input Sink Current	V_{in} = 5.25V/0.45 V	I_{LI}	–	–	10	μAdc
V_{PP} Supply Current	Ē/Progr = V_{IL}	I_{PP1}	–	–	400	μAdc
V_{PP} Programming Pulse Supply Current	Ē/Progr = V_{IH}	I_{PP2}	–	–	30	mAdc
V_{CC} Supply Current		I_{CC}	–	–	160	mAdc

AC PROGRAMMING OPERATING CONDITIONS AND CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Address Setup Time	t_{AVEL}	2.0	–	μs
V_{PP} Setup Time	t_{PHEL}	0	–	ns
Data Setup Time	t_{DVEL}	2.0	–	μs
Address Hold Time	t_{EHAX}	2.0	–	μs
V_{PP} to Enable Low Time	t_{PLEL}	0	–	ns
Data Hold Time	t_{EHQZ}	2.0	–	μs
V_{PP} Hold Time	t_{EHPL}	0	–	ns
Enable (Program) Active Time	t_{ELEH}	1*	55	ms
Enable (Ē/Progr) Pulse Transition Time	$t_{T(PE)}$	5	–	ns
V_{PP} Rise and Fall Time from 5 to 25 V	t_R, t_F	0.5	2	μs

*If shorter than 45 ms (min) pulses are used, the same number of pulses should be applied after the specific data has been verified.

PROGRAMMING OPERATION TIMING DIAGRAM



PROGRAMMING INSTRUCTIONS

After the completion of an ERASE operation, every bit in the device is in the "1" state (represented by Output High). Data are entered by programming zeros (Output Low) into the required bits. The words are addressed the same way as in the READ operation. A programmed "0" can only be changed to a "1" by ultraviolet light erasure.

To set the memory up for PROGRAM mode, the V_{PP} input (pin 21) should be raised to +25 V. The V_{CC} supply voltage is the same as for the READ operation. Programming data is entered in 8-bit words through the data out (DQ) terminals while $\overline{E}/\overline{Progr}$ is high. Only "0's" will be programmed when "0's" and "1's" are entered in the data word.

After address and data setup, a 50 ms program pulse (V_{IH} to V_{IL}) is applied to the $\overline{E}/\overline{Progr}$ input. A program pulse is applied to each address location to be programmed. Locations may be programmed individually, sequentially, or at random. The maximum program pulse width is 55 ms; therefore, programming must not be attempted with a dc signal applied to the $\overline{E}/\overline{Progr}$ input.

Multiple MCM2532s may be programmed in parallel with the same data by connecting together like inputs and applying the program pulse to the $\overline{E}/\overline{Progr}$ inputs. Different data may be programmed into multiple MCM2532s connected in parallel by using the PROGRAM INHIBIT mode. Except for the $\overline{E}/\overline{Progr}$ pin, all like inputs may be common.

PROGRAM VERIFY for the MCM2532 is the read operation.

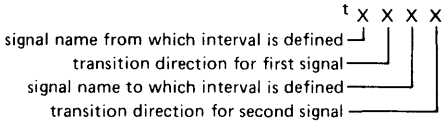
READ OPERATION

After access time, data is valid at the outputs in the READ mode.

ERASING INSTRUCTIONS

The MCM2532/25A32 can be erased by exposure to high intensity shortwave ultraviolet light, with a wavelength of 2537 angstroms. The recommended integrated dose (i.e., UV-intensity X exposure time) is 15 Ws/cm^2. As an example, using the "Model 30-000" UV-Eraser (Turner Designs, Mountain View, CA 94043) the ERASE-time is 36 minutes. The lamps should be used without shortwave filters and the MCM2532/25A32 should be positioned about one inch away from the UV-tubes.

TIMING PARAMETER ABBREVIATIONS



The transition definitions used in this data sheet are:

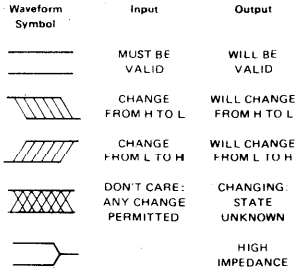
- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

2

WAVEFORMS



MOTOROLA

MCM2708
MCM27A08

MOS

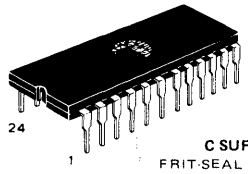
(N-CHANNEL, SILICON-GATE)

1024 X 8-BIT UV ERASABLE PROM

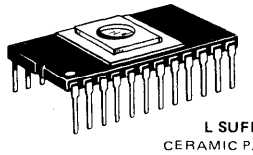
1024 X 8 ERASABLE PROM

The MCM2708/27A08 is an 8192-bit Erasable and Electrically Reprogrammable PROM designed for system debug usage and similar applications requiring nonvolatile memory that could be reprogrammed periodically. The transparent window on the package allows the memory content to be erased with ultraviolet light. Pin-for-pin mask-programmable ROMs are available for large volume production runs of systems initially using the MCM2708/27A08.

- Organized as 1024 Bytes of 8 Bits
- Static Operation
- Standard Power Supplies of +12 V, +5 V and -5 V
- Maximum Access Time = 300 ns – MCM27A08
  450 ns – MCM2708
- Low Power Dissipation
- Chip-Select Input for Memory Expansion
- TTL Compatible
- Three-State Outputs
- Pin Equivalent to the 2708
- Pin-for-Pin Compatible to MCM65308, MCM68308 or 2308 Mask-Programmable ROMs



C SUFFIX
FRIT-SEAL PACKAGE
CASE 623A

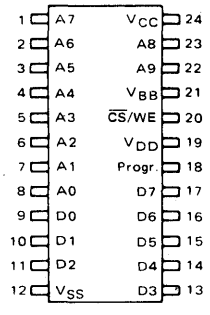


L SUFFIX
CERAMIC PACKAGE
CASE 716

PIN CONNECTION DURING READ OR PROGRAM

Mode	Pin Number						
	9-11, 13-17	12	18	19	20	21	24
Read	D_{out}	V_{SS}	V_{SS}	V_{DD}	V_{IL}	V_{BB}	V_{CC}
Program	Din	V_{SS}	Pulsed V_{IHP}	V_{DD}	V_{IHW}	V_{BB}	V_{CC}

PIN ASSIGNMENT

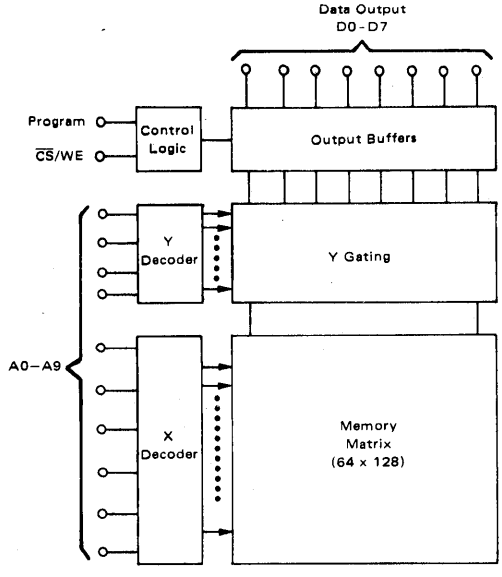


ABSOLUTE MAXIMUM RATINGS (1)

Rating	Value	Unit
Operating Temperature	0 to +70	°C
Storage Temperature	-65 to +125	°C
V_{DD} with Respect to V_{BB}	+20 to -0.3	Vdc
V_{CC} and V_{SS} with Respect to V_{BB}	+15 to -0.3	Vdc
All Input or Output Voltages with Respect to V_{BB} during Read	+15 to -0.3	Vdc
$\overline{CS}$/WE Input with Respect to V_{BB} during Programming	+20 to -0.3	Vdc
Program Input with Respect to V_{BB}	+35 to -0.3	Vdc
Power Dissipation	1.8	Watts

Note 1:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

BLOCK DIAGRAM



DC READ OPERATING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC READ OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
	V_{DD}	11.4	12	12.6	Vdc
	V_{BB}	-5.25	-5.0	-4.75	Vdc
Input High Voltage	V_{IH}	3.0	–	V_{CC} + 1.0	Vdc
Input Low Voltage	V_{IL}	V_{SS}	–	0.65	Vdc

READ OPERATION DC CHARACTERISTICS

Characteristic		Condition	Symbol	Min	Typ	Max	Unit
Address and CS Input Sink Current		V_{in} = 5.25 V or V_{in} = V_{IL}	I_{in}	–	1	10	μA
Output Leakage Current		V_{out} = 5.25 V, $\overline{CS}$/WE = 5 V	I_{LO}	–	1	10	μA
V_{DD} Supply Current		Worst-Case Supply Currents	I_{DD}	–	50	65	mA
V_{CC} Supply Current	(Note 2)	All Inputs High	I_{CC}	–	6	10	mA
V_{BB} Supply Current		$\overline{CS}$/WE = 5.0 V, T_A = 0°C	I_{BB}	–	30	45	mA
Output Low Voltage		I_{OL} = 1.6 mA	V_{OL}	–	–	0.45	V
Output High Voltage		I_{OH} = -100 μA	$V_{OH}1$	3.7	–	–	V
Output High Voltage		I_{OH} = -1.0 mA	$V_{OH}2$	2.4	–	–	V
Power Dissipation	(Note 2)	T_A = 70°C	P_D	–	–	800	mW

Note 2:
The total power dissipation is specified at 800 mW. It is not calculable by summing the various current (I_{DD}, I_{CC}, and I_{BB}) multiplied by their respective voltages, since current paths exist between the various power supplies and V_{SS}. The I_{DD}, I_{CC}, and I_{BB} currents should be used to determine power supply capacity only.

V_{BB} must be applied prior to V_{CC} and V_{DD}. V_{BB} must also be the last power supply switched off.

2

AC READ OPERATING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature range unless otherwise noted.)
(All timing with $t_r = t_f = 20$ ns, Load per Note 3)

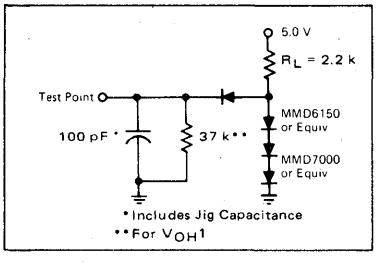
Characteristic	Symbol	MCM27A08			MCM2708			Unit
		Min	Typ	Max	Min	Typ	Max	
Address to Output Delay	t_{AO}	–	220	300	–	280	450	ns
Chip Select to Output Delay	t_{CO}	–	60	120	–	60	120	ns
Data Hold from Address	t_{DHA}	0	–	–	0	–	–	ns
Data Hold from Deselection	t_{DHD}	0	–	120	0	–	120	ns

CAPACITANCE (periodically sampled rather than 100% tested.)

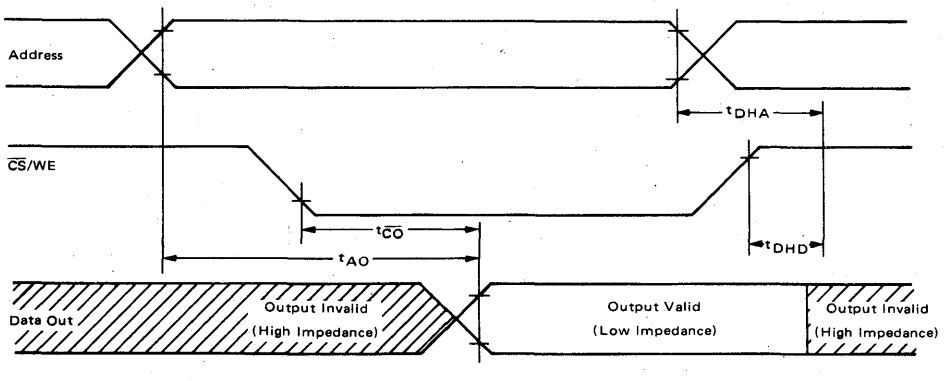
Characteristic	Condition	Symbol	Typ	Max	Unit
Input Capacitance (f = 1.0 MHz)	$V_{in} = 0$ V, $T_A = 25^oC$	C_{in}	4.0	6.0	pF
Output Capacitance (f = 1.0 MHz)	$V_{out} = 0$ V, $T_A = 25^oC$	C_{out}	8.0	12	pF

Note 3:
Output Load = 1 TTL Gate and C_L = 100 pF (Includes Jig Capacitance)
Timing Measurement Reference Levels: Inputs: 0.8 V and 2.8 V
Outputs: 0.8 V and 2.4 V

AC TEST LOAD



READ OPERATION TIMING DIAGRAM



DC PROGRAMMING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED PROGRAMMING OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
	V_{DD}	11.4	12	12.6	Vdc
	V_{BB}	-5.25	-5.0	-4.75	Vdc
Input High Voltage for All Addresses and Data	V_{IH}	3.0	–	V_{CC} + 1.0	Vdc
Input Low Voltage (except Program)	V_{IL}	V_{SS}	–	0.65	Vdc
$\overline{CS}$/WE Input High Voltage (Note 4)	V_{IHW}	11.4	12	12.6	Vdc
Program Pulse Input High Voltage (Note 4)	V_{IHP}	25	–	27	Vdc
Program Pulse Input Low Voltage (Note 5)	V_{ILP}	V_{SS}	–	1.0	Vdc

Note 4: Referenced to V_{SS}.
Note 5: $V_{IHP} - V_{ILP} = 25$ V min.

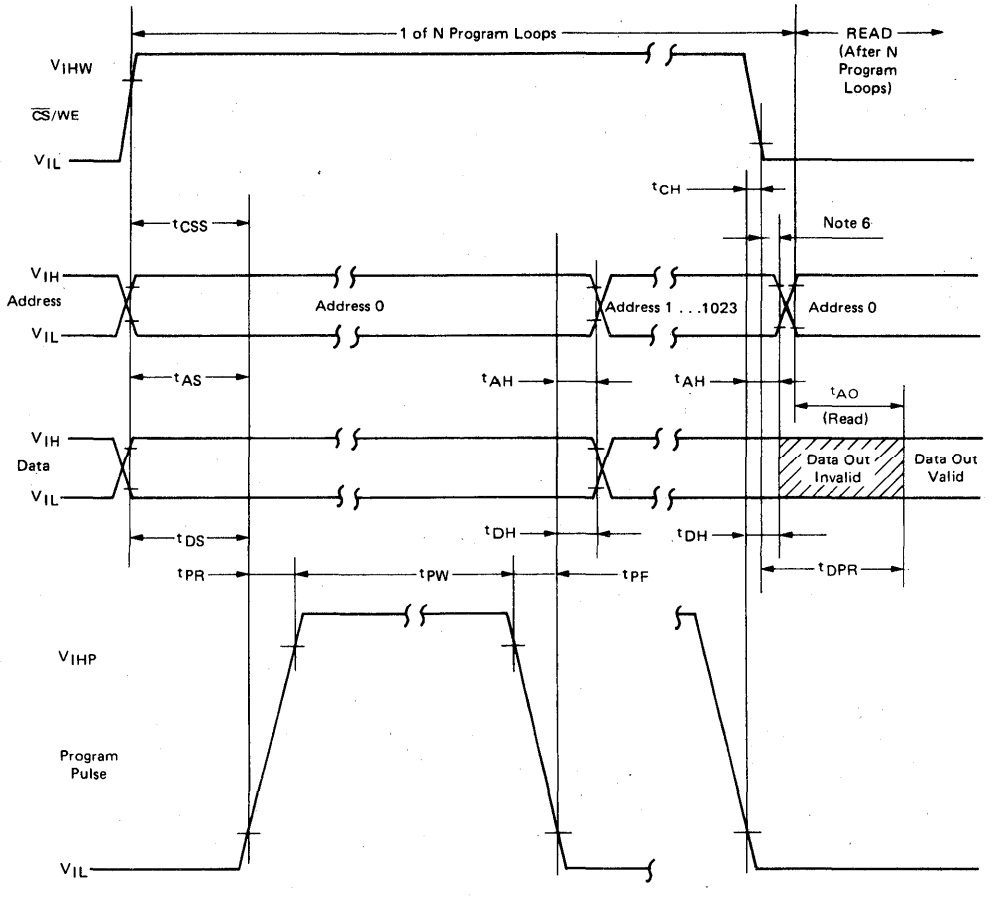
PROGRAMMING OPERATION DC CHARACTERISTICS

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address and $\overline{CS}$/WE Input Sink Current	V_{in} = 5.25 V	I_{LI}	–	–	10	μAdc
Program Pulse Source Current		I_{IPL}	–	–	3.0	mAdc
Program Pulse Sink Current		I_{IPH}	–	–	20	mAdc
V_{DD} Supply Current	Worst-Case Supply Currents	I_{DD}	–	50	65	mAdc
V_{CC} Supply Current	All Inputs High	I_{CC}	–	6	10	mAdc
V_{BB} Supply current	$\overline{CS}$/WE = 5 V, T_A = 0°C	I_{BB}	–	30	45	mAdc

AC PROGRAMMING OPERATING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
Address Setup Time	t_{AS}	10	–	μs
$\overline{CS}$/WE Setup Time	t_{CSS}	10	–	μs
Data Setup Time	t_{DS}	10	–	μs
Address Hold Time	t_{AH}	1.0	–	μs
$\overline{CS}$/WE Hold Time	t_{CH}	0.5	–	μs
Data Hold Time	t_{DH}	1.0	–	μs
Chip Deselect to Output Float Delay	t_{DF}	0	120	ns
Program to Read Delay	t_{DPR}	–	10	μs
Program Pulse Width	t_{PW}	0.1	1.0	ms
Program Pulse Rise Time	t_{PR}	0.5	2.0	μs
Program Pulse Fall Time	t_{PF}	0.5	2.0	μs

PROGRAMMING OPERATION TIMING DIAGRAM



Note 6: The $\overline{CS}$/WE transition must occur after the Program Pulse transition and before the Address Transition.

PROGRAMMING INSTRUCTIONS

After the completion of an ERASE operation, every bit in the device is in the "1" state (represented by Output High). Data are entered by programming zeros (Output Low) into the required bits. The words are addressed the same way as in the READ operation. A programmed "0" can only be changed to a "1" by ultraviolet light erasure.

To set the memory up for programming mode, the $\overline{CS}$/WE input (Pin 20) should be raised to +12 V. Programming data is entered in 8-bit words through the data output terminals (D0 to D7).

Logic levels for the data lines and addresses and the supply voltages (V_{CC}, V_{DD}, V_{BB}) are the same as for the READ operation.

After address and data setup one program pulse per address is applied to the program input (Pin 18). A program loop is a full pass through all addresses. Total programming time, $T_{Ptotal} = N \times t_{PW} \geqslant 100$ ms. The required number of program loops (N) is a function of the program pulse width (t_{PW}), where: $0.1 \text{ ms} \leqslant t_{PW} \leqslant 1.0$ ms; correspondingly N is: $100 \leqslant N \leqslant 1000$. There must be N successive loops through all 1024 addresses. It is not permitted to apply more than one program pulse in succession to the same address (i.e., N program pulses to an address and then change to the next address to be programmed). At the end of a program sequence the $\overline{CS}$/WE falling edge transition must occur before the first address transition, when changing from a PROGRAM to a READ cycle. The program pin (Pin 18) should be pulled down to V_{ILP} with an active device, because this pin sources a small amount of current (I_{IPL}) when $\overline{CS}$/WE is at V_{IHW} (12 V) and the program pulse is at V_{ILP}.

EXAMPLES FOR PROGRAMMING

Always use the $T_{Ptotal} = N \times t_{PW} \geqslant 100$ ms relationship.

1. All 8192 bits should be programmed with a 0.2 ms program pulse width.

   The minimum number of program loops:

   $$N = \frac{T_{Ptotal}}{t_{PW}} = \frac{100 \text{ ms}}{0.2 \text{ ms}} = 500$$. One program loop consists of words 0 to 1023.

2. Words 0 to 200 and 300 to 700 are to be programmed. All other bits are "don't care". The program pulse width is 0.5 ms. The minimum number of program loops, $N = \frac{100}{0.5} = 200$. One program loop consists of words 0 to 1023. The data entered into the "don't care" bits should be all 1s.

3. Same requirements as example 2, but the EPROM is now to be updated to include data for words 850 to 880. The minimum number of program loops is the same as in the previous example, N = 200. One program loop consists of words 0 to 1023. The data entered into the "don't care" bits should be all 1s. Addresses 0 to 200 and 300 to 700 must be reprogrammed with their original data pattern.

ERASING INSTRUCTIONS

The MCM2708/27A08 can be erased by exposure to high intensity shortwave ultraviolet light, with a wavelength of 2537 Å. The recommended integrated dose (i.e., UV-intensity x exposure time) is 12.5 Ws/cm^2. As an example, using the "Model 30-000" UV-Eraser (Turner Designs, Mountain View, CA94043) the ERASE-time is 30 minutes. The lamps should be used without shortwave filters and the MCM2708/27A08 should be positioned about one inch away from the UV-tubes.

MOTOROLA

MCM2716
MCM27A16

Advance Information

2

2048 X 8-BIT UV ERASABLE PROM

The MCM2716/27A16 is a 16,384-bit Erasable and Electrically Reprogrammable PROM designed for system debug usage and similar applications requiring nonvolatile memory that could be reprogrammed periodically. The transparent window on the package allows the memory content to be erased with ultraviolet light.

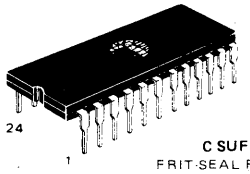
For ease of use, the device operates from a single power supply and has a static power-down mode. Pin-for-pin mask programmable ROMS are available for large volume production runs of systems initially using the MCM2716/27A16.

- Single ±10% 5 V Power Supply
- Automatic Power-down Mode (Standby)
- Organized as 2048 Bytes of 8 Bits
- Low Power Dissipation
- TTL Compatible During Read and Program
- Maximum Access Time = 450 ns MCM2716
  350 ns MCM27A16
- Pin Equivalent to Intel's 2716
- Pin Compatible to MCM68A316E Mask Programmable ROMs

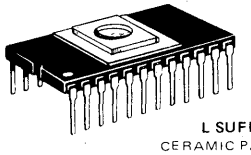
MOS

(N-CHANNEL, SILICON-GATE)

2048 X 8-BIT
UV ERASABLE PROM



C SUFFIX
FRIT-SEAL PACKAGE
CASE 623A



L SUFFIX
CERAMIC PACKAGE
CASE 716

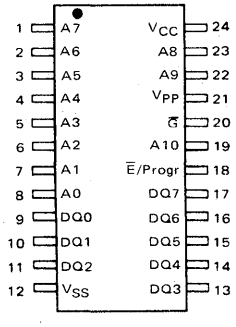
Mode	PIN NUMBER					
	9–11, 13–17	12	18	20	21	24
	DQ	V_{SS}	$\overline{E}$/Progr	$\overline{G}$	V_{PP}	V_{CC}
Read	Data out	V_{SS}	V_{IL}	V_{IL}	V_{CC}	V_{CC}
Output Disable	Hi Z	V_{SS}	Don't Care	V_{IH}	V_{CC}	V_{CC}
Standby	Hi Z	V_{SS}	V_{IH}	Don't Care	V_{CC}	V_{CC}
Program	Data in	V_{SS}	Pulsed V_{IL} to V_{IH}	V_{IH}	V_{IHP}	V_{CC}
Program Verify	Data out	V_{SS}	V_{IL}	V_{IL}	V_{IHP}	V_{CC}
Program Inhibit	Hi Z	V_{SS}	V_{IL}	V_{IH}	V_{IHP}	V_{CC}

ABSOLUTE MAXIMUM RATINGS (1)

Rating	Value	Unit
Temperature Under Bias	–10 to +80	°C
Storage Temperature	–65 to +125	°C
All Input or Output Voltages with Respect to V_{SS} during Read	+ 6 to –0.3	Vdc
V_{PP} Supply Voltage with Respect to V_{SS}	+28 to –0.3	Vdc

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

PIN ASSIGNMENT

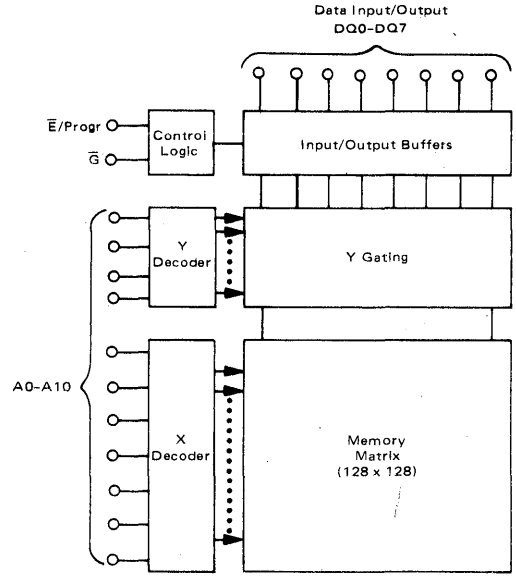


*PIN NAMES
A . . . . Address
DQ . . . . Data Input/Output
$\overline{E}$/Progr . . . . Chip Enable/Program
$\overline{G}$ . . . . Output Enable

*New industry standard nomenclature

This is advance information and specifications are subject to change without notice.

BLOCK DIAGRAM



DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC READ OPERATING CONDITIONS (T_A = 0° to +70°C)

Parameter		Symbol	Min	Nom	Max	Unit
Supply Voltage*	MCM2716	V_{CC}	4.75	5.0	5.25	Vdc
	MCM27A16		4.5	5.0	5.5	
		V_{PP}	V_{CC} – 0.6	5.0	V_{CC} + 0.6	
Input High Voltage		V_{IH}	2.0	–	V_{CC} + 1.0	Vdc
Input Low Voltage		V_{IL}	–0.1	–	0.8	Vdc

READ OPERATION DC CHARACTERISTICS

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address, $\overline{G}$ and $\overline{E}$/Progr Input Sink Current	V_{in} = 5.25 V	I_{in}	–	–	10	μA
Output Leakage Current	V_{out} = 5.25 V, $\overline{G}$ = 5.0 V	I_{LO}	–	–	10	μA
V_{CC} Supply Current* (Standby)	$\overline{E}$/Progr = V_{IH}, $\overline{G}$ = V_{IL}	I_{CC1}	–	10	25	mA
V_{CC} Supply Current* (Active)	$\overline{G}$ = $\overline{E}$/Progr = V_{IL}	I_{CC2}	–	57	100	mA
V_{PP} Supply Current*	V_{PP} = 5.85 V	I_{PP1}	–	–	5.0	mA
Output Low Voltage	I_{OL} = 2.1 mA	V_{OL}	–	–	0.45	V
Output High Voltage	I_{OH} = –400 μA	V_{OH}	2.4	–	–	V

*V_{CC} must be applied simultaneously or prior to V_{PP}. V_{CC} must also be switched off simultaneously with or after V_{PP}. With V_{PP} connected directly to V_{CC} during the read operation, the supply current would be the sum of I_{PP1} and I_{CC}. The additional 0.6 V tolerance on V_{PP} makes it possible to use a driver circuit for switching the V_{PP} supply pin from V_{CC} in Read mode to +25 V for programming. Typical values are for T_A = 25°C and nominal supply voltages.

CAPACITANCE

(f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	4.0	6.0	pF
Output Capacitance (V_{out} = 0 V)	C_{out}	8.0	12	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I\Delta_t}{\Delta V}$.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

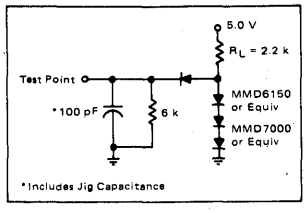
AC OPERATING CONDITIONS AND CHARACTERISTICS

(T_A = 0 to +70°C, V_{CC} = 5.0 V ± 10% unless otherwise noted.)

Input Pulse Levels . . . . . 0.8 Volt to 2.2 Volts
Input Rise and Fall Times . . . . . 20 ns
Input and Output Timing Levels . . . . . 2.0 Volts
Output Load . . . . . See Figure 1

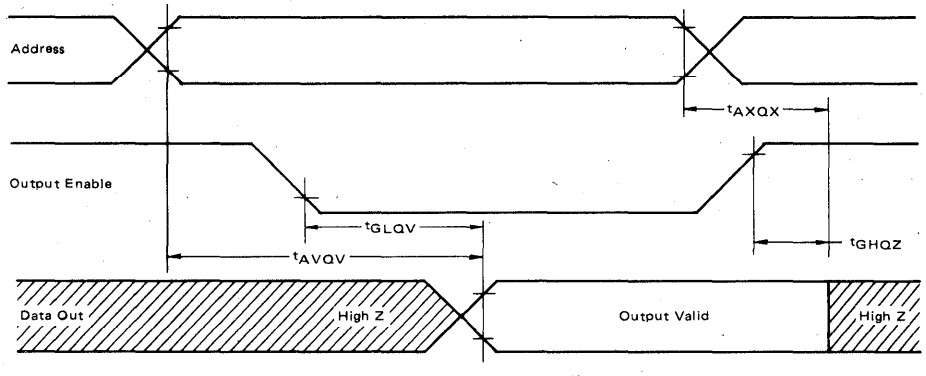
Characteristic	Condition	Symbol	MCM27A16 Min	MCM27A16 Max	MCM2716 Min	MCM2716 Max	Units
Address Valid to Output Valid	$\overline{E}$/Progr = G = V_{IL}	t_{AVQV}	–	350	–	450	ns
$\overline{E}$/Progr to Output Valid	(Note 2)	t_{ELQV}	–	350	–	450	ns
Output Enable to Output Valid	$\overline{E}$/Progr = V_{IL}	t_{GLQV}	–	120	–	120	ns
$\overline{E}$/Progr to Hi Z Output		t_{EHQZ}	0	100	0	100	ns
Output Disable to Hi Z Output	$\overline{E}$/Progr = V_{IL}	t_{GHQZ}	0	100	0	100	ns
Data Hold from Address	$\overline{E}$/Progr = G = V_{IL}	t_{AXDX}	0	–	0	–	ns

FIGURE 1 – AC TEST LOAD



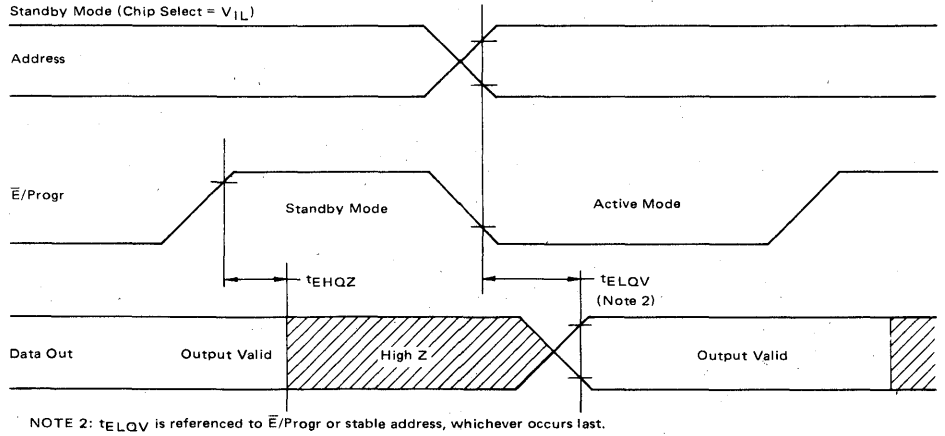
READ MODE TIMING DIAGRAMS

(Chip Enable = V_{IL})



STANDBY MODE

(Output Enable = V_{IL})



NOTE 2: t_{ELQV} is referenced to $\overline{E}$/Progr or stable address, whichever occurs last.

DC PROGRAMMING CONDITIONS AND CHARACTERISTICS

(T_A = 0 to +70°C, V_{CC} = 5.0 V ± 10%)

RECOMMENDED PROGRAMMING OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
	V_{PP}	24	25	26	Vdc
Input High Voltage for Data	V_{IH}	2.2	–	V_{CC} + 1	Vdc
Input Low Voltage for Data	V_{IL}	-0.1	–	0.8	Vdc

*V_{CC} must be applied simulataneously or prior to V_{PP}. V_{CC} must also be switched off simultaneously with or after V_{PP}. The device must not be inserted into or removed from a board with V_{PP} at +25 V. V_{PP} must not exceed the +26 V maximum specifications.

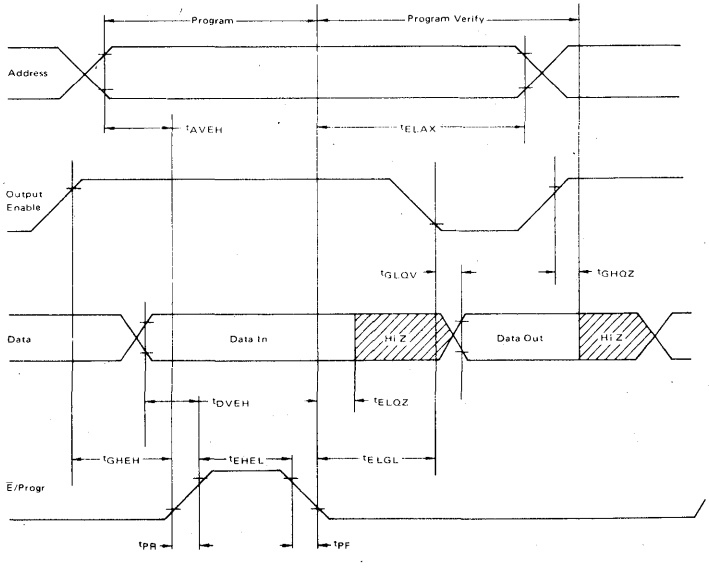
PROGRAMMING OPERATION DC CHARACTERISTICS

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address, $\overline{G}$ and $\overline{E}$/Progr Input Sink Current	V_{in} = 5.25 V/0.45	I_{LI}	–	–	10	μAdc
V_{PP} Supply Current	$\overline{E}$/Progr = V_{IL}	I_{PP1}	–	–	5.0	mAdc
V_{PP} Programming Pulse Supply Current	$\overline{E}$/Progr = V_{IH}	I_{PP2}	–	–	30	mAdc
V_{CC} Supply Current		I_{CC}	–	–	100	mAdc

AC PROGRAMMING OPERATING CONDITIONS AND CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Address Setup Time	t_{AVEH}	2.0	–	μs
Output Enable High to Program Pulse	t_{GHEH}	2.0	–	μs
Data Setup Time	t_{DVEH}	2.0	–	μs
Address Hold Time	t_{ELAX}	2.0	–	μs
Output Enable Hold Time	t_{ELGL}	2.0	–	μs
Data Hold Time	t_{ELQZ}	2.0	–	μs
Output Disable to Hi Z Output	t_{GHQZ}	0	120	ns
Output Enable to Valid Data ($\overline{E}$/Progr = V_{IL})	t_{GLQV}	–	120	ns
Program Pulse Width	t_{EHEL}	45	55	ms
Program Pulse Rise Time	t_{PR}	5	–	ns
Program Pulse Fall Time	t_{PF}	5	–	ns

PROGRAMMING OPERATION TIMING DIAGRAM



PROGRAMMING INSTRUCTIONS

After the completion of an ERASE operation, every bit in the device is in the "1" state (represented by Output High). Data are entered by programming zeros (Output Low) into the required bits. The words are addressed the same way as in the READ operation. A programmed "0" can only be changed to a "1" by ultraviolet light erasure.

To set the memory up for PROGRAM mode, the Vpp input (pin 21) should be raised to +25 V. The V_{CC} supply voltage is the same as for the READ operation and G is at V_{IH}. Programming data is entered in 8-bit words through the data out (DQ) terminals. Only "'0's" will be programmed when "0's" and "1's" are entered in the data word.

After address and data setup, a 50 ms program pulse (V_{IL} to V_{IH}) is applied to the $\overline{E}$/Progr input. A program pulse is applied to each address location to be programmed. Locations may be programmed individually, sequentially, or at random. The maximum program pulse width is 55 ms; therefore, programming must not be attempted with a dc signal applied to the $\overline{E}$/Progr input.

Multiple MCM2716s may be programmed in parallel with the same data by connecting together like inputs and applying the program pulse to the $\overline{E}$/Progr inputs. Different data may be programmed into multiple MCM2716s connected in parallel by using the PROGRAM INHIBIT mode. Except for the $\overline{E}$/Progr pin, all like inputs (including Output Enable) may be common.

The PROGRAM VERIFY mode with Vpp at 25 V is used to determine that all programmed bits were correctly programmed.

READ OPERATION

After access time, data is valid at the outputs in the READ mode. With stable system addresses, effectively faster access time (120 ns) can be obtained by gating the data onto the bus with a low Output Enable input (V_{IL}).

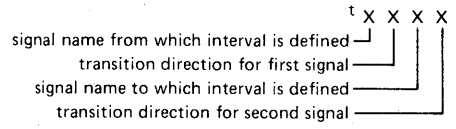
A high level Output Enable input (V_{IH}) puts the MCM2716 in the Output Disable mode with outputs in the high impedance state. This mode allows two or more devices to have outputs OR-tied together on the same data bus. Only one of the MCM2716s in this configuration should have output enable at V_{IL} to prevent contention on the data bus.

The Standby mode is available to reduce active power dissipation from 525 mW to 132 mW. The outputs are in the high impedance state when the $\overline{E}$/Progr input pin is high (V_{IH}) independent of the Output Enable input.

ERASING INSTRUCTIONS

The MCM2716/27A16 can be erased by exposure to high intensity shortwave ultraviolet light, with a wavelength of 2537 Å. The recommended integrated dose (i.e., UV-intensity X exposure time) is 15 Ws/cm^2. As an example, using the "Model 30-000" UV-Eraser (Turner Designs, Mountain View, CA 94043) the ERASE-time is 36 minutes. The lamps should be used without shortwave filters and the MCM2716/27A16 should be positioned about one inch away from the UV-tubes.

TIMING PARAMETER ABBREVIATIONS



The transition definitions used in this data sheet are:

- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS

Waveform Symbol	Input	Output
——— ———	MUST BE VALID	WILL BE VALID
▨	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
▨	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
▨	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
———		HIGH IMPEDANCE

MOTOROLA

MCM68708
MCM68A708

MOS

(N-CHANNEL, SILICON-GATE)

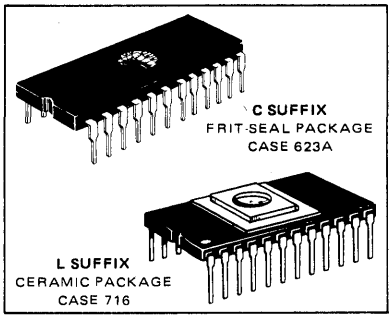
1024 X 8-BIT
UV ERASABLE PROM

2

1024 X 8 ERASABLE PROM

The MCM68708/68A708 is a 8192-bit Erasable and Electrically Reprogrammable PROM designed for system debug usage and similar applications requiring nonvolatile memory that could be reprogrammed periodically. The transparent window on the package allows the memory content to be erased with ultraviolet light. Pin-for-pin mask-programmable ROMs are available for large volume production runs of systems initially using the MCM68708/68A708.

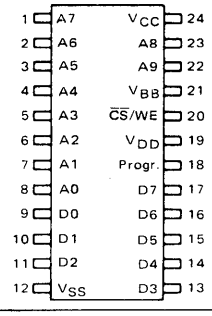
- Organized as 1024 Bytes of 8 Bits
- Fully Static Operation
- Standard Power Supplies of +12 V, +5 V and -5 V
- Maximum Access Time = 300 ns — MCM68A708
  450 ns — MCM68708
- Low Power Dissipation
- Chip-Select Input for Memory Expansion
- TTL Compatible
- Three-State Outputs
- Pin Equivalent to the 2708
- Pin-for-Pin Compatible to MCM65308, MCM68308 or 2308 Mask-Programmable ROMs
- Bus Compatible to the M6800 Family



C SUFFIX
FRIT-SEAL PACKAGE
CASE 623A

L SUFFIX
CERAMIC PACKAGE
CASE 716

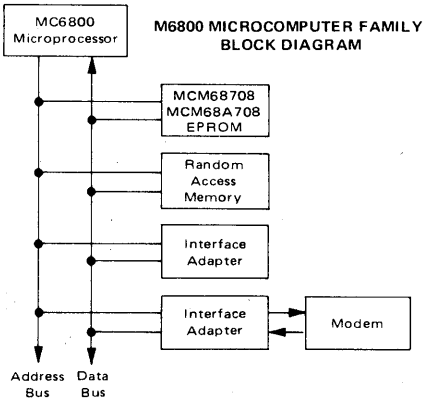
PIN ASSIGNMENT



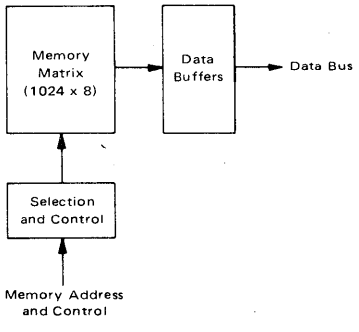
PIN CONNECTION DURING READ OR PROGRAM

Mode	Pin Number						
	9-11, 13-17	12	18	19	20	21	24
Read	D_{out}	V_{SS}	V_{SS}	V_{DD}	V_{IL}	V_{BB}	V_{CC}
Program	D_{in}	V_{SS}	Pulsed V_{IHP}	V_{DD}	V_{IHW}	V_{BB}	V_{CC}

M6800 MICROCOMPUTER FAMILY
BLOCK DIAGRAM

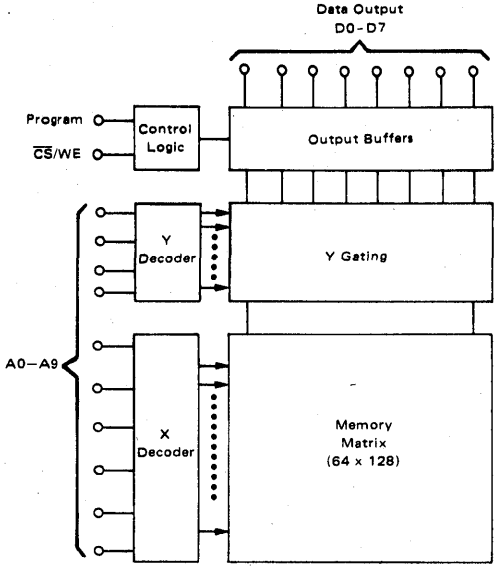


MCM68708/68A708 READ ONLY
MEMORY BLOCK DIAGRAM



2

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

Rating	Value	Unit
Operating, Temperature	0 to +70	°C
Storage Temperature	-65 to +125	°C
V_{DD} with Respect to V_{BB}	+20 to -0.3	Vdc
V_{CC} and V_{SS} with Respect to V_{BB}	+15 to -0.3	Vdc
All Input or Output Voltages with Respect to V_{BB} during Read	+15 to -0.3	Vdc
$\overline{CS}$/WE Input with Respect to V_{BB} during Programming	+20 to -0.3	Vdc
Program Input with Respect to V_{BB}	+35 to -0.3	Vdc
Power Dissipation	1.8	Watts

Note 1:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC READ OPERATING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC READ OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
	V_{DD}	11.4	12	12.6	Vdc
	V_{BB}	-5.25	-5.0	-4.75	Vdc
Input High Voltage	V_{IH}	V_{SS} +2.0	–	V_{CC}	Vdc
Input Low Voltage	V_{IL}	V_{SS} -0.3	–	V_{SS} +0.8	Vdc

READ OPERATION DC CHARACTERISTICS

Characteristic		Condition	Symbol	Min	Typ	Max	Unit
Address and CS Input Sink Current		V_{in} = 5.25 V or V_{in} = V_{IL}	I_{in}	–	1	10	μA
Output Leakage Current		V_{out} = 5.25 V, $\overline{CS}$/WE = 5 V	I_{LO}	–	1	10	μA
V_{DD} Supply Current	(Note 2)	Worst-Case Supply Currents	I_{DD}	–	50	65	mA
V_{CC} Supply Current		All Inputs High	I_{CC}	–	6	10	mA
V_{BB} Supply Current		$\overline{CS}$/WE = 5.0 V, T_A = 0°C	I_{BB}	–	30	45	mA
Output Low Voltage		I_{OL} = 1.6 mA	V_{OL}	–	–	V_{SS} +0.4	V
Output High Voltage		I_{OH} = -100 μA	V_{OH}	V_{SS} +2.4	–	–	V
Power Dissipation	(Note 2)	T_A = 70°C	P_D	–	–	800	mW

Note 2:
The total power dissipation is specified at 800 mW. It is not calculable by summing the various currents (I_{DD}, I_{CC}, and I_{BB}) multiplied by their respective voltages, since current paths exist between the various power supplies and V_{SS}. The I_{DD}, I_{CC}, and I_{BB} currents should be used to determine power supply capacity only.

V_{BB} must be applied prior to V_{CC} and V_{DD}. V_{BB} must also be the last power supply switched off.

AC READ OPERATING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature range unless otherwise noted.)
(All timing with $t_r = t_f = 20$ ns, Load per Note 3)

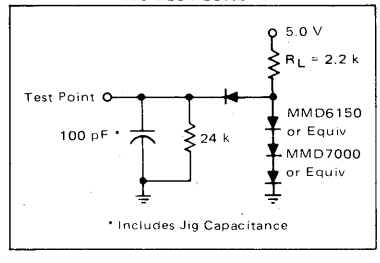
Characteristic	Symbol	MCM68A708			MCM68708			Unit
		Min	Typ	Max	Min	Typ	Max	
Address to Output Delay	t_{AO}	–	220	300	–	280	450	ns
Chip Select to Output Delay	t_{CO}	–	60	120	–	60	120	ns
Data Hold from Address	t_{DHA}	10	–	–	10	–	–	ns
Data Hold from Deselection	t_{DHD}	10	–	120	10	–	120	ns

CAPACITANCE (periodically sampled rather than 100% tested.)

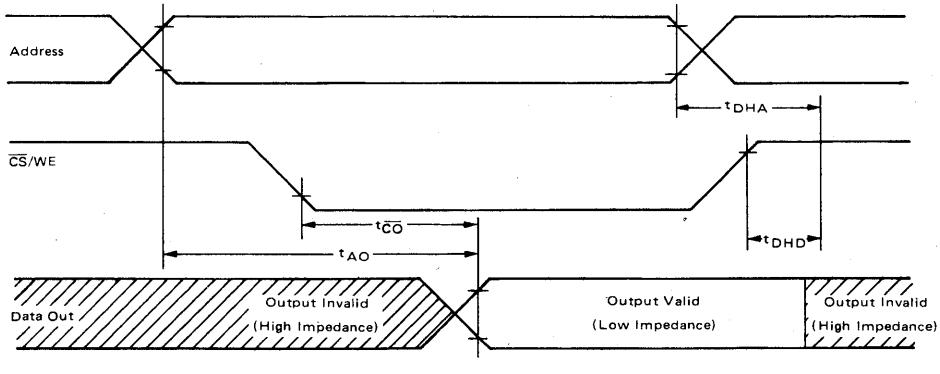
Characteristic	Condition	Symbol	Typ	Max	Unit
Input Capacitance (f = 1.0 MHz)	$V_{in} = 0$ V, $T_A = 25^oC$	C_{in}	4.0	6.0	pF
Output Capacitance (f = 1.0 MHz)	$V_{out} = 0$ V, $T_A = 25^oC$	C_{out}	8.0	12	pF

Note 3:
Output Load = 1 TTL Gate and C_L = 100 pF (Includes Jig Capacitance)
Timing Measurement Reference Levels: Inputs: 0.8 V and 2.8 V
Outputs: 0.8 V and 2.4 V

AC TEST LOAD



READ OPERATION TIMING DIAGRAM



2

DC PROGRAMMING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED PROGRAMMING OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
	V_{DD}	11.4	12	12.6	Vdc
	V_{BB}	-5.25	-5.0	-4.75	Vdc
Input High Voltage for All Addresses and Data	V_{IH}	3.0	–	V_{CC} + 1.0	Vdc
Input Low Voltage (except Program)	V_{IL}	V_{SS}	–	0.65	Vdc
$\overline{CS}$/WE Input High Voltage (Note 4)	V_{IHW}	11.4	12	12.6	Vdc
Program Pulse Input High Voltage (Note 4)	V_{IHP}	25	–	27	Vdc
Program Pulse Input Low Voltage (Note 5)	V_{ILP}	V_{SS}	–	1.0	Vdc

Note 4: Referenced to V_{SS}.
Note 5: $V_{IHP} - V_{ILP} = 25$ V min.

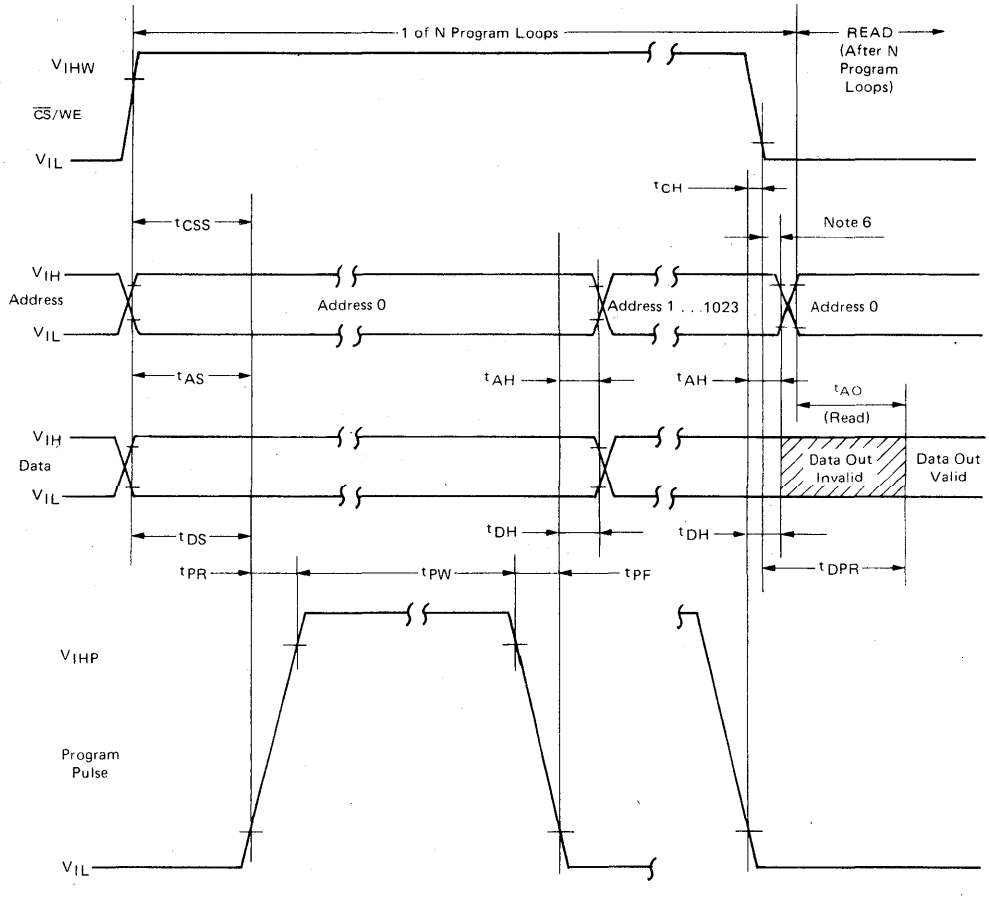
PROGRAMMING OPERATION DC CHARACTERISTICS

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address and $\overline{CS}$/WE Input Sink Current	$V_{in} = 5.25$ V	I_{LI}	–	–	10	μAdc
Program Pulse Source Current		I_{IPL}	–	–	3.0	mAdc
Program Pulse Sink Current		I_{IPH}	–	–	20	mAdc
V_{DD} Supply Current	Worst-Case Supply Currents	I_{DD}	–	50	65	mAdc
V_{CC} Supply Current	All Inputs High	I_{CC}	–	6	10	mAdc
V_{BB} Supply current	$\overline{CS}$/WE = 5 V, $T_A = 0^oC$	I_{BB}	–	30	45	mAdc

AC PROGRAMMING OPERATING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
Address Setup Time	t_{AS}	10	–	μs
$\overline{CS}$/WE Setup Time	t_{CSS}	10	–	μs
Data Setup Time	t_{DS}	10	–	μs
Address Hold Time	t_{AH}	1.0	–	μs
$\overline{CS}$/WE Hold Time	t_{CH}	0.5	–	μs
Data Hold Time	t_{DH}	1.0	–	μs
Chip Deselect to Ouptut Float Delay	t_{DF}	0	120	ns
Program to Read Delay	t_{DPR}	–	10	μs
Program Pulse Width	t_{PW}	0.1	1.0	ms
Program Pulse Rise Time	t_{PR}	0.5	2.0	μs
Program Pulse Fall Time	t_{PF}	0.5	2.0	μs

PROGRAMMING OPERATION TIMING DIAGRAM



Note 6: The $\overline{CS}$/WE transistion must occur after the Program Pulse transition and before the Address Transistion.

PROGRAMMING INSTRUCTIONS

After the completion of an ERASE operation, every bit in the device is in the "1" state (represented by Output High). Data are entered by programming zeros (Output Low) into the required bits. The words are addressed the same way as in the READ operation. A programmed "0" can only be changed to a "1" by ultraviolet light erasure.

To set the memory up for programming mode, the $\overline{CS}$/WE input (Pin 20) should be raised to +12 V. Programming data is entered in 8-bit words through the data output terminals (D0 to D7).

Logic levels for the data lines and addresses and the supply voltages (V_{CC}, V_{DD}, V_{BB}) are the same as for the READ operation.

After address and data setup one program pulse per address is applied to the program input (Pin 18). A program loop is a full pass through all addresses. Total programming time, $T_{Ptotal} = N \times t_{PW} \geq 100$ ms. The required number of program loops (N) is a function of the program pulse width (t_{PW}), where: $0.1 \text{ ms} \leq t_{PW} \leq 1.0$ ms; correspondingly N is: $100 \leq N \leq 1000$. There must be N successive loops through all 1024 addresses. It is not permitted to apply more than one program pulse in succession to the same address (i.e., N program pulses to an address and then change to the next address to be programmed). At the end of a program sequence the $\overline{CS}$/WE falling edge transition must occur before the first address transition, when changing from a PROGRAM to a READ cycle. The program pin (Pin 18) should be pulled down to V_{ILP} with an active device, because this pin sources a small amount of current (I_{IPL}) when $\overline{CS}$/WE is at V_{IHW} (12 V) and the program pulse is at V_{ILP}.

EXAMPLES FOR PROGRAMMING

Always use the $T_{Ptotal} = N \times t_{PW} \geq 100$ ms relationship.

1. All 8092 bits should be programmed with a 0.2 ms program pulse width.

   The minimum number of program loops:

   $$N = \frac{T_{Ptotal}}{t_{PW}} = \frac{100 \text{ ms}}{0.2 \text{ ms}} = 500$$. One program loop consists of words 0 to 1023.

2. Words 0 to 200 and 300 to 700 are to be programmed. All other bits are "don't care". The program pulse width is 0.5 ms. The minimum number of program loops, $N = \frac{100}{0.5} = 200$. One program loop consists of words 0 to 1023. The data entered into the "don't care" bits should be all 1s.

3. Same requirements as example 2, but the EPROM is now to be updated to include data for words 850 to 880. The minimum number of program loops is the same as in the previous example, N = 200. One program loop consists of words 0 to 1023. The data entered into the "don't care" bits should be all 1s. Addresses 0 to 200 and 300 to 700 must be reprogrammed with their original data pattern.

ERASING INSTRUCTIONS

The MCM68708/68A708 can be erased by exposure to high intensity shortwave ultraviolet light, with a wavelength of 2537 Å. The recommended integrated dose (i.e., UV-intensity x exposure time) is 12.5 Ws/cm^2. As an example, using the "Model 30-000" UV-Eraser (Turner Designs, Mountain View, CA 94043) the ERASE-time is 30 minutes. The lamps should be used without shortwave filters and the MCM68708/68A708 should be positioned about one inch away from the UV-tubes.

MOTOROLA

MCM68764
MCM68A764

Advance Information

MOS

(N-CHANNEL, SILICON-GATE)

8192 X 8-BIT
UV ERASABLE PROM

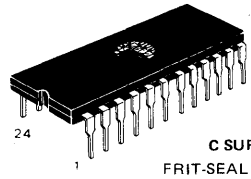
2

8192 X 8-BIT UV ERASABLE PROM

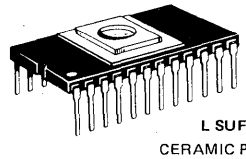
The MCM68764/68A764 is a 65,536-bit Erasable and Electrically Reprogrammable PROM designed for system debug usage and similar applications requiring nonvolatile memory that could be reprogrammed periodically or for replacing 64K ROMs for fast turnaround time. The transparent window on the package allows the memory content to be erased with ultraviolet light.

For ease of use, the device operates from a single power supply and has a static power-down mode. Pin-for-pin mask programmable ROMs are available for large volume production runs of systems initially using the MCM68764/68A764.

- Single +5 V Power Supply
- Automatic Power-down Mode (Standby) with Chip Enable
- Organized as 8192 Bytes of 8 Bits
- Low Power Dissipation
- Fully TTL Compatible
- Maximum Access Time = 450 ns MCM68764
  350 ns MCM68A764
- Standard 24-Pin DIP for EPROM Upgradability
- Pin Compatible to MCM68A364 Mask Programmable ROM



C SUFFIX
FRIT-SEAL PACKAGE
CASE 623A

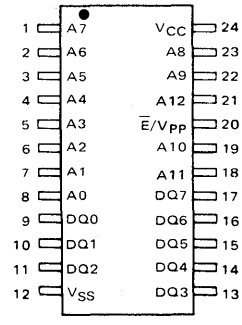


L SUFFIX
CERAMIC PACKAGE
CASE 716

MODE SELECTION

Mode	PIN NUMBER			
	9-11, 13-17, DQ	12 V_{SS}	20 $\overline{E}/V_{PP}$	24 V_{CC}
Read	Data out	V_{SS}	V_{IL}	V_{CC}
Output Disable	Hi-Z	V_{SS}	V_{IH}	V_{CC}
Standby	Hi-Z	V_{SS}	V_{IH}	V_{CC}
Program	Data in	V_{SS}	Pulsed V_{ILP} to V_{IHP}	V_{CC}

PIN ASSIGNMENT



*PIN NAMES	
A	Address
DQ	Data Input/Output
$\overline{E}/V_{PP}$	Chip Enable/Program
$\overline{G}$	Output Enable

*New industry standard nomenclature

ABSOLUTE MAXIMUM RATINGS (1)

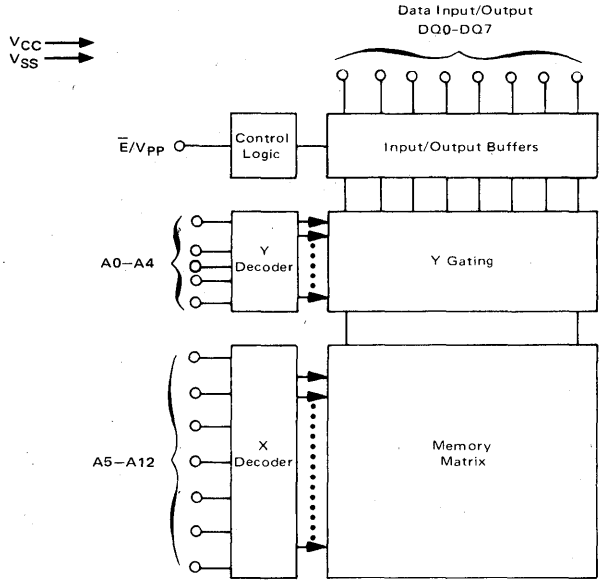
Rating	Value	Unit
Temperature Under Bias	–10 to +80	°C
Storage Temperature	–65 to +125	°C
All Input or Output Voltages with Respect to V_{SS} during Read	+ 6 to –0.3	Vdc
V_{PP} Supply Voltage with Respect to V_{SS}	+28 to –0.3	Vdc

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This is advance information and specifications are subject to change without notice.

2

BLOCK DIAGRAM



DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC READ OPERATING CONDITIONS (T_A = 0° to +70°C)

Parameter		Symbol	Min	Nom	Max	Unit
Supply Voltage*	MCM68764	V_{CC}	4.75	5.0	5.25	Vdc
	MCM68A764		4.5	5.0	5.5	
Input High Voltage		V_{IH}	2.0	–	V_{CC} +1.0	Vdc
Input Low Voltage		V_{IL}	–0.1	–	0.8	Vdc

READ OPERATING DC CHARACTERISTICS

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address Input Sink Current	V_{in} = 5.25 V	I_{in}	–	–	10	μA
Output Leakage Current	V_{out} = 5.25 V	I_{LO}	–	–	10	μA
E/Vpp Input Sink Current	$\overline{E}/V_{PP} = V_{IL}$	I_{EL}	–	–	10	μA
	$\overline{E}/V_{PP} = V_{IH}$	$I_{EH} = I_{PL}$	–	–	200	μA
	$\overline{E}/V_{PP} = V_{IHP}$	I_{PH}	–	–	30	mA
V_{CC} Supply Current (Active)	$\overline{E}/V_{PP} = V_{IL}$	I_{CC1}	–	–	160	mA
V_{CC} Supply Current (Standby)	$\overline{E}/V_{PP} = V_{IH}$	I_{CC2}	–	–	25	mA
Output Low Voltage	I_{OL} = 2.1 mA	V_{OL}	–	0.1	0.45	V
Output High Voltage	I_{OH} = –400 μA	V_{OH}	2.4	4.0	–	V

CAPACITANCE

(f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	4.0	6.0	pF
Output Capacitance (V_{out} = 0 V)	C_{out}	8.0	12	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I\Delta_t}{\Delta V}$.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC PROGRAMMING CONDITIONS AND CHARACTERISTICS

(T_A = 0 to +70°C, V_{CC} = 5.0 V ±5%)

RECOMMENDED PROGRAMMING OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
Input High Voltage for All Addresses and Data	V_{IH}	2.0	–	V_{CC} + 1	Vdc
Input Low Voltage for All Addresses and Data	V_{IL}	–0.1	–	0.8	Vdc
Program Pulse Input High Voltage	V_{IHP}	24	25	26	Vdc
Program Pulse Input Low Voltage	V_{ILP}	2.0	V_{CC}	6.0	Vdc

PROGRAMMING OPERATION DC CHARACTERISTICS

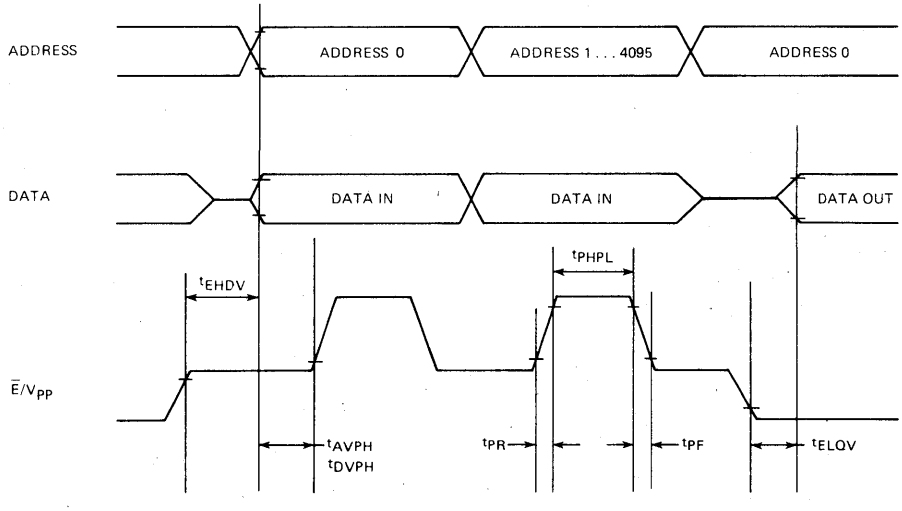
Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address Input Sink Current	V_{in} = 5.25 V	I_{LI}	–	–	10	μAdc
Program Pulse Current (Vpp = 25 V)		I_{PH}	–	–	30	mAdc
Vpp Programming Pulse Current (Vpp = 5 V)		I_{PL} = I_{EH}	–	–	200	μA
V_{CC} Supply Current		I_{CC}	–	–	160	mAdc

AC PROGRAMMING OPERATING CONDITIONS AND CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Address Setup Time	t_{AVPH}	2.0	–	μs
Data Setup Time	t_{DVPH}	2.0	–	μs
Chip Enable to Valid Data	t_{ELQV}	450	–	ns
Chip Disable to Data In	t_{EHDV}	2.0	–	μs
Program Pulse Width*	t_{PHPL}	1.0	55	ms
Program Pulse Rise Time	t_{PR}	0.5	2.0	μs
Program Pulse Fall Time	t_{PF}	0.5	2.0	μs

*The minimum programming time is twice the programming time after successful verification of the programmed pattern, but maximum programming time is 55 ms.

PROGRAMMING OPERATION TIMING DIAGRAM



2

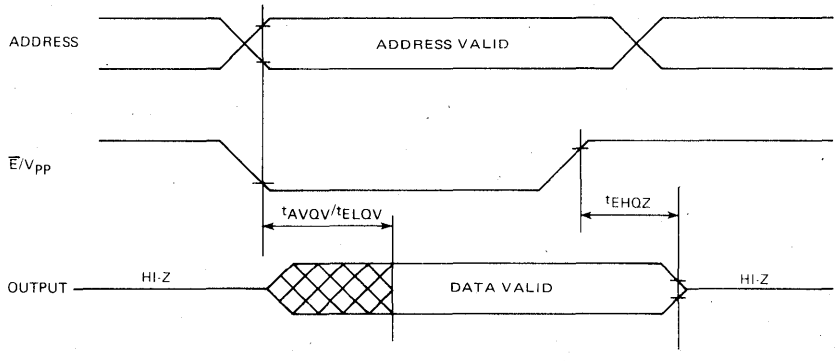
AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

Input Pulse Levels . . . . . 0.8 Volt to 2.2 Volts
Input Rise and Fall Times . . . . . 20 ns
Input Timing Levels . . . . . 1 Volt and 2 Volts
Output Timing Levels . . . . . 0.8 Volt to 2 Volts
Output Load . . . . . 100 pF + 1 74 Series TTL Load

Characteristic	Condition	Symbol	MCM68A764		MCM68764		Units
			Min	Max	Min	Max	
Address Valid to Output Valid	$\overline{E} = V_{IL}$	t_{AVQV}	–	350	–	450	ns
E to Output Valid		t_{ELQV}	–	350	–	450	ns
E to Hi-Z Output		t_{EHQZ}	0	100	0	100	ns
Data Hold from Address	$\overline{E} = V_{IL}$	t_{AXDX}	0	–	0	–	ns

READ MODE TIMING DIAGRAM



PROGRAMMING INSTRUCTIONS

After the completion of an ERASE operation, every bit in the device is in the "1" state (represented by Output High). Data are entered by programming zeros (Output Low) into the required bits. The words are addressed the same way as in the READ operation. A programmed "0" can only be changed to a "1" by ultraviolet light erasure.

To set the memory up for Program Mode, the $\overline{E}$/Vpp input (Pin 20) should be between +2.0 and +6.0 V, which will tristate the outputs and allow data to be setup on the DQ terminals. The V_{CC} voltage is the same as for the Read operation. Only "0's" will be programmed when "0's" and "1's" are entered in the 8-bit data word.

After address and data setup, 25 volt programming pulse (V_{IH} to V_{IHP}) is applied to the $\overline{E}$/Vpp input. A program pulse is applied to each address location to be programmed. Locations may be programmed individually, sequentially, or at random. The maximum program pulse width is 55 ms and the maximum program pulse amplitude is 26.0 V.

Multiple MCM68764s may be programmed in parallel by connecting like inputs and applying the program pulse to the $\overline{E}$/Vpp inputs. Different data may be programmed into multiple MCM68764s connected in parallel by selectively applying the programming pulse only to the MCM68764s to be programmed.

READ OPERATION

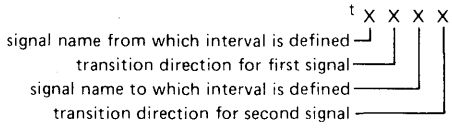
After access time, data is valid at the outputs in the Read mode. A single input ($\overline{E}$/Vpp) enables the outputs and puts the chip in active or standby mode. With $\overline{E}$/Vpp = "0" the outputs are enabled and the chip is in active mode, with $\overline{E}$/Vpp = "1" the outputs are tristated and the chip is in standby mode. During standby mode, the power dissipation is reduced from 880 mW to 132 mW.

Multiple MCM68764 may share a common data bus with like outputs OR-tied together. In this configuration the $\overline{E}$/Vpp input should be high on all unselected MCM 68764s to prevent data contention.

ERASING INSTRUCTIONS

The MCM68764 can be erased by exposure to high intensity shortwave ultraviolet light, with a wavelength of 2537 angstroms. The recommended integrated dose (i.e., UV-intensity X exposure time) is 15 Ws/cm^2. As an example, using the "Model 30-000" UV-Eraser (Turner Designs, Mountain View, CA 94043) the ERASE-time is 36 minutes. The lamps should be used without shortwave filters and the MCM68764 should be positioned about one inch away from the UV-tubes.

TIMING PARAMETER ABBREVIATIONS



The transition definitions used in this data sheet are:

- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS

Waveform Symbol	Input	Output
——— ———	MUST BE VALID	WILL BE VALID
⟍⟍⟍⟍	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
⟋⟋⟋⟋	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
⟋⟍⟋⟍	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
——⟩		HIGH IMPEDANCE

MOTOROLA

TMS2716
TMS27A16

MOS

(N-CHANNEL, SILICON-GATE)

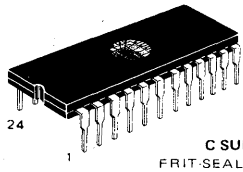
2048 X 8-BIT
UV ERASABLE PROM

2

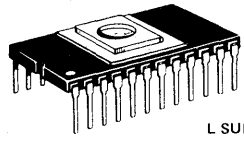
2048 X 8 ERASABLE PROM

The TMS2716 and TMS27A16 are 16,384-bit Erasable and Electrically Reprogrammable PROMs designed for system debug usage and similar applications requiring nonvolatile memory that could be reprogrammed periodically. The transparent window on the package allows the memory content to be erased with ultraviolet light. The TMS2716 is pin compatible with 2708 EPROMs, allowing easy memory size doubling.

- Organized as 2048 Bytes of 8 Bits
- Fully Static Operation (No Clocks, No Refresh)
- Standard Power Supplies of +12 V, +5 V, and -5 V
- Maximum Access Time = 300 ns — TMS27A16
  450 ns — TMS2716
- Chip-Select Input for Memory Expansion
- TTL Compatible — No Pull-up Resistors Required
- Three-State Outputs for OR-Tie Capability
- The TMS2716 is Pin Compatible to MCM2708 and MCM68708 EPROMs

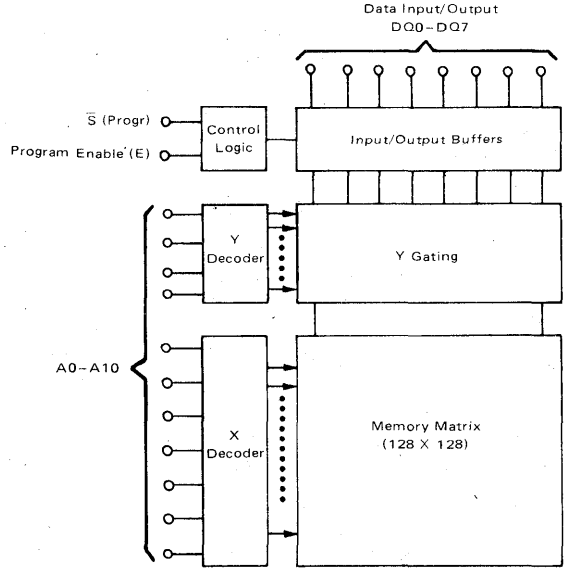


C SUFFIX
FRIT-SEAL PACKAGE
CASE 623A

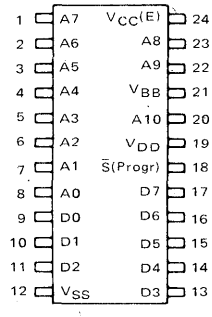


L SUFFIX
CERAMIC PACKAGE
CASE 716

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

A0–A10	Address Inputs
DQ0–DQ7	Data Input (Program) or Output (Read)
(E)	Program Enable
$\overline{S}$	Chip Select
(Progr)	Program Pulse
V_{BB}	-5 V Power Supply
V_{CC}	+5 V Power Supply
V_{DD}	+12 V Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS (1)

Rating	Value	Unit
Operating Temperature	0 to +70	°C
Storage Temperature	−65 to +125	°C
V_{DD} with Respect to V_{BB}	+20 to −0.3	Vdc
V_{CC} and V_{SS} with Respect to V_{BB}	+15 to −0.3	Vdc
All Input or Output Voltage with Respect to V_{BB} During Read	+15 to −0.3	Vdc
(E) Input with Respect to V_{BB} During Programming	+20 to −0.3	Vdc
Program Input with Respect to V_{BB}	+35 to −0.3	Vdc
Power Dissipation	1.8	Watts

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

PIN CONNECTION DURING READ OR PROGRAM

Mode	Pin Number 9–11, 13–17	Pin Number 18	Pin Number 24
Read	D_{out}	V_{IL} or V_{IH}	V_{CC}
Program	D_{in}	Pulsed V_{IHP}	V_{IHW}

DC READ OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC READ OPERATING CONDITIONS

Parameter		Symbol	Min	Nom	Max	Unit
Supply Voltage	TMS2716	V_{CC}	4.75	5.0	5.25	Vdc
		V_{DD}	11.4	12	12.6	Vdc
		V_{BB}	−5.25	−5.0	−4.75	Vdc
	TMS27A16	V_{CC}	4.5	5.0	5.5	Vdc
		V_{DD}	10.8	12	13.2	Vdc
		V_{BB}	−5.5	−5.0	−4.5	Vdc
Input High Voltage		V_{IH}	2.2	–	V_{CC} + 1.0	Vdc
Input Low Voltage		V_{IL}	V_{SS}	–	0.65	Vdc

READ OPERATING DC CHARACTERISTICS

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address Input Sink Current	$V_{in} = V_{CC}$max or $V_{in} = V_{IL}$	I_{in}	–	1	10	μA
Output Leakage Current	$V_{out} = V_{CC}$max and $\overline{S} = 5$ V	I_{LO}	–	1	10	μA
V_{DD} Supply Current	Worst-Case Supply Currents All Inputs High (E) = 5.0 V, $T_A = 0^{\circ}C$	I_{DD}	–	–	65	mA
V_{CC} Supply Current		I_{CC}	–	–	12	mA
V_{BB} Supply Current		I_{BB}	–	–	45	mA
Output Low Voltage	$I_{OL} = 1.6$ mA	V_{OL}	–	–	0.45	V
Output High Voltage	$I_{OH} = -100$ μA	V_{OH1}	3.7	–	–	V
Output High Voltage	$I_{OH} = -1.0$ mA	V_{OH2}	2.4	–	–	V

V_{BB} must be applied prior to V_{CC} and V_{DD}. V_{BB} must also be the last power supply switched off.

CAPACITANCE (periodically sampled rather than 100% tested)

Characteristic	Condition	Symbol	Typ	Max	Unit
Input Capacitance (f = 1.0 MHz)	$V_{in} = 0$ V, $T_A = 25^{\circ}C$	C_{in}	4.0	6.0	pF
Output Capacitance (f = 1.0 MHz)	$V_{out} = 0$ V, $T_A = 25^{\circ}C$	C_{out}	8.0	12	pF

2

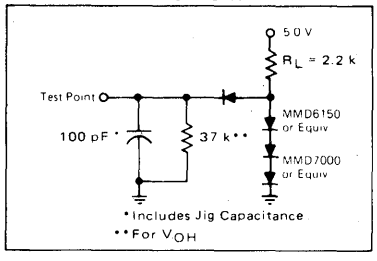
AC READ OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)
(All timing with $t_r = t_f = 20$ ns, Load per Note 2)

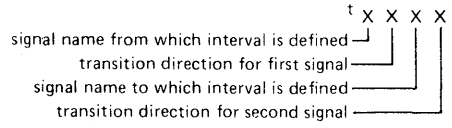
Characteristic	Symbol	TMS2716		TMS27A16		Unit
		Min	Max	Min	Max	
Address to Output Delay	t_{AVQV}	–	450	–	300	ns
Chip Select to Output Delay	t_{SLQV}	–	120	–	120	ns
Data Hold from Address	t_{AXQZ}	10	–	10	–	ns
Data Hold from Deselection	t_{SHQZ}	10	120	10	120	ns

NOTE 2: Output Load = 1 TTL Gate and C_L = 100 pF (Includes Jig Capacitance)
Timing Measurement Reference Levels – Inputs: 0.8 V and 2.8 V
Outputs: 0.8 V and 2.4 V

AC TEST LOAD



TIMING PARAMETER ABBREVIATIONS



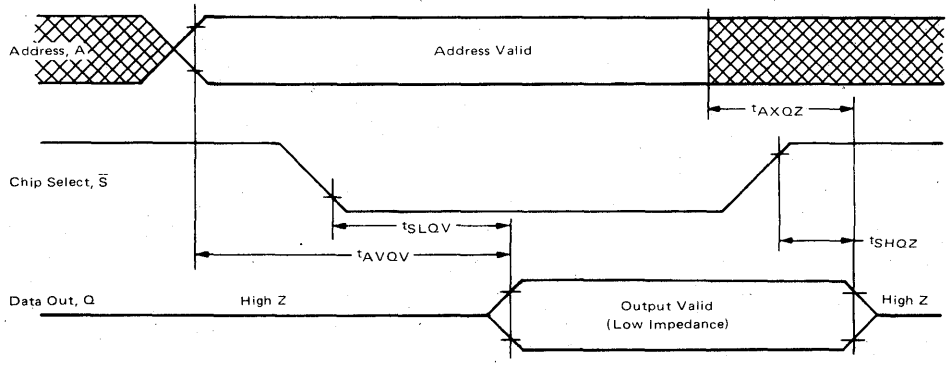
The transition definitions used in this data sheet are:

- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ OPERATION TIMING DIAGRAM



DC PROGRAMMING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED PROGRAMMING OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
	V_{DD}	11.4	12	12.6	Vdc
	V_{BB}	-5.25	-5.0	-4.75	Vdc
Input High Voltage for Data	V_{IHD}	3.8	–	V_{CC} + 1	Vdc
Input Low Voltage for Data	V_{ILD}	V_{SS}	–	0.65	Vdc
Input High Voltage for Addresses	V_{IHA}	3.8	–	V_{CC} + 1	Vdc
Input Low Voltage for Addresses	V_{ILA}	V_{SS}	–	0.4	Vdc
Program Enable (E) Input High Voltage (Note 3)	V_{IHW}	11.4	12	12.6	Vdc
Program Enable (E) Input Low Voltage (Note 3)	$V_{ILW}=V_{CC}$	4.75	5.0	5.25	Vdc
Program Pulse Input High Voltage (Note 3)	V_{IHP}	25	–	27	Vdc
Program Pulse Input Low Voltage (Note 4)	V_{ILP}	V_{SS}	–	1.0	Vdc

NOTE 3: Referenced to V_{SS}.
NOTE 4: $V_{IHP} - V_{ILP} = 25$ V min.

PROGRAMMING OPERATION DC CHARACTERISTICS

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address Input Sink Current	$V_{in} = 5.25$ V	I_{LI}	–	–	10	μAdc
Program Pulse Source Current		I_{IPL}	–	–	3.0	mAdc
Program Pulse Sink Current		I_{IPH}	–	–	20	mAdc
V_{DD} Supply Current	Worst-Case Supply Currents All Inputs High (E) = 5 V, $T_A = 0^oC$	I_{DD}	–	–	65	mAdc
V_{CC} Supply Current		I_{CC}	–	–	15	mAdc
V_{BB} Supply current		I_{BB}	–	–	45	mAdc

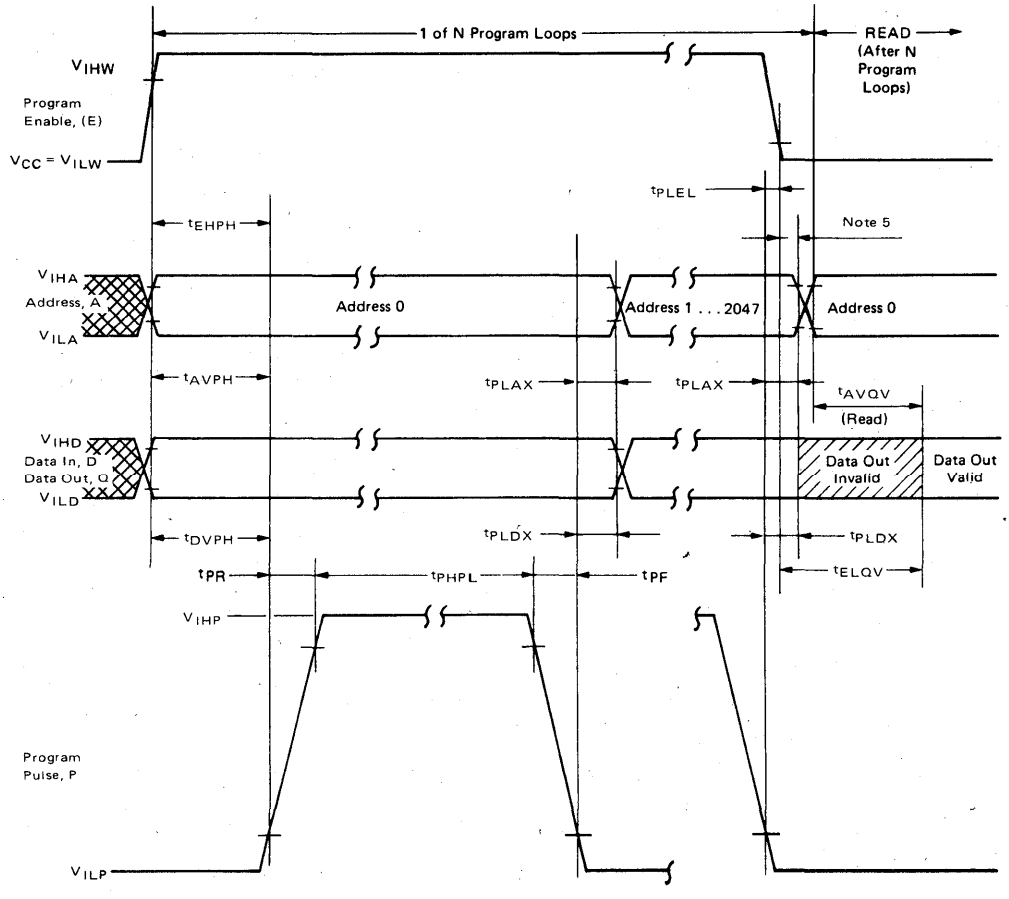
AC PROGRAMMING OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Address Setup Time	t_{AVPH}	10	–	μs
(E) Setup Time	t_{EHPH}	10	–	μs
Data Setup Time	t_{DVPH}	10	–	μs
Address Hold Time	t_{PLAX}	1.0	–	μs
(E) Hold Time	t_{PLEL}	0.5	–	μs
Data Hold Time	t_{PLDX}	1.0	–	μs
Program to Read Delay	t_{ELQV}	–	10	μs
Program Pulse Width	t_{PHPL}	0.1	1.0	ms
Program Pulse Rise Time	t_{PR}	0.5	2.0	μs
Program Pulse Fall Time	t_{PF}	0.5	2.0	μs

2

PROGRAMMING OPERATION TIMING DIAGRAM



NOTE 5: This Program Enable tranistion must occur after the Program Pulse transition and before the Address Transition.

WAVEFORM DEFINITIONS

Waveform Symbol	Input	Output
———	MUST BE VALID	WILL BE VALID
▨	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
▨	CHANGE FROM L TO H	WILL CHANGE FROM L TO H

Waveform Symbol	Input	Output
▨	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
⟋⟍		HIGH IMPEDANCE

PROGRAMMING INSTRUCTIONS

After the completion of an ERASE operation, every bit in the device is in the "1" state (represented by Output High). Data are entered by programming zeros (Output Low) into the required bits. The words are addressed the same way as in the READ operation. A programmed "0" can only be changed to a "1" by ultraviolet light erasure.

To set the memory up for programming mode, the V_{CC}(E) input (Pin 24) should be raised to +12 V. Programming data is entered in 8-bit words through the data output terminals (DQ0 to DQ7).

The V_{DD} and V_{BB} supply voltages are the same as for the READ operation.

After address and data setup, one program pulse per address is applied to the program input. A program loop is a full pass through all addresses. Total programming time/address, $T_{Ptotal} = N \times t_{PHPL} \geq 100$ ms. The required number of program loops (N) is a function of the program pulse width (t_{PHPL}) where: $0.1 \text{ ms} \leq t_{PHPL} \leq 1.0$ ms; correspondingly, N is: $100 \leq N \leq 1000$. There must be N successive loops through all 2048 addresses. It is not permitted to apply more than one program pulse in succession to the same address (i.e., N program pulses to an address and then change to the next address to be programmed). At the end of a program sequence the Program Enable (E) falling edge transition must occur before the first address transition, when changing from a PROGRAM to a READ cycle. The program pin should be pulled down to V_{ILP} with an active device, because this pin sources a small amount of current (I_{IPL}) when (E) is at V_{IHW} (12 V) and the program pulse is at V_{ILP}.

EXAMPLE FOR PROGRAMMING

Always use the $T_{Ptotal} = N \times t_{PHPL} \geq 100$ ms relationship.

1. All 16,384 bits should be programmed with a 0.2 ms program pulse width.

The minimum number of program loops:

$$N = \frac{T_{Ptotal}}{t_{PHPL}} = \frac{100 \text{ ms}}{0.2 \text{ ms}} = 500.$$

One program loop consists of words 0 to 2047.

2. Words 0 to 200 and 300 to 700 are to be programmed. All other bits are "don't care". The program pulse width is 0.5 ms. The minimum number of program loops, N = 100/0.5 = 200. One program loop consists of words 0 to 2047. The data entered into the "don't care" bits should be all 1s.

3. Same requirements as example 2, but the EPROM is now to be updated to include data for words 850 to 880. The minimum number of program loops is the same as in the previous example, N = 200. One program loop consists of words 0 to 2047. The data entered into the "don't care" bits should be all 1s. Addresses 0 to 200 and 300 to 700 must be reprogrammed with their original data pattern.

ERASING INSTRUCTIONS

The TMS2716/27A16 can be erased by exposure to high intensity shortwave ultraviolet light, with a wavelength of 2537 Å. The recommended integrated dose (i.e., UV-intensity × exposure time) is 12.5 Ws/cm^2. As an example, using the "Model 30-000" UV-Eraser (Turner Designs, Mountain View, CA 94043) the ERASE-time is 30 minutes. The lamps should be used without shortwave filters and the TMS2716/27A16 should be positioned about one inch away from the UV-tubes.

MOTOROLA

MCM6670
MCM6674

MOS

(N-CHANNEL, SILICON GATE)

128c x 7 x 5 HORIZONTAL-SCAN CHARACTER GENERATOR

2

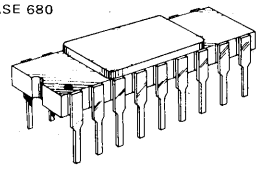
128c X 7 X 5 CHARACTER GENERATOR

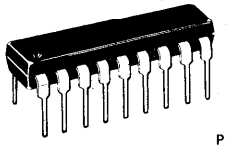
The MCM6670 is a mask-programmable horizontal-scan (row select) character generator containing 128 characters in a 5 X 7 matrix. A 7-bit address code is used to select one of the 128 available characters, and a 3-bit row select code chooses the appropriate row to appear at the outputs. The rows are sequentially displayed, providing a 7-word sequence of 5 parallel bits per word for each character selected by the address inputs.

The MCM6674 is a preprogrammed version of the MCM6670. The complete pattern of this device is contained in this data sheet.

- Fully Static Operation
- TTL Compatibility
- Single ±10% +5 Volt Power Supply
- 18-Pin Package
- Diagonal Corner Power Supply Pins
- Fast Access Time, 350 ns (max)

L SUFFIX
CERAMIC PACKAGE
CASE 680





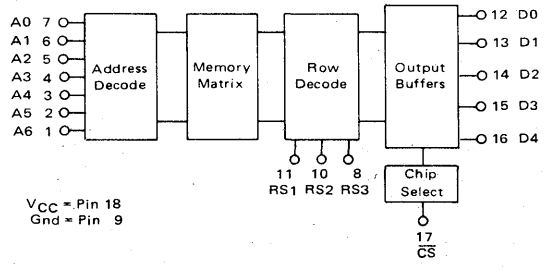
P SUFFIX
PLASTIC PACKAGE
CASE 707

ABSOLUTE MAXIMUM RATINGS (See Note 1)

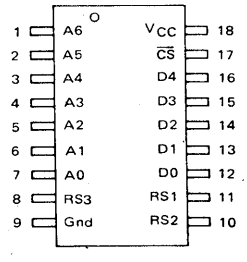
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

BLOCK DIAGRAM



PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISITCS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
Input High Voltage	V_{IH}	2.0	–	5.25	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.8	Vdc

DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (V_{in} = 0 to 5.25 V)	I_{in}	–	–	2.5	μAdc
Output High Voltage (I_{OH} = -205 μA)	V_{OH}	2.4	–	V_{CC}	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	Vdc
Output Leakage Current (Three-State) (CS = 2.0 V or $\overline{CS}$ = 0.8 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	–	–	10	μAdc
Supply Current (V_{CC} = 5.25 V, T_A = 0°C)	I_{CC}	–	–	130	mAdc

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

Characteristic	Symbol	Typ	Unit
Input Capacitance	C_{in}	5.0	pF
Output Capacitance	C_{out}	5.0	pF

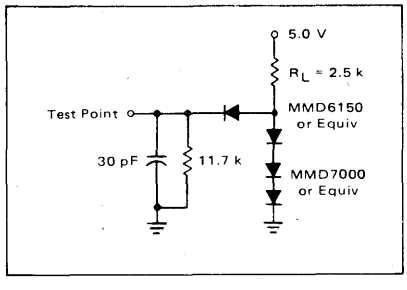
AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

AC TEST CONDITIONS

Condition	Value
Input Pulse Levels	0.8 V to 2.0 V
Input Rise and Fall Times	20 ns
Output Load	1 TTL Gate and C_L = 30 pF

AC TEST LOAD

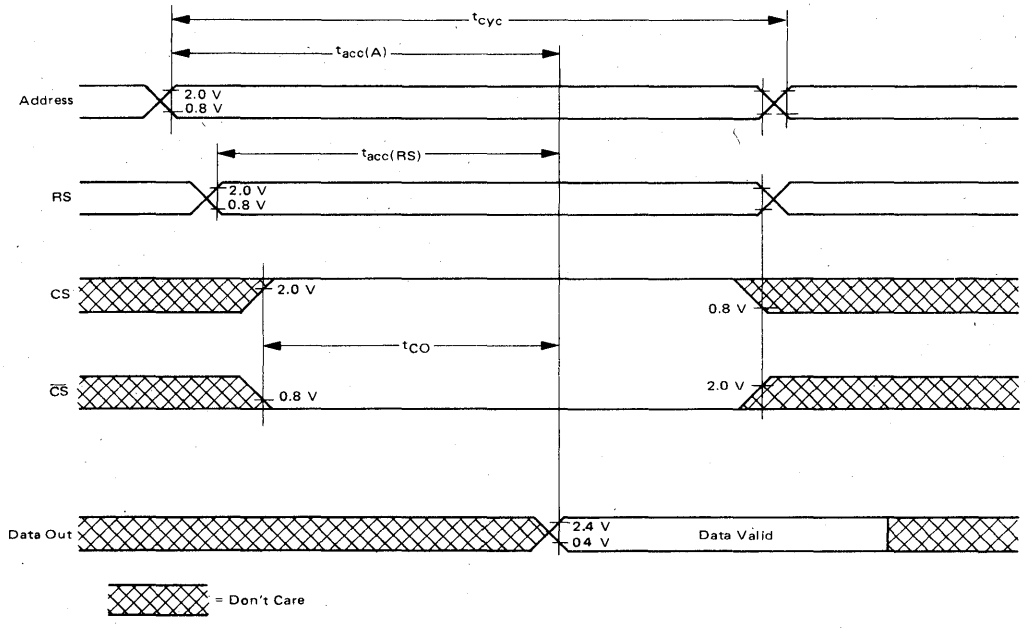


AC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Cycle Time	t_{cyc}	350	–	ns
Address Access Time	$t_{acc(A)}$	–	350	ns
Row Select Access Time	$t_{acc(RS)}$	–	350	ns
Chip Select to Output Delay	t_{CO}	–	150	ns

2

TIMING DIAGRAM



CUSTOM PROGRAMMING FOR MCM6670

By the programming of a single photomask, the customer may specify the content of the MCM6670. Encoding of the photomask is done with the aid of a computer to provide quick, efficient implementation of the custom bit pattern while reducing the cost of implementation.

Information for the custom memory content may be sent to Motorola in the following forms, in order of preference:

1. Hexadecimal coding using IBM Punch Cards (Figures 3 and 4).
2. Hexadecimal coding using ASCII Paper Tape Punch (Figure 5).

Programming of the MCM6670 can be achieved by using the following sequence:

1. Create the 128 characters in a 5 x 7 font using the format shown in Figure 1. Note that information at output D4 appears in column one, D3 in column two, thru D0 information in column five. The dots filled in and programmed as a logic "1" will appear at the outputs as V_{OH}; the dots left blank will be at V_{OL}. R0 is always programmed to be blank (V_{OL}). (Blank formats appear at the end of this data sheet for your convenience; they are not to be submitted to Motorola, however.)

2. Convert the characters to hexadecimal coding treating dots as ones and blanks as zeros, and enter this information in the blocks to the right of the character font format. The information for D4 must be a hex one or zero, and is entered in the left block. The information for D3 thru D0 is entered in the right block, with D3 the most significant bit for the hex coding, and D0 the least significant.

3. Transfer the hexadecimal figures either to punched cards (Figure 3) or to paper tape (Figure 5).

4. Transmit this data to Motorola, along with the customer name, customer part number and revision, and an indication that the source device is the MCM6670.

5. Information should be submitted on an organizational data form such as that shown in Figure 2.

FIGURE 1 – CHARACTER FORMAT

ROW SELECT TRUTH TABLE

RS3	RS2	RS1	OUTPUT
0	0	0	R0
0	0	1	R1
0	1	0	R2
0	1	1	R3
1	0	0	R4
1	0	1	R5
1	1	0	R6
1	1	1	R7

Character Number (CUSTOMER INPUT)

	MSB			LSB	HEX
R0	□	□	□	□	0 0
R1	□	□	⊠	□	0 4
R2	□	⊠	□	⊠	0 A
R3	⊠	□	□	⊠	1 1
R4	⊠	□	□	⊠	1 1
R5	⊠	⊠	⊠	⊠	1 F
R6	⊠	□	□	⊠	1 1
R7	⊠	□	□	⊠	1 1
	D4	D3		D0	

Character Number (CUSTOMER INPUT)

	MSB			LSB	HEX
R0	□	□	□	□	0 0
R1	⊠	⊠	⊠	⊠	1 F
R2	⊠	□	□	□	1 0
R3	⊠	□	□	□	1 0
R4	⊠	⊠	⊠	□	1 C
R5	⊠	□	□	□	1 0
R6	⊠	□	□	□	1 0
R7	⊠	⊠	⊠	⊠	1 F
	D4	D3		D0	

FIGURE 2 – FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM6670 MOS READ ONLY MEMORY

Customer:

Company _____

Part No. _____

Originator _____

Phone No. _____

Motorola Use Only:

Quote: _____

Part No.: _____

Specif. No.: _____

Chip-Select Options:

	Active High 1	Active Low 0	No-Connect
CS	☐	☐	☐

FIGURE 3 – CARD PUNCH FORMAT

Columns	
1-9	Blank
10-25	Hex coding for first character
26	Slash (/)
27-42	Hex coding for second character
43	Slash (/)
44-59	Hex coding for third character
60	Slash (/)
61-76	Hex coding for fourth character
77-78	Blank
79-80	Card number (starting 01; thru 32)

Column 10 on the first card contains either a zero or a one to program D4 of row R0 for the first character. Column 11 contains the hex character for D3 thru D0. Columns 12 and 13 contain the information to program R1. The entire first character is coded in columns 10 thru 25. Each card contains the coding for four characters; 32 cards are required to program the entire 128 characters. The characters must be programmed in sequence from the first character to the last in order to establish proper addressing for the part. Figure 3 provides an illustration of the correct format.

FIGURE 4 – EXAMPLE OF CARD PUNCH FORMAT
(First 12 Characters of MCM6670P4)

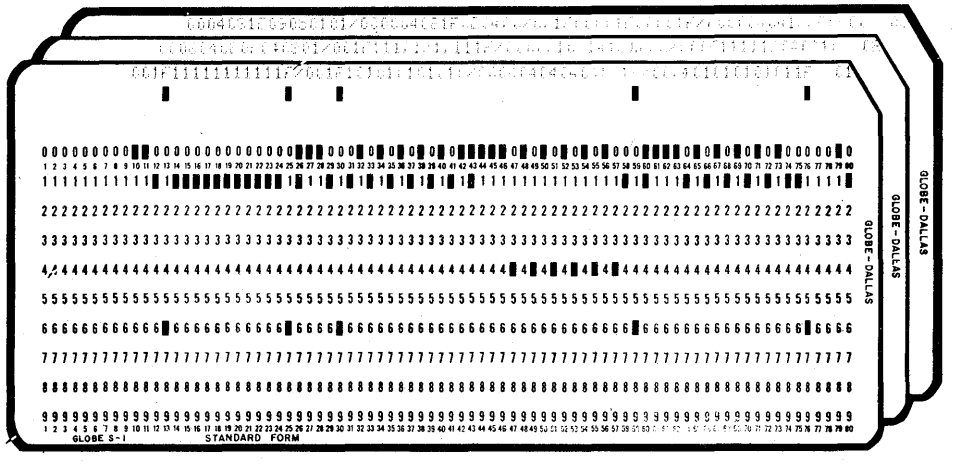


FIGURE 5 – PAPER TAPE FORMAT

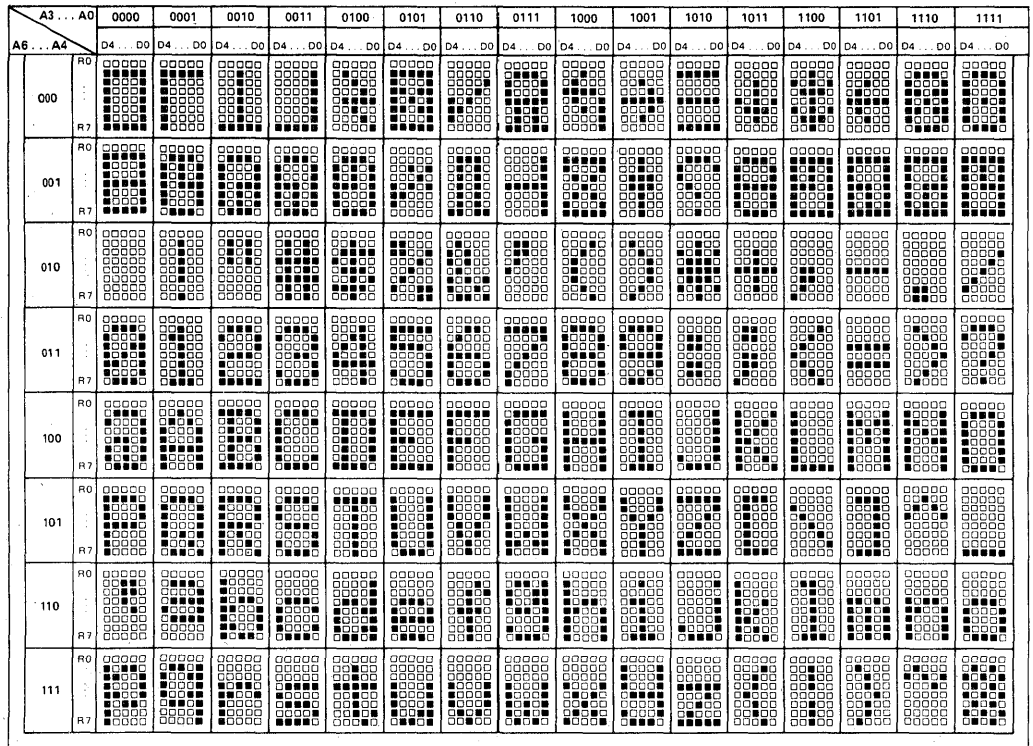
Frames	
Leader	Blank Tape
1 to M	Allowed for customer use (M ≤ 64)
M + 1, M + 2	CR; LF (Carriage Return; Line Feed)
M + 3 to M + 66	First line of pattern information (64 hex figures per line)
M + 67, M + 68	CR; LF
M + 69 to M + 2114	Remaining 31 lines of hex figures, each line followed by a Carriage Return and Line Feed

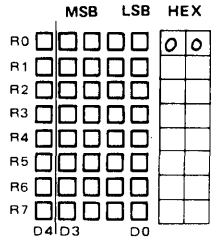
Blank Tape

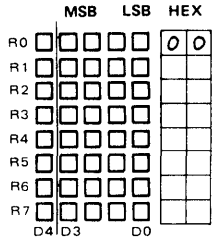
Frames 1 to M are left to the customer for internal identification, where M ≤ 64. Any combination of alphanumerics may be used. This information is terminated with a Carriage Return and Line Feed, delineating the start of data entry. (Note that the tape cannot begin with a CR and/or LF, or the customer identification will be assumed to be programming data.)

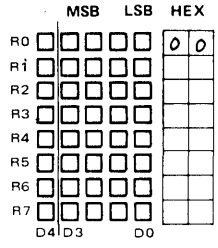
Frame M + 3 contains a zero or a one to program D4 of row R0 for the first character. Frame M + 4 contains the hex character for D3 thru D0, completing the programming information for R0. Frames M + 5 and M + 6 contain the information to program R1. The entire first character is coded in Frames M + 3 thru M + 18. Four complete characters are programmed with each line. A total of 32 lines program all 128 characters (32 x 4). The characters must be programmed in sequence from the first character to the last in order to establish proper addressing for the part.

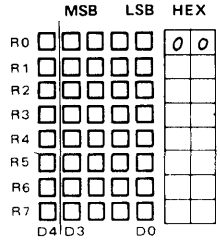
FIGURE 6 – MCM6674 PATTERN

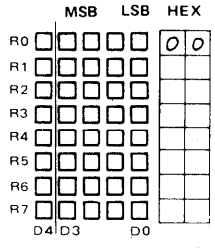


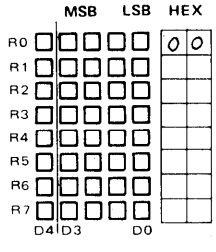


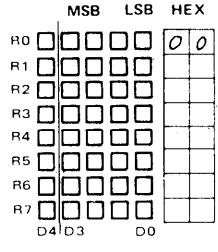


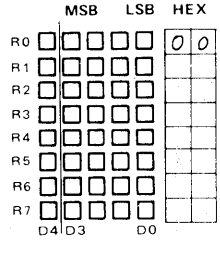


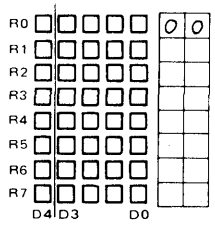


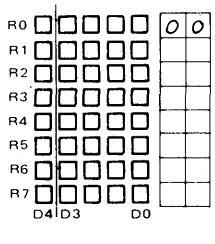


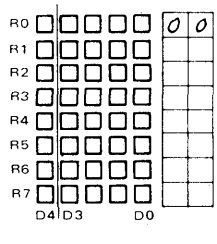


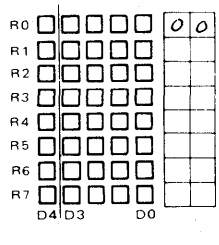


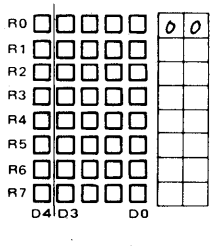


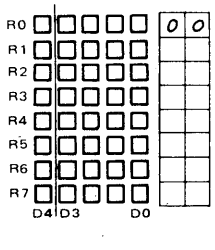


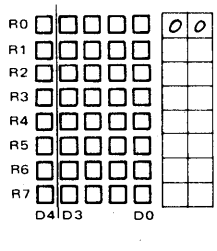


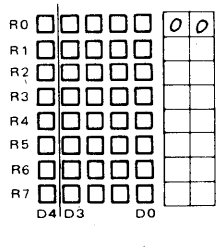












The formats below are given for your convenience in preparing character information for MCM6670 programming. THESE FORMATS ARE NOT TO BE USED TO TRANSMIT THE INFORMATION TO MOTOROLA. Refer to the Custom Programming instructions for detailed procedures.

Character Number ________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

MOTOROLA

MCM66700 MCM66710 MCM66714 MCM66720 MCM66730 MCM66734 MCM66740 MCM66750 MCM66751 MCM66760 MCM66770 MCM66780 MCM66790

2

8192-BIT READ ONLY MEMORIES
ROW SELECT CHARACTER GENERATORS

The MCM66700 is a mask-programmable 8192-bit horizontal-scan (row select) character generator. It contains 128 characters in a 7 X 9 matrix, and has the capability of shifting certain characters that normally extend below the baseline such as j, y, g, p, and q. Circuitry is supplied internally to effectively lower the whole matrix for this type of character—a feature previously requiring external circuitry.

A seven-bit address code is used to select one of the 128 available characters. Each character is defined as a specific combination of logic 1s and 0s stored in a 7 X 9 matrix. When a specific four-bit binary row select code is applied, a word of seven parallel bits appears at the output. The rows can be sequentially selected, providing a nine-word sequence of seven parallel bits per word for each character selected by the address inputs. As the row select inputs are sequentially addressed, the devices will automatically place the 7 X 9 character in one of two preprogrammed positions on the 16-row matrix, with the positions defined by the four row select inputs. Rows that are not part of the character are automatically blanked.

The devices listed are preprogrammed versions of the MCM66700. They contain various sets of characters to meet the requirements of diverse applications. The complete patterns of these devices are contained in this data sheet.

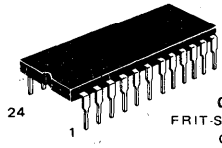
- Fully Static Operation
- Fully TTL Compatible with Three-State Outputs
- CMOS and MPU Compatible, Single ±10% 5 Volt Supply
- Shifted Character Capability
  (Except MCM66720, MCM66730, and MCM66734)
- Maximum Access Time = 350 ns
- 4 Programmable Chip Selects (0, 1, or X)
- Pin-for-Pin Replacement for the MCM6570, Including All Standard Patterns

MOS

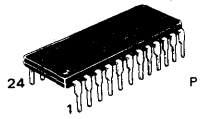
(N-CHANNEL, SILICON-GATE)

8K READ ONLY MEMORIES

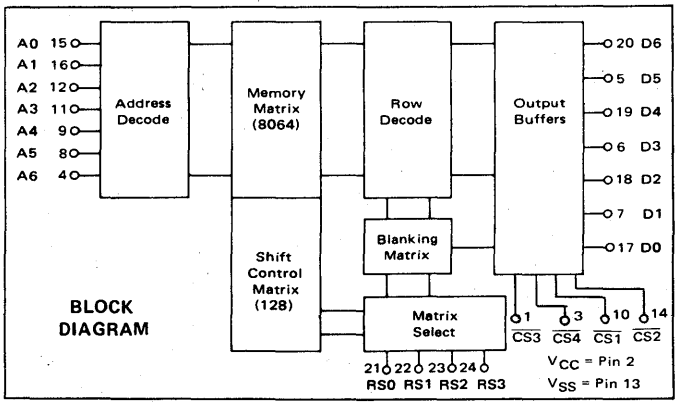
HORIZONTAL-SCAN CHARACTER GENERATORS WITH SHIFTED CHARACTERS



C SUFFIX
FRIT-SEAL PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 709



BLOCK DIAGRAM

PIN ASSIGNMENT

1	CS3	RS3	24
2	V_{CC}	RS2	23
3	CS4	RS1	22
4	A6	RS0	21
5	D5	D6	20
6	D3	D4	19
7	D1	D2	18
8	A5	D0	17
9	A4	A1	16
10	CS1	A0	15
11	A3	CS2	14
12	A2	V_{SS}	13

ABSOLUTE MAXIMUM RATINGS (See Note 1, Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
Supply Voltages	V_{CC}	-0.3 to 7.0	Vdc
Input Voltage	V_{in}	-0.3 to 7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher-than-recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
Input Logic "1" Voltage	V_{IH}	2.0	–	V_{CC}	Vdc
Input Logic "0" Voltage	V_{IL}	-0.3	–	0.8	Vdc

DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 5.5 Vdc, V_{CC} = 4.5 Vdc)	I_{IH}	–	–	2.5	μAdc
Output Low Voltage (Blank) (I_{OL} = 1.6 mAdc)	V_{OL}	0	–	0.4	Vdc
Output High Voltage (Dot) (I_{OH} = -205 μAdc)	V_{OH}	2.4	–	–	Vdc
Power Supply Current	I_{CC}	–	–	80	mAdc
Power Dissipation	P_D	–	200	440	mW

CAPACITANCE (Periodically sampled rather than 100% tested)

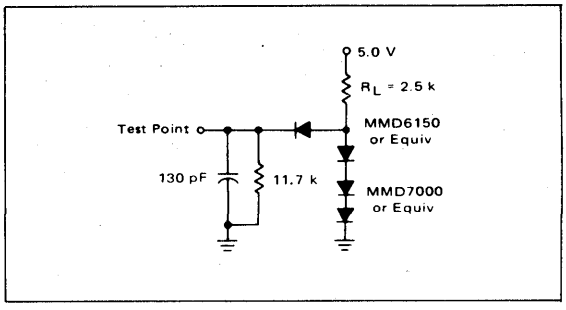
Input Capacitance (f = 1.0 MHz)	C_{in}	–	4.0	7.0	pF
Output Capacitance (f = 1.0 MHz)	C_{out}	–	4.0	7.0	pF

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

AC TEST LOAD



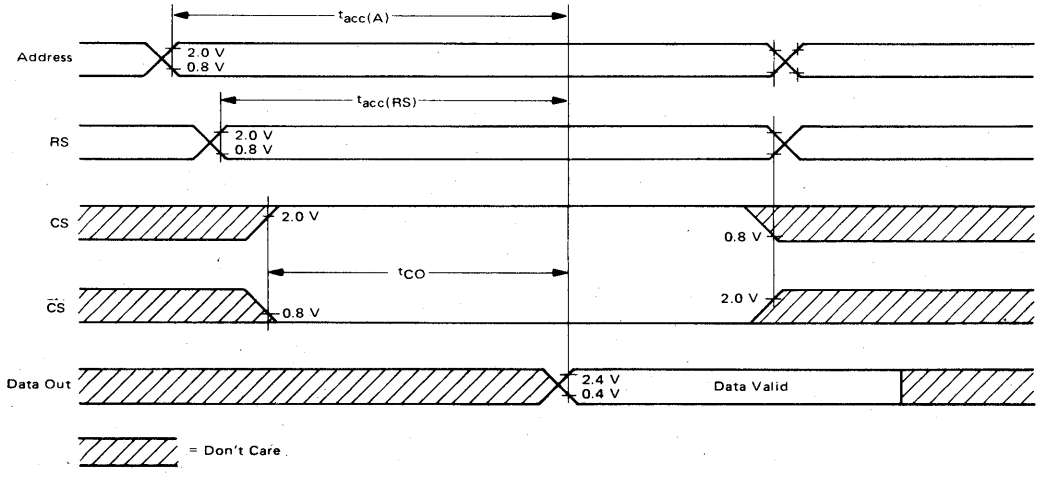
AC TEST CONDITIONS

Condition	Value
Input Pulse Levels	0.8 V to 2.0 V
Input Rise and Fall Times	20 ns
Output Load	1 TTL Gate and C_L = 130 pF

AC CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
Address Access Time	$t_{acc(A)}$	250	350	ns
Row Select Access Time	$t_{acc(RS)}$	250	350	ns
Chip Select to Output Delay	t_{CO}	100	150	ns

TIMING DIAGRAM



MEMORY OPERATION (Using Positive Logic)

Most positive level = 1, most negative level = 0.

Address

To select one of the 128 characters, apply the appropriate binary code to the Address inputs (A0 through A6).

Row Select

To select one of the rows of the addressed character to appear at the seven output lines, apply the appropriate binary code to the Row Select inputs (RS0 through RS3).

Shifted Characters

These devices have the capability of displaying characters that descend below the bottom line (such as lowercase letters j, y, g, p, and q). Internal circuitry effectively drops the whole matrix for this type of character. Any character can be programmed to occupy either of the two positions in a 7 X 16 matrix. (Shifted characters are not available on MCM66720, MCM66730, or MCM66734.)

Output

For these devices, an output dot is defined as a logic 1 level, and an output blank is defined as a logic 0 level.

Programmable Chip Select

The MCM66700 has four Chip Select inputs that can be programmed with a 1, 0, or *don't care* (not connected). A don't care must always be the highest chip select pin or pins. All standard patterns have Don't Care Chip Select—except MCM66751.

DISPLAY FORMAT

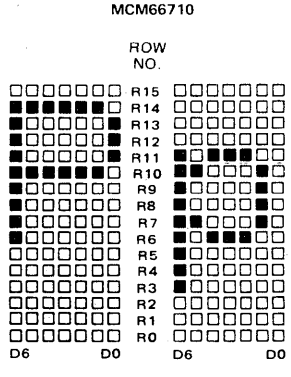
Figure 1 shows the relationship between the logic levels at the row select inputs and the character row at the outputs. The MCM66700 allows the user to locate the basic 7 X 9 font anywhere in the 7 X 16 array. In addition, a shifted font can be placed anywhere in the same 7 X 16 array. For example, the basic MCM66710 font is established in rows R14 through R6. All other rows are automatically blanked. The shifted font is established in rows R11 through R3, with all other rows blanked. Thus, while any one character is contained in a 7 X 9 array, the MCM66710 requires a 7 X 12 array on the CRT screen to contain both normal and descending characters. Other uses of the shift option may require as much as the full 7 X 16 array, or as little as the basic 7 X 9 array (when no shifting occurs, as in the MCM66720).

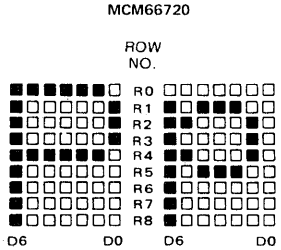
The MCM66700 can be programmed to be scanned either from bottom to top or from top to bottom. This is achieved through the option of assigning row numbers in ascending or descending count, as long as both the basic font and the shifted font are the same. For example, an up counter will scan the MCM66710 from bottom to top, whereas an up counter will scan the MCM66714 from top to bottom (see Figures 7 and 8 for row designation).

FIGURE 1 – ROW SELECT INPUT CODE AND SAMPLE CHARACTERS FOR MCM66710 AND MCM66720

ROW SELECT TRUTH TABLE

RS3	RS2	RS1	RS0	OUTPUT
0	0	0	0	R0
0	0	0	1	R1
0	0	1	0	R2
0	0	1	1	R3
0	1	0	0	R4
0	1	0	1	R5
0	1	1	0	R6
0	1	1	1	R7
1	0	0	0	R8
1	0	0	1	R9
1	0	1	0	R10
1	0	1	1	R11
1	1	0	0	R12
1	1	0	1	R13
1	1	1	0	R14
1	1	1	1	R15





2

CUSTOM PROGRAMMING FOR MCM66700

By the programming of a single photomask, the customer may specify the content of the MCM66700. Encoding of the photomask is done with the aid of a computer to provide quick, efficient implementation of the custom bit pattern while reducing the cost of implementation.

Information for the custom memory content may be sent to Motorola in the following forms, in order of preference:*

1. Hexadecimal coding using IBM Punch Cards (Figures 3 and 4)
2. Hexadecimal coding using ASCII Paper Tape Punch (Figure 5)

Programming of the MCM66700 can be achieved by using the follow sequence:

1. Create the 128 characters in a 7 X 9 font using the format shown in Figure 2. Note that information at output D6 appears in column one, D5 in column two, through D0 information in column seven. The dots filled in and programmed as a logic 1 will appear at the outputs as V_{OH}; the dots left blank will be at V_{OL}. (Blank formats appear at the end of this data sheet for your convenience; they are not to be submitted to Motorola, however.)

2. Indicate which characters are shifted by filling in the extra square (dot) in the top row, at the left (column S).

3. Convert the characters to hexadecimal coding treating dots as 1s and blanks as 0s, and enter this information in the blocks to the right of the character font format. High order bits are at the left, in columns S and D3. For the bottom eight rows, the bit in Column S must be 0, so these locations have been omitted. For the top row, the bit in Column S will be 0 for an unshifted character, and 1 for a shifted character.

4. Transfer the hexadecimal figures either to punched cards (Figure 3) or to paper tape (Figure 5).

5. Assign row numbers to the unshifted font. These must be nine sequential numbers (values 0 through 15) assigned consecutively to the rows. The shifted font is similarly placed in any position in the 16 rows.

6. Provide, in writing, the information indicated in Figure 6 (a copy of Figure 10 may be used for this purpose). Submit this information to Motorola together with the punched cards or paper tape.

FIGURE 2 – CHARACTER FORMAT

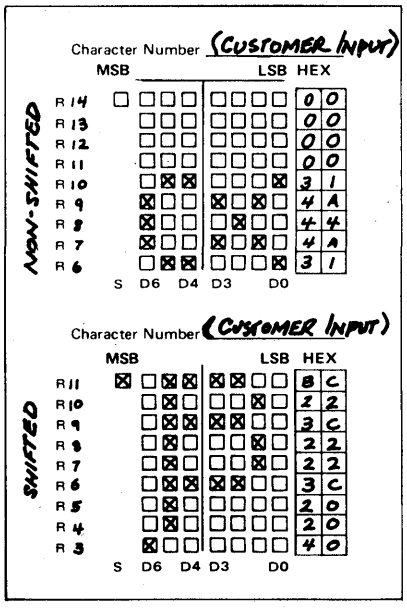


FIGURE 3 – CARD PUNCH FORMAT

Columns	
1 – 10	Blank
11	Asterisk (*)
12 – 29	Hex coding for first character
30	Slash (/)
31 – 48	Hex coding for second character
49	Slash (/)
50 – 67	Hex coding for third character
68	Slash (/)
69 – 76	Blank
77 – 78	Card number (starting 01; through 43)
79 – 80	Blank

Column 12 on the first card contains the hexadecimal equivalent of column S and D6 through D4 for the top row of the first character. Column 13 contains D3 through D0. Columns 14 and 15 contain the information for the next row. The entire first character is coded in columns 12 through 29. Each card contains the coding for three characters. 43 cards are required to program the entire 128 characters, the last card containing only two characters. The characters must be programmed in sequence from the first character to the last in order to establish proper addressing for the part. As an example, the first nine characters of the MCM66710 are correctly coded and punched in Figure 4.

*NOTE: Motorola can accept magnetic tape and truth table formats. For further information contact your local Motorola sales representative.

FIGURE 4 – EXAMPLE OF CARD PUNCH FORMAT
(First 9 Characters of MCM66710)

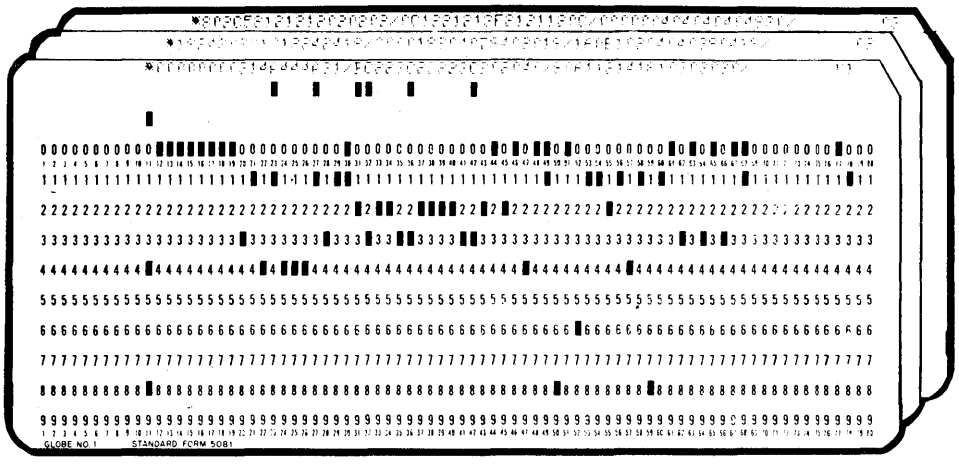


FIGURE 5 – PAPER TAPE FORMAT

Frames	
Leader	Blank Tape
1 to M	Allowed for customer use (M ⩽ 64)
M + 1, M + 2	CR; LF (Carriage Return; Line Feed)
M + 3 to M + 66	First line of pattern information (64 hex figures per line)
M + 67, M + 68	CR; LF
M + 69 to M + 2378	Remaining 35 lines of hex figures, each line followed by a Carriage Return and Line Feed

Blank Tape

Frames 1 to M are left to the customer for internal identification, where M ⩽ 64. Any combination of alphanumerics may be used. This information is terminated with a Carriage Return and Line Feed, delineating the start of data entry. (Note that the tape cannot begin with a CR and/or LF, or the customer identification will be assumed to be programming data.)

Frame M + 3 contains the hexadecimal equivalent of column S and D6 thru D4 for the top row of the first character. Frame M + 4 contains D3 thru D0. Frames M + 5 and M + 6 program the second row of the first character. Frames M + 3 to M + 66 comprise the first line of the printout. The line is terminated with a CR and LF.

The remaining 35 lines of data are punched in sequence using the same format, each line terminated with a CR and LF. The total 36 lines of data contain 36 x 64 or 2304 hex figures. Since 18 hex figures are required to program each 7 x 9 character, the full 128 (2304 ÷ 18) characters are programmed.

FIGURE 6 – FORMAT FOR ORGANIZATIONAL DATA

ORGANIZATIONAL DATA
MCM66700 MOS READ ONLY MEMORY

Customer _____

Customer Part No. _____ Rev. _____

Row Number for top row of non-shifted font _____

Row Number for bottom row of non-shifted font _____

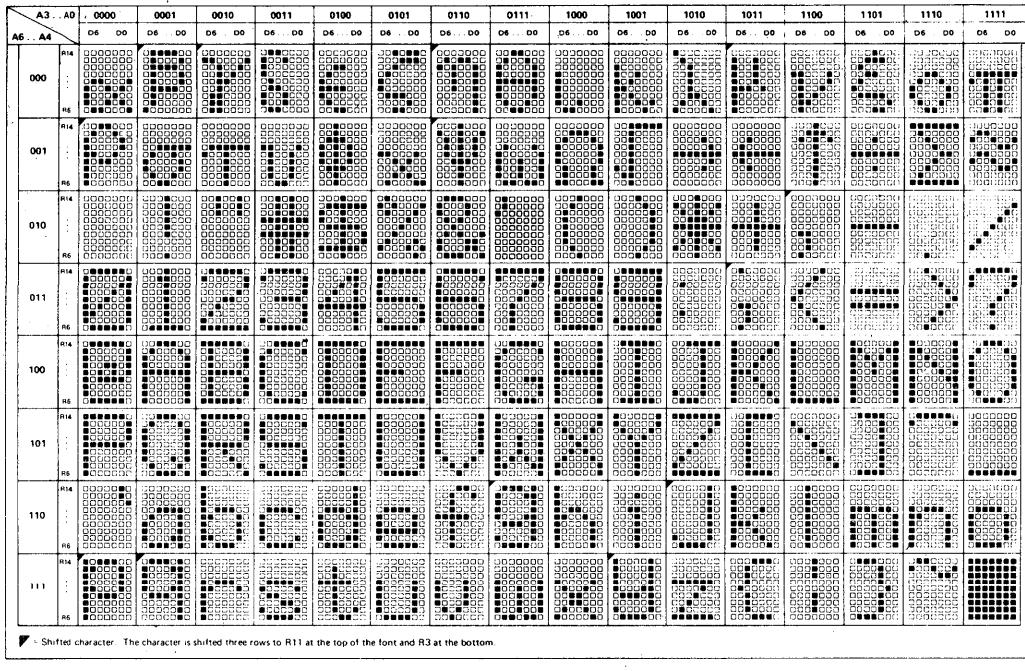
Row Number for top row of shifted font _____

Programmable Chip Select information: 1 = Active High 0 = Active Low X = Don't Care (Not Connected)

CS1___ CS2___ CS3___ CS4___

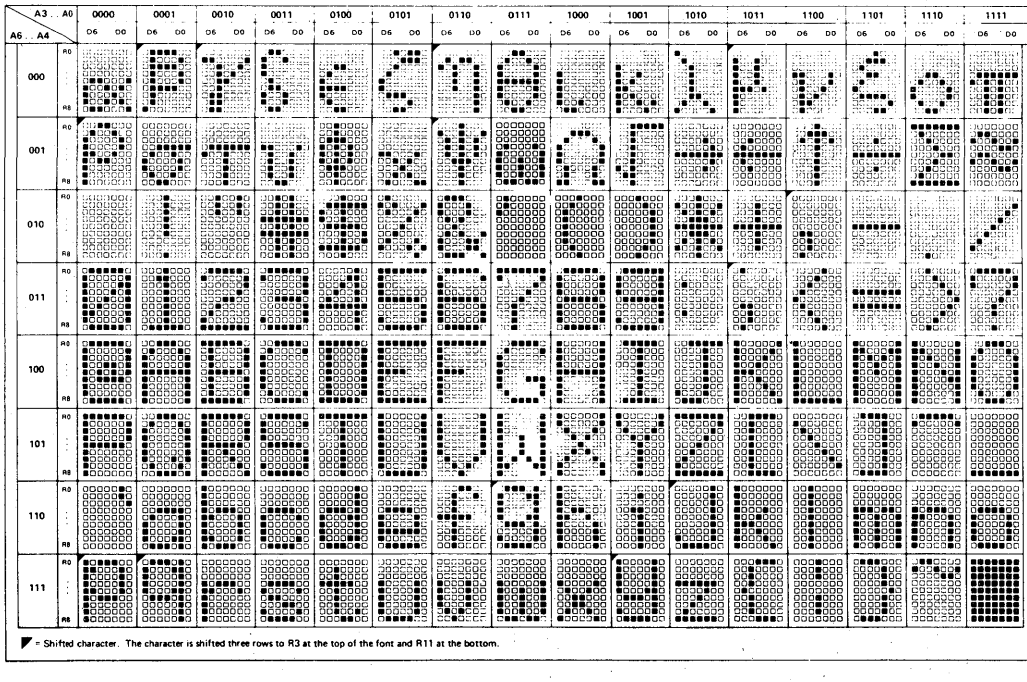
2

FIGURE 7 – MCM66710 PATTERN



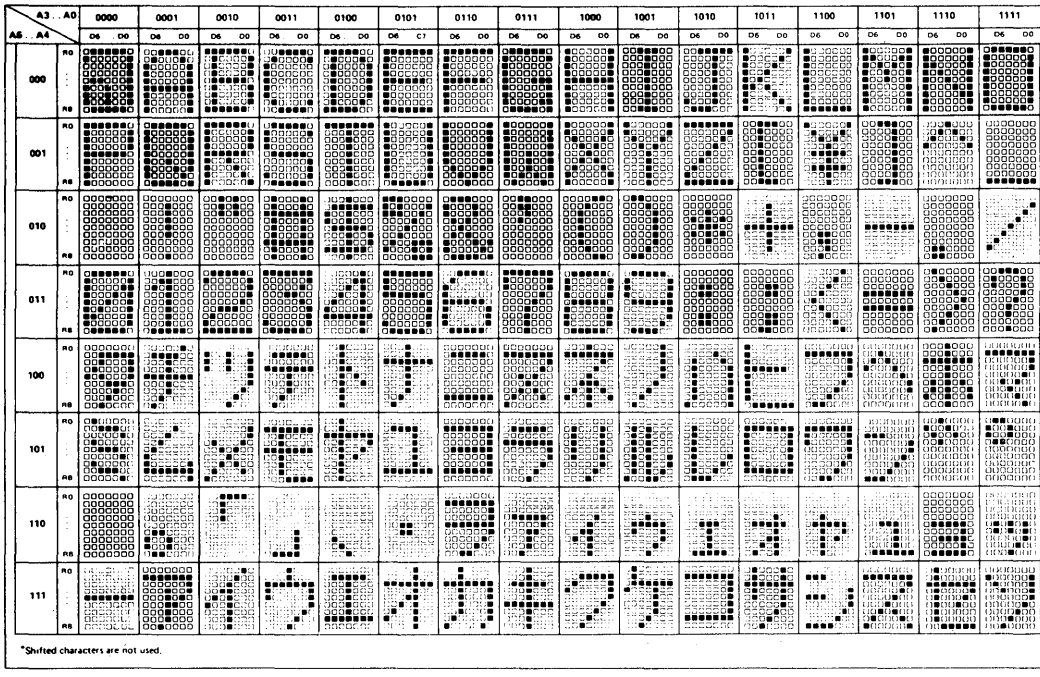
◤ = Shifted character. The character is shifted three rows to R11 at the top of the font and R3 at the bottom.

FIGURE 8 – MCM66714 PATTERN



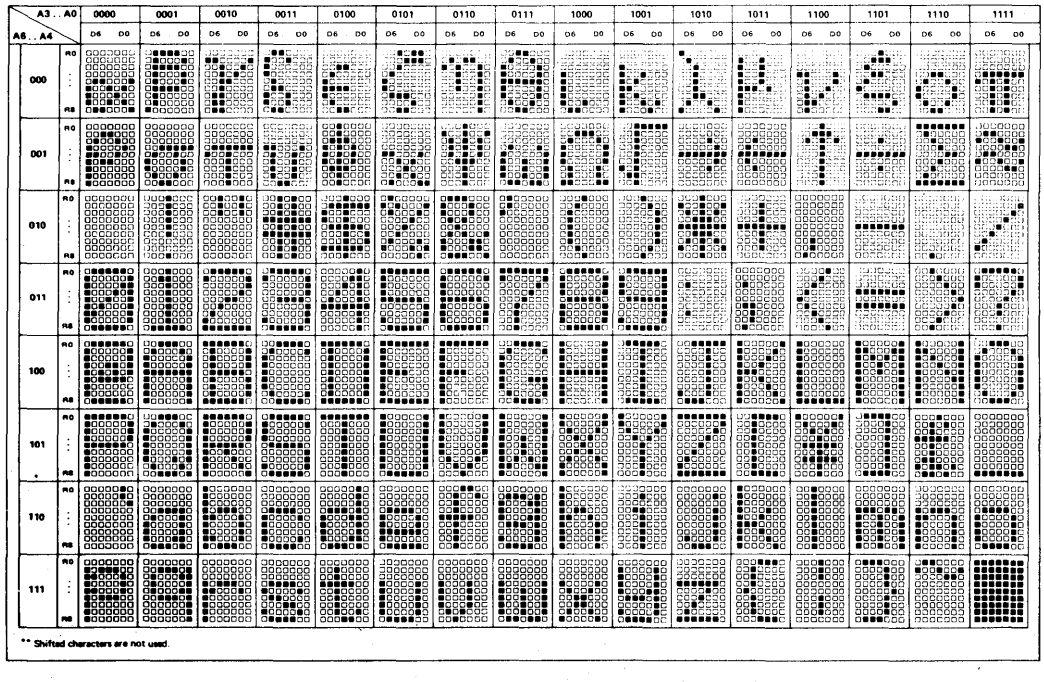
◤ = Shifted character. The character is shifted three rows to R3 at the top of the font and R11 at the bottom.

FIGURE 9 – MCM66734 PATTERN*



*Shifted characters are not used.

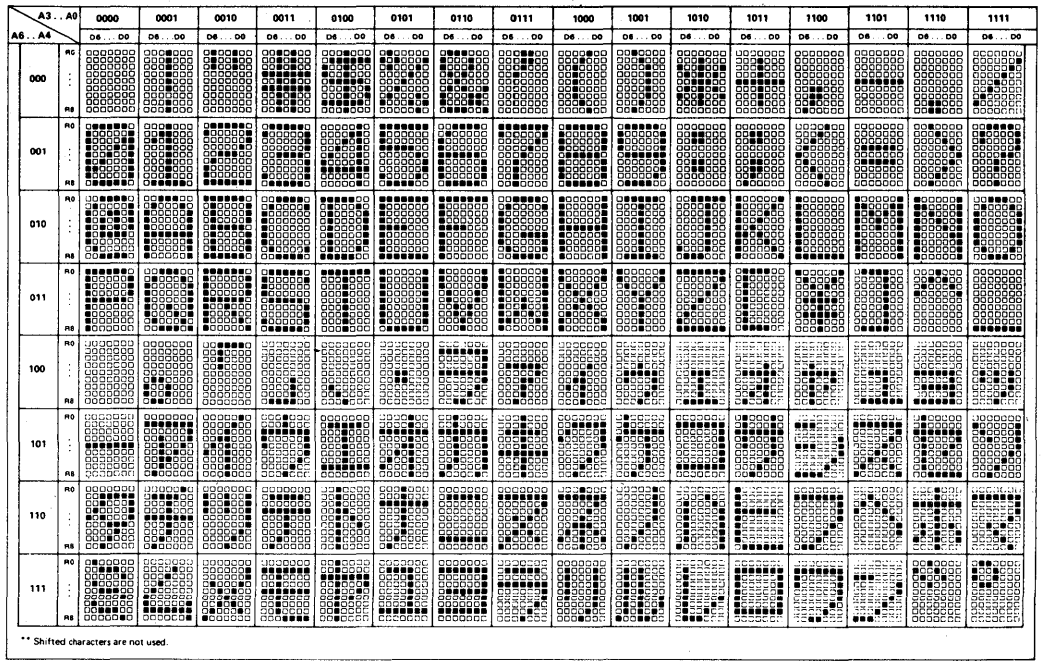
FIGURE 10 – MCM66720 PATTERN**



** Shifted characters are not used.

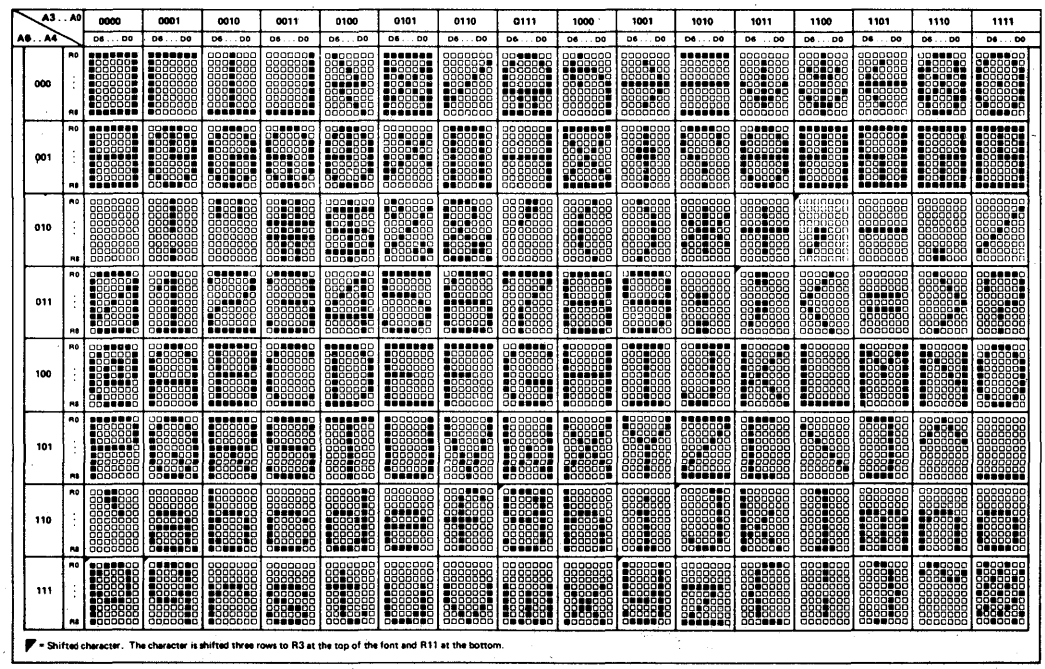
2

FIGURE 11 – MCM66730 PATTERN**



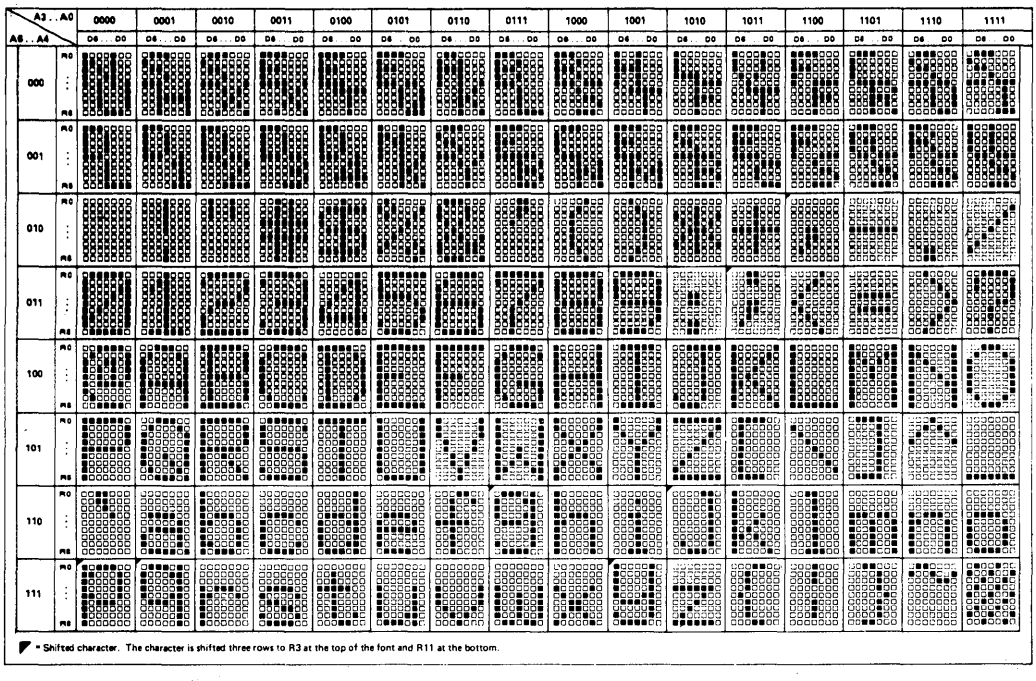
** Shifted characters are not used.

FIGURE 12 – MCM66740 PATTERN



◤ = Shifted character. The character is shifted three rows to R3 at the top of the font and R11 at the bottom.

FIGURE 13 – MCM66750 PATTERN



MCM66751 – Same as MCM66750 except CS1 = 0, CS2 = 0, CS3 = X, and CS4 = X.

FIGURE 14 – MCM66760 PATTERN

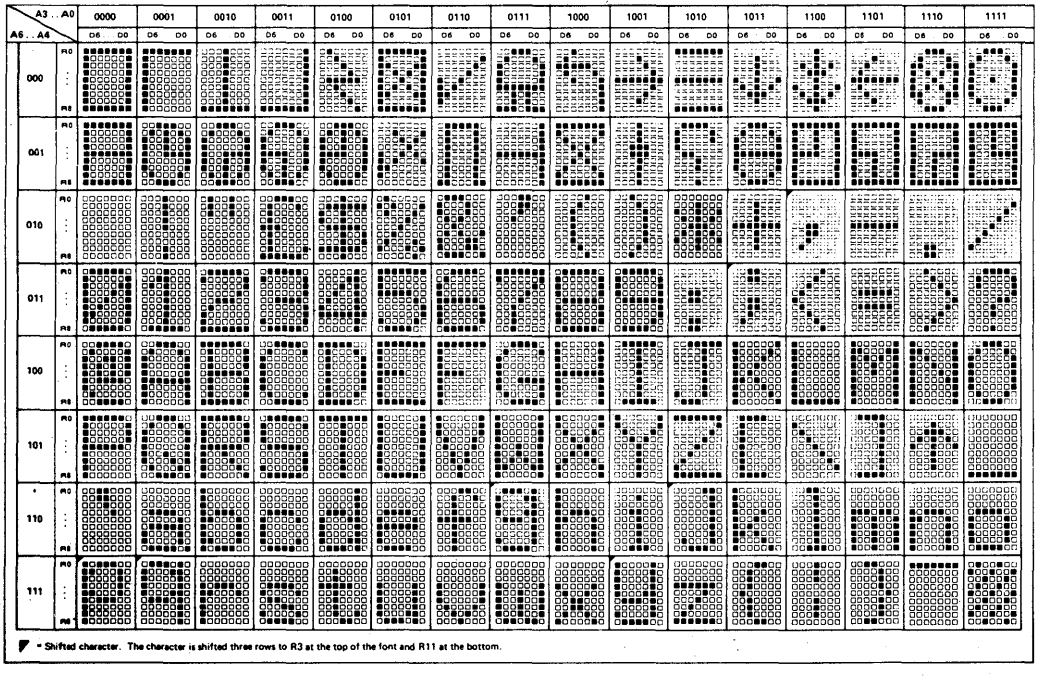


FIGURE 15 – MCM66770 PATTERN

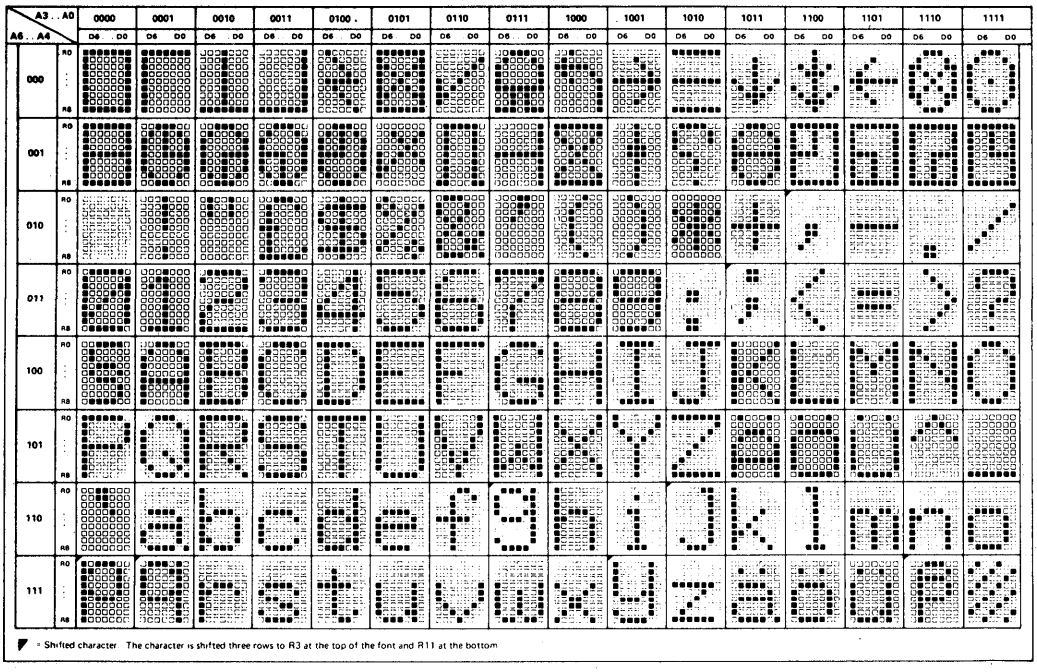


FIGURE 16 – MCM66780 PATTERN

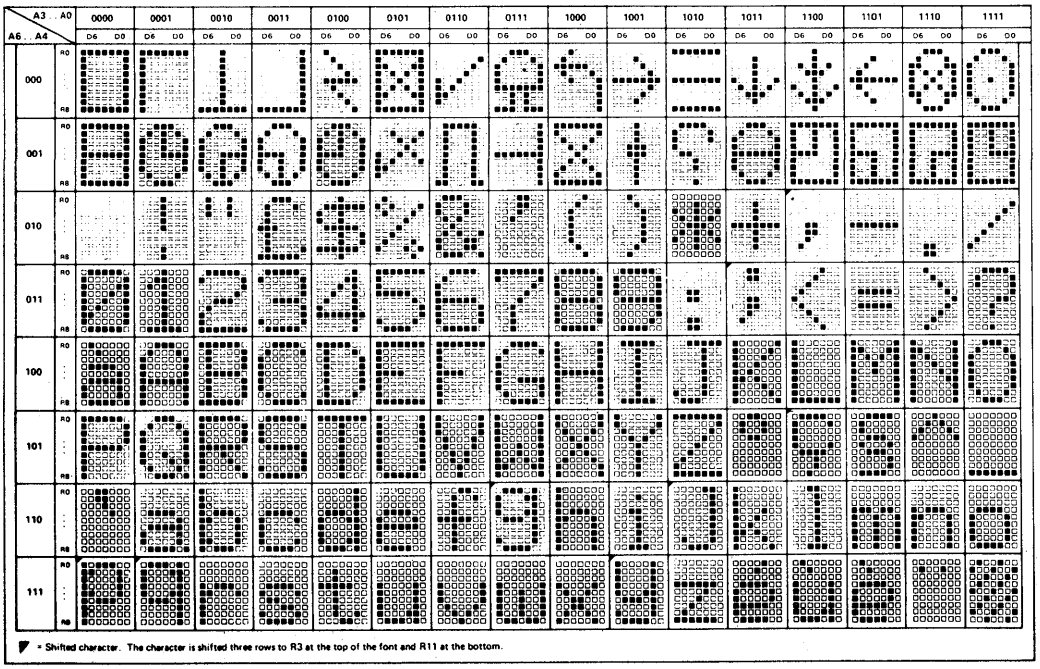
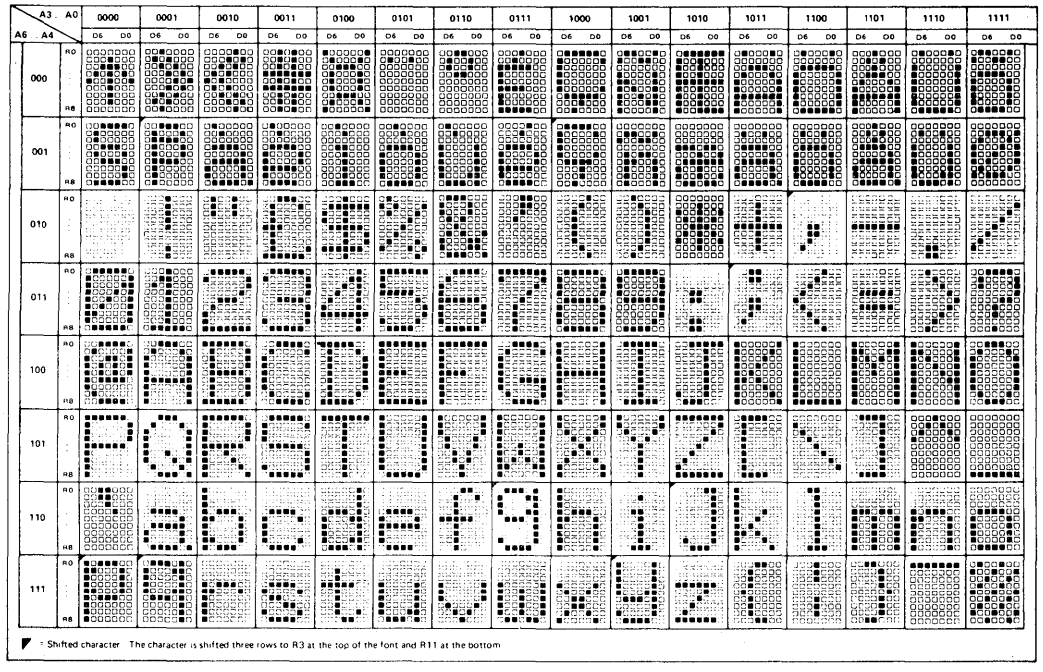


FIGURE 17 – MCM66790 PATTERN

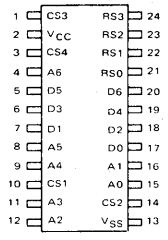


◤ = Shifted character. The character is shifted three rows to R3 at the top of the font and R11 at the bottom

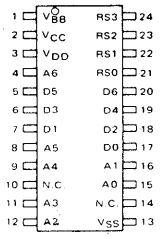
2

MCM6570 Series	MCM66700 Equivalent	Description
MCM6571	MCM66710	ASCII, shifted
MCM6571A	MCM66714	ASCII, shifted
MCM6572	MCM66720	ASCII
MCM6573	MCM66730	Japanese
MCM6573A	MCM66734	Japanese
MCM6574	MCM66740	Math Symbols
MCM6575	MCM66750	Alphanumeric Control
MCM6576	MCM66760	British, shifted
MCM6577	MCM66770	German, shifted
MCM6578	MCM66780	French, shifted
MCM6579	MCM66790	European, shifted

MCM66700 Series Pin Assignment



MCM6570 Series Pin Assignment

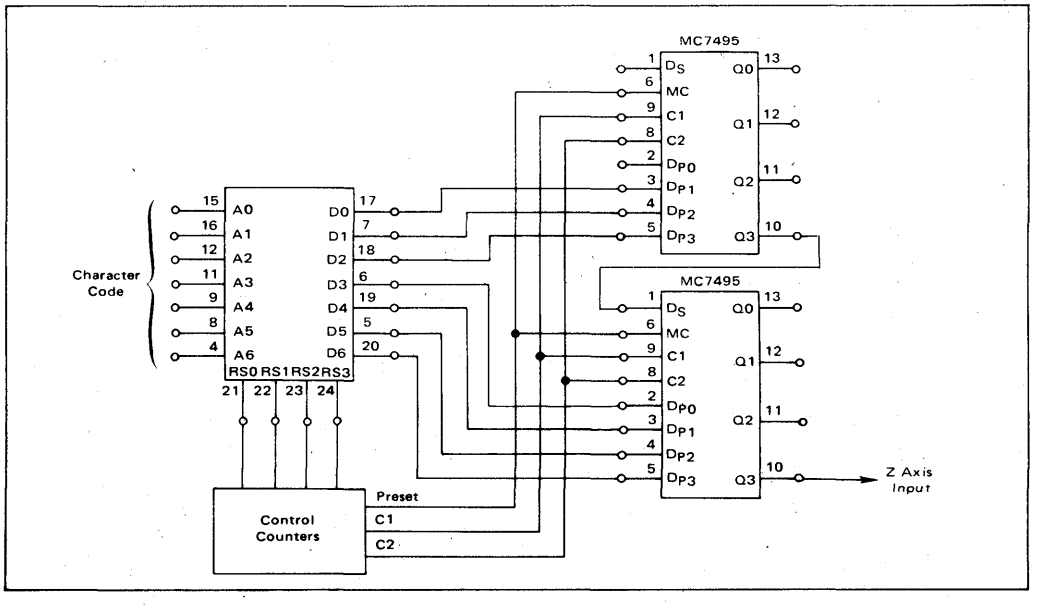


APPLICATIONS INFORMATION

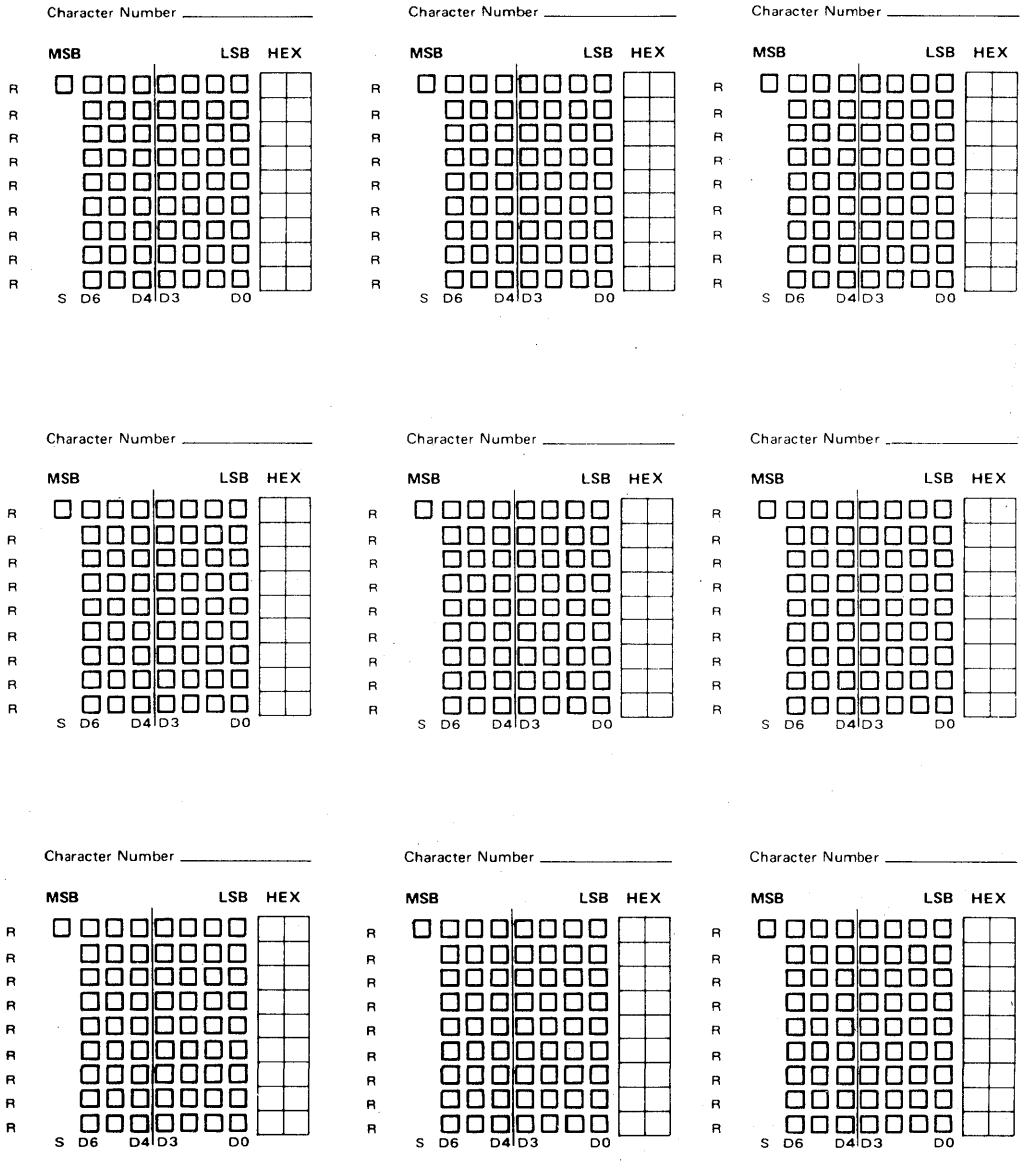
One important application for the MCM66700 series is in CRT display systems (Figure 18). A set of buffer shift registers or random access memories applies a 7-bit character code to the input of the character generator, which then supplies one row of the character according to the count at the four row select inputs. As each row is available, it is put into the TTL MC7495 shift registers. The parallel information in these shift registers is clocked serially out to the Z-axis where it modulates the raster to form the character.

The MCM66700 series require one power supply of +5.0 volts. When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit spikes or glitches on their outputs when the ac power is switched on and off.

FIGURE 18 – CRT DISPLAY APPLICATION USING MCM66710



The formats below are given for your convenience in preparing character information for MCM66700 programming. **THESE FORMATS ARE NOT TO BE USED TO TRANSMIT THE INFORMATION TO MOTOROLA.** Refer to the Custom Programming instructions for detailed procedures.



MOTOROLA

MCM68A30A
MCM68B30A

MOS

(N-CHANNEL, SILICON-GATE)

1024 X 8-BIT
READ ONLY MEMORY

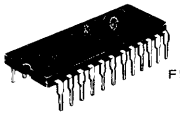
2

1024 X 8-BIT READ ONLY MEMORY

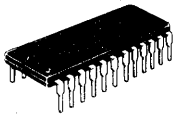
The MCM68A30A/MCM68B30A are mask-programmable byte-organized memories designed for use in bus-organized systems. They are fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of static operation.

The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. Memory expansion is provided through multiple Chip Select inputs. The active level of the Chip Select inputs and the memory content are defined by the customer.

- Organized as 1024 Bytes of 8 Bits
- Static Operation
- Three-State Data Output
- Four Chip Select Inputs (Programmable)
- Single ±10% 5-Volt Power Supply
- TTL Compatible
- Maximum Access Time = 350 ns – MCM68A30A
  250 ns – MCM68B30A

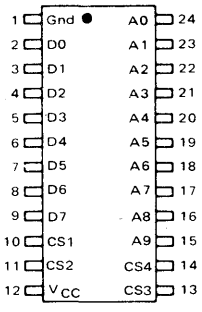


C SUFFIX
FRIT-SEAL PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 709

PIN ASSIGNMENT

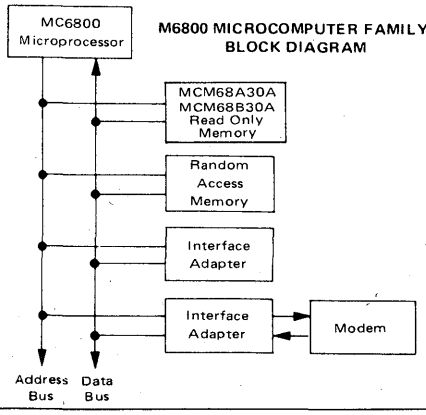


ABSOLUTE MAXIMUM RATINGS (See Note 1)

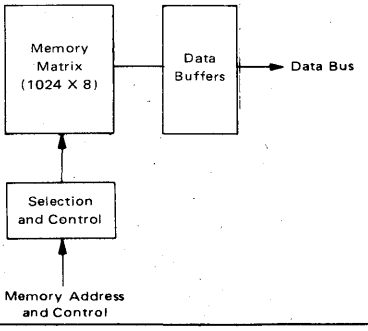
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

M6800 MICROCOMPUTER FAMILY
BLOCK DIAGRAM



MCM68A30A/MCM68B30A READ ONLY
MEMORY BLOCK DIAGRAM



DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
Input High Voltage	V_{IH}	2.0	-	5.5	Vdc
Input Low Voltage	V_{IL}	-0.3	-	0.8	Vdc

DC CHARACTERISTICS

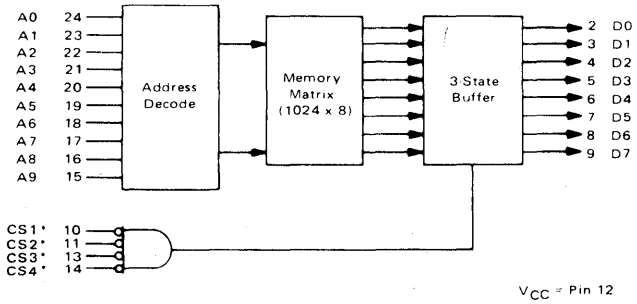
Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	-	-	2.5	μAdc
Output High Voltage (I_{OH} = -205μA)	V_{OH}	2.4	-	-	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	-	-	0.4	Vdc
Output Leakage Current (Three-State) (CS = 0.8 V or $\overline{CS}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	-	-	10	μAdc
Supply Current (V_{CC} = 5.5 V, T_A = 0°C)	I_{CC}	-	-	130	mAdc

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	7.5	pF
Output Capacitance	C_{out}	12.5	pF

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

BLOCK DIAGRAM



*Active level defined by the customer.

V_{CC} = Pin 12
Gnd = Pin 1

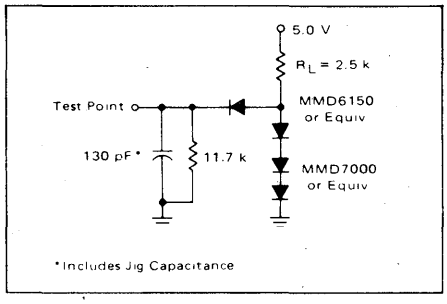
AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.)

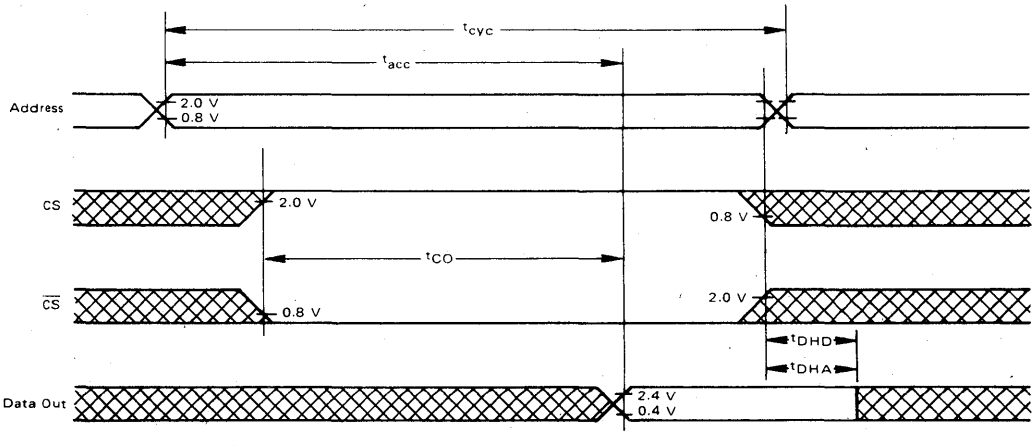
(All timing with $t_r = t_f = 20$ ns, Load of Figure 1)

Characteristic	Symbol	MCM68A30AL		MCM68B30AL		Unit
		Min	Max	Min	Max	
Cycle Time	t_{cyc}	350	–	250	–	ns
Access Time	t_{acc}	–	350	–	250	ns
Chip Select to Output Delay	t_{CO}	–	150	–	125	ns
Data Hold from Address	t_{DHA}	10	–	10	–	ns
Data Hold from Deselection	t_{DHD}	10	150	10	125	ns

FIGURE 1 – AC TEST LOAD



TIMING DIAGRAM



CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68A30A/MCM68B30A, the customer may specify the content of the memory and the method of enabling the outputs.

Information on the general options of the MCM68A30A/MCM68B30A should be submitted on an Organizational Data form such as that shown in Figure 3. ("No Connect" must always be the highest order Chip Select pin(s).)

Information for custom memory content may be sent to Motorola in one of four forms (shown in order of preference):

1. Paper tape output of the Motorola M6800 Software.
2. Hexadecimal coding using IBM Punch Cards.
3. EPROM (MCM2708, MCM27A08, or MCM68708).
4. Hand-punched paper tape (Figure 3).

PAPER TAPE

Included in the software packages developed for the M6800 Microcomputer Family is the ability to produce a paper tape output for computerized mask generation. The assembler directives are used to control allocation of memory, to assign values for stored data, and for controlling the assembly process. The paper tape must specify the full 1024 bytes.

FIGURE 2 – BINARY TO HEXADECIMAL CONVERSION

Binary Data				Hexadecimal Character
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

IBM PUNCH CARDS

The hexadecimal equivalent (from Figure 2) may be placed on 80 column IBM punch cards as follows.

Step	Column	
1	12	Byte "0" Hexadecimal equivalent for outputs D7 thru D4 (D7 = M.S.B.)
2	13	Byte "0" Hexadecimal equivalent for outputs D3 thru D0 (D3 = M.S.B.)
3	14-75	Alternate steps 1 and 2 for consecutive bytes.
4	77-80	Card number (starting 0001)

FIGURE 3 – HAND-PUNCHED PAPER TAPE FORMAT

Frames	
Leader	Blank Tape
1 to M	Allowed for customer use (M ≤ 64)
M + 1, M + 2	CR; LF (Carriage Return; Line Feed)
M + 3 to M + 66	First line of pattern information (64 hex figures per line)
M + 67, M + 68	CR; LF
M + 69 to M + 2112	Remaining 31 lines of hex figures, each line followed by a Carriage Return and Line Feed

Blank Tape

Frames 1 to M are left to the customer for internal identification, where M ≤ 64. Any combination of alphanumerics may be used. This information is terminated with a Carriage Return and Line Feed, delineating the start of data entry. (Note that the tape cannot begin with a CR and/or LF, or the customer identification will be assumed to be programming data.)

Option A (1024 x 8)

Frame M + 3 contains the hexadecimal equivalent of bits D7 thru D4 of byte 0. Frame M + 4 contains bits D3 thru D0. These two hex figures together program byte 0. Likewise, frames M + 5 and M + 6 program byte 1, while M + 7 and M + 8 program byte 2. Frames M + 3 to M + 66 comprise the first line of the printout and program, in sequence, the first 32 bytes of storage. The line is terminated with a CR and LF.

Option B (2048 x 4)

Frame M + 3 contains the hexadecimal equivalent of byte 0, bits D3 thru D0. Frame M + 4 contains byte 1, frame M + 5 byte 2, and so on. Frames M + 3 to M + 66 sequentially program bytes 0 to 31 (the first 32 bytes). The line is terminated with a CR and LF.

Both Options

The remaining 31 lines of data are punched in sequence using the same format, each line terminated with a CR and LF. The total 32 lines of data contain 32 x 64 or 2048 characters. Since each character programs 4 bits of information, a full 8192 bits are programmed.

As an example, a printout of the punched tape for Figure 13 would read as shown in Figure 10 (a CR and LF is implicit at the end of each line).

FIGURE 4 – FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM68A30A/68B30A MOS READ ONLY MEMORY

Customer:

Company _____

Part No. _____

Originator _____

Phone No. _____

Motorola Use Only:

Quote: _____

Part No.: _____

Specif. No.: _____

Chip Select Options:

	Active High	Active Low	No Connect "Don't Care"
CS1	☐	☐	☐
CS2	☐	☐	☐
CS3	☐	☐	☐
CS4	☐	☐	☐

MOTOROLA

MCM68A308
MCM68B308

MOS

(N-CHANNEL, SILICON-GATE)

1024 X 8-BIT READ ONLY MEMORY

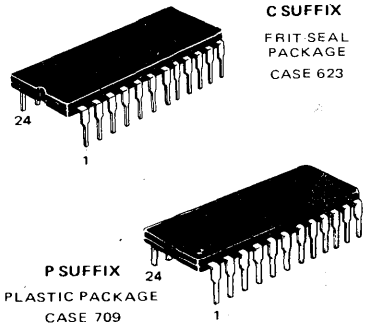
2

1024 X 8-BIT READ ONLY MEMORY

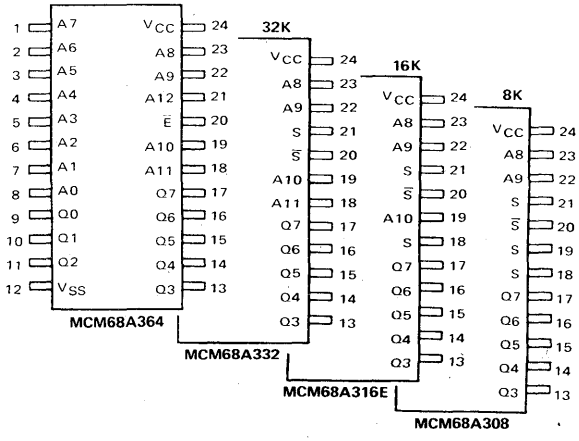
The MCM68A308/MCM68B308 is a mask-programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of static operation.

The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. Memory expansion is provided through multiple Chip Select inputs. The active level of the Chip Select inputs and the memory content are defined by the customer.

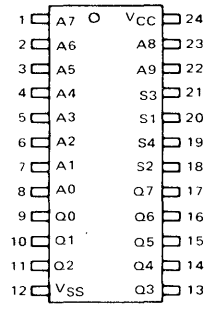
- Organized as 1024 Bytes of 8 Bits
- Static Operation
- Three-State Data Output
- Mask-Programmable Chip Selects for Simplified Memory Expansion
- Single ±10% 5-Volt Power Supply
- TTL Compatible
- Maximum Access Time = 350 ns – MCM68A308
  250 ns – MCM68B308
- 350 mW Typical Power Dissipation



MOTOROLA'S PIN COMPATIBLE ROM FAMILY
(Industry Standard Pinouts)



PIN ASSIGNMENT



PIN NAMES	
A0–A9	Address Inputs
S1–S4	Chip Selects
Q0–Q7	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

2

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
Input High Voltage	V_{IH}	2.0	–	5.5	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.8	Vdc

DC CHARACTERISTICS

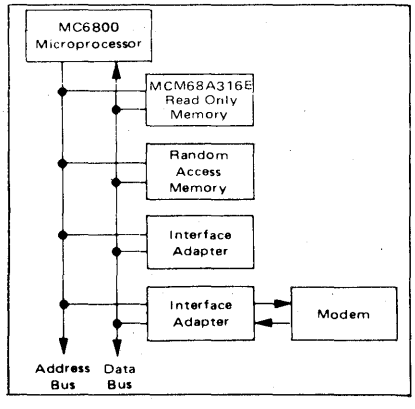
Characteristic	Symbol	Min	Max	Unit
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	–	2.5	μAdc
Output High Voltage (I_{OH} = -205 μA)	V_{OH}	2.4	–	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	0.4	Vdc
Output Leakage Current (Three-State) (S = 0.8 V or $\overline{S}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	–	10	μAdc
Supply Current (V_{CC} = 5.5 V, T_A = 0°C)	I_{CC}	–	130	mAdc

ABSOLUTE MAXIMUM RATINGS (See Note 1)

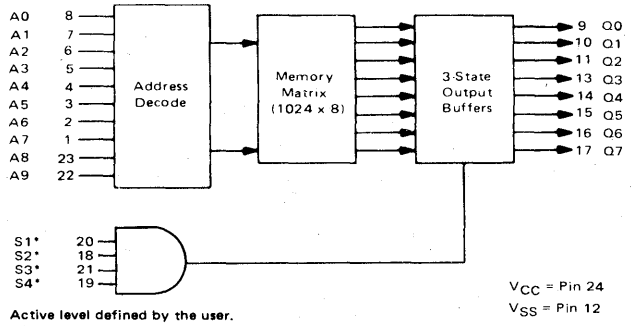
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM



BLOCK DIAGRAM



* Active level defined by the user.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.
All timing with $t_r = t_f = 20$ ns, Load of Figure 1)

Characteristic	Symbol	MCM68A308		MCM68B308		Unit
		Min	Max	Min	Max	
Cycle Time	t_{cyc}	350	–	250	–	ns
Access Time	t_{acc}	–	350	–	250	ns
Chip Select to Output Delay	t_{SO}	–	150	–	150	ns
Data Hold from Address	t_{DHA}	10	–	10	–	ns
Data Hold from Deselection	t_{DHD}	10	150	10	150	ns

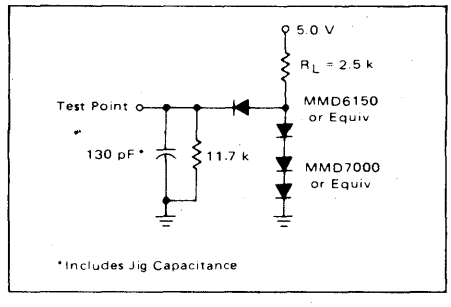
CAPACITANCE

($f = 2.0$ MHz, $T_A = 25^oC$, periodically sampled rather than 100% tested)

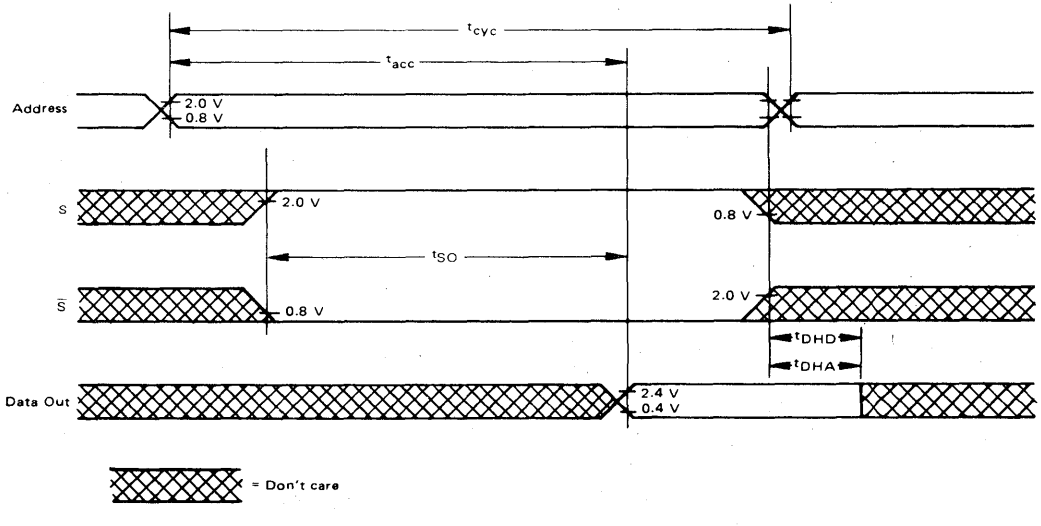
Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	7.5	pF
Output Capacitance	C_{out}	12.5	pF

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

FIGURE 1 – AC TEST LOAD



TIMING DIAGRAM



2

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68A308/MCM68B308, the customer may specify the content of the memory and the method of enabling the outputs. (A "no-connect" must always be the highest order chip-select(s).)

Information on the general options of the MCM68A308/MCM68B308 should be submitted on an Organizational Data form such as that shown in Figure 4.

Information for customer memory content may be sent to Motorola in one of four forms (shown in order of preference):

1. Paper tape output of the Motorola M6800 Software.
2. Hexadecimal coding using IBM Punch Cards.
3. EPROM one MCM68A708 or equivalent.
4. Hand punched paper tape (Figure 3).

PAPER TAPE

Included in the software packages developed for the M6800 Microcomputer Family is the ability to produce a paper tape output for computerized mask generation. The assembler directives are used to control allocation of memory, to assign values for stored data, and for controlling the assembly process. The paper tape must specify the full 1024 bytes.

FIGURE 2 – BINARY TO HEXADECIMAL CONVERSION

Binary Data				Hexadecimal Character
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

IBM PUNCH CARDS

The hexadecimal equivalent (from Figure 2) may be placed on 80 column IBM punch cards as follows:

Step	Column	
1	12	Byte "0" Hexadecimal equivalent for outputs Q7 thru Q4 (Q7 = M.S.B.)
2	13	Byte "0" Hexadecimal equivalent for outputs Q3 thru Q0 (Q3 = M.S.B.)
3	14–75	Alternate steps 1 and 2 for consecutive bytes.
4	77–80	Card number (starting 0001)

FIGURE 3 – HAND-PUNCHED PAPER TAPE FORMAT

Frames	
Leader	Blank Tape
1 to M	Allowed for customer use ($M \leqslant 64$)
M + 1, M + 2	CR; LF (Carriage Return; Line Feed)
M + 3 to M + 66	First line of pattern information (64 hex figures per line)
M + 67, M + 68	CR; LF
M + 69 to M + 2112	Remaining 31 lines of hex figures, each line followed by a Carriage Return and Line Feed

Blank Tape

Frames 1 to M are left to the customer for internal identification, where $M \leqslant 64$. Any combination of alphanumerics may be used. This information is terminated with a Carriage Return and Line Feed, delineating the start of data entry. (Note that the tape cannot begin with a CR and/or LF, or the customer identification will be assumed to be programming data.)

Frame M + 3 contains the hexadecimal equivalent of bits Q7 thru Q4 of byte 0. Frame M + 4 contains bits Q3 thru Q0. These two hex figures together program byte 0. Likewise, frames M + 5 and M + 6 program byte 1, while M + 7 and M + 8 program byte 2. Frames M + 3 to M + 66 comprise the first line of the printout and program, in sequence, the first 32 bytes of storage. The line is terminated with a CR and LF.

The remaining 31 lines of data are punched in sequence using the same format, each line terminated with a CR and LF. The total 32 lines of data contain 32 x 64 or 2048 characters. Since each character programs 4 bits of information, a full 8192 bits are programmed.

FIGURE 4 – FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM68308 MOS READ ONLY MEMORY

Customer:

Company _____

Part No. _____

Originator _____

Phone No. _____

Motorola Use Only:

Quote: _____

Part No.: _____

Specif. No.: _____

Chip Select:

	Active High	Active Low	No Connect
S1	☐	☐	☐
S2	☐	☐	☐
S3	☐	☐	☐
S4	☐	☐	☐

MOTOROLA

MCM68A316A

MOS

(N-CHANNEL, SILICON-GATE)

2048 X 8-BIT
READ ONLY MEMORY

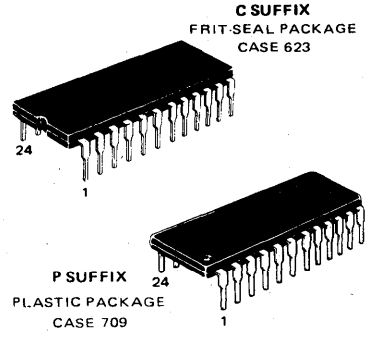
2

2048 X 8-BIT READ ONLY MEMORY

The MCM68A316A is a mask-programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of fully static operation.

The memory is compatible with the M6800 Microcomputer Family, providing read-only storage in byte increments. Memory expansion is provided through multiple Chip Select inputs. The active level of the Chip Select inputs and the memory content are defined by the user.

- Fully Static Operation
- Three-State Data Output
- Mask-Programmable Chip Selects for Simplified Memory Expansion
- Single ±10% 5-Volt Power Supply
- TTL Compatible
- Maximum Access Time = 350 ns
- Plug-in Compatible with 2316A

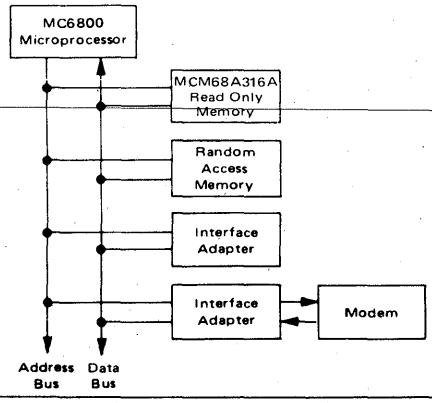


ABSOLUTE MAXIMUM RATINGS (See Note 1)

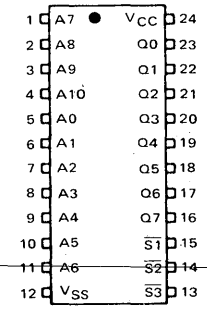
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES	
A0–A10	Address Inputs
S1–S3	Chip Selects
Q0–Q7	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
Input High Voltage	V_{IH}	2.0	–	5.5	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.8	Vdc

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	–	2.5	μAdc
Output High Voltage (I_{OH} = -205 μA)	V_{OH}	2.4	–	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	0.4	Vdc
Output Leakage Current (Three-State) (S = 0.8 V or $\overline{S}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	–	10	μAdc
Supply Current (V_{CC} = 5.5 V, T_A = 0°C)	I_{CC}	–	130	mAdc

CAPACITANCE

(f = 2.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	7.5	pF
Output Capacitance	C_{out}	12.5	pF

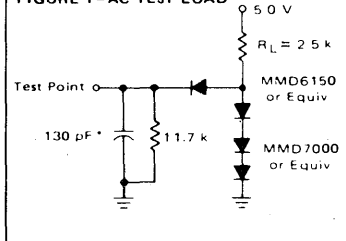
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

AC OPERATING CONDITIONS AND CHARACTERISTICS

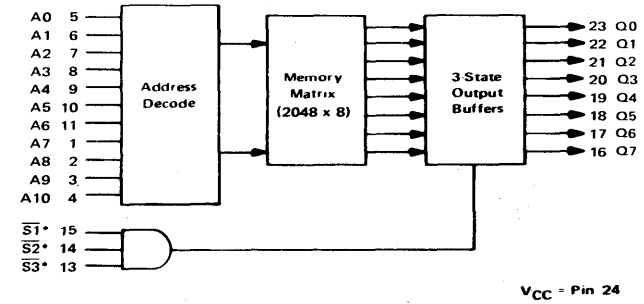
(Full operating voltage and temperature unless otherwise noted.
All timing with $t_r = t_f$ = 20 ns, Load of Figure 1)

Characteristic	Symbol	Min	Max	Unit
Cycle Time	t_{cyc}	350	–	ns
Access Time	t_{acc}	–	350	ns
Chip Select to Output Delay	t_{SO}	–	150	ns
Data Hold from Address	t_{DHA}	10	–	ns
Data Hold from Deselection	t_H	10	150	ns

FIGURE 1 – AC TEST LOAD



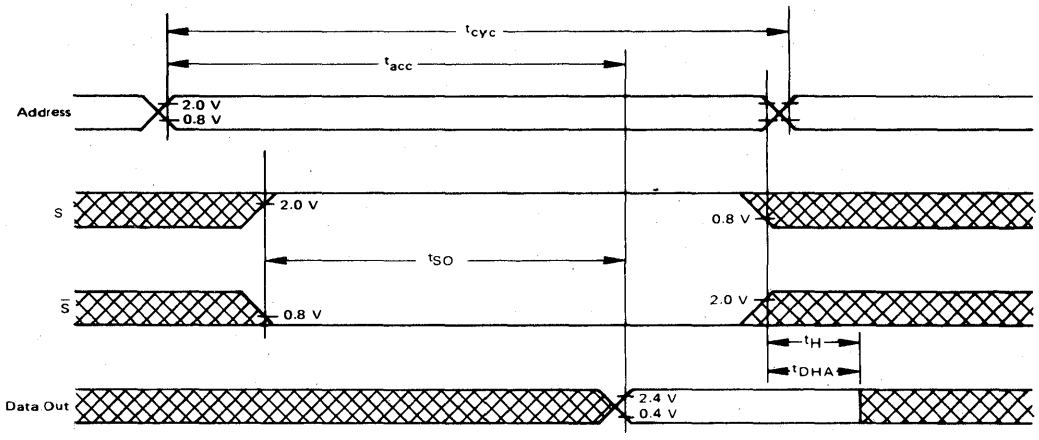
BLOCK DIAGRAM



* Active level defined by the user.

V_{CC} = Pin 24
V_{SS} = Pin 12

TIMING DIAGRAM



CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68316A, the customer may specify the content of the memory and the method of enabling the outputs.

Information on the general options of the MCM68A316A should be submitted on an Organizational Data form such as that shown in Figure 3.

Information for custom memory content may be sent to Motorola in one of four forms (shown in order of preference):

1. Paper tape output of the Motorola M6800 Software.
2. Hexadecimal coding using IBM Punch Cards.
3. EPROM (TMS2716 or MCM2716).
4. Hand-punched paper tape.

PAPER TAPE

Included in the software packages developed for the M6800 Microcomputer Family is the ability to produce a paper tape output for computerized mask generation. The assembler directives are used to control allocation of memory, to assign values for stored data, and for controlling the assembly process. The paper tape must specify the full 2048 bytes.

FIGURE 2 – BINARY TO HEXADECIMAL CONVERSION

Binary Data				Hexadecimal Character
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

IBM PUNCH CARDS

The hexadecimal equivalent (from Figure 2) may be placed on 80 column IBM punch cards as follows:

Step	Column	
1	12	Byte "0" Hexadecimal equivalent for outputs Q7 thru Q4 (Q7 = M.S.B.)
2	13	Byte "0" Hexadecimal equivalent for outputs Q3 thru Q0 (Q3 = M.S.B.)
3	14-75	Alternate steps 1 and 2 for consecutive bytes.
4	77-80	Card number (starting 0001) Total number of cards (64)

FIGURE 3 – FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM68A316A MOS READ ONLY MEMORY

Customer:

Company _____

Part No. _____

Originator _____

Phone No. _____

Motorola Use Only:

Quote: _____

Part No.: _____

Specif. No.: _____

Chip Select:

	Active High	Active Low	*Don't Care (No Connect)
$\overline{S1}$	☐	☐	☐
$\overline{S2}$	☐	☐	☐
$\overline{S3}$	☐	☐	☐

*A don't care must always be the highest order Chip Select(s).

MOTOROLA

MCM68A316E

MOS

(N-CHANNEL, SILICON-GATE)

2048 X 8 BIT
READ ONLY MEMORY

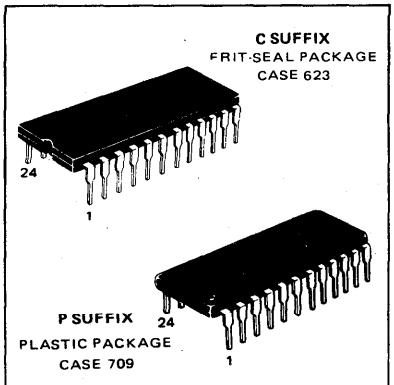
2

2048 X 8 BIT READ ONLY MEMORY

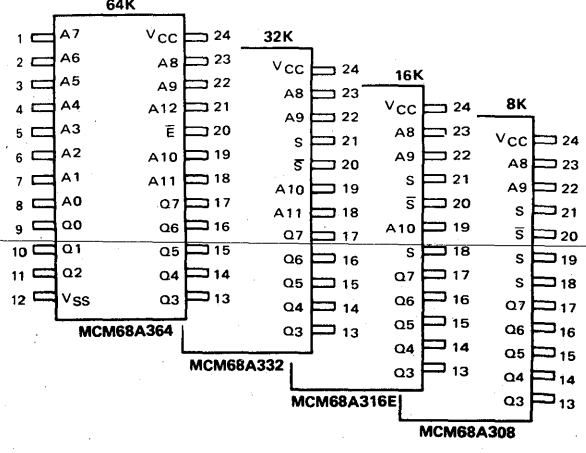
The MCM68A316E is a mask-programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refeshing because of static operation.

The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. Memory expansion is provided through multiple Chip Select inputs. The active level of the Chip Select inputs and the memory content are defined by the user.

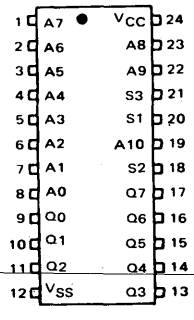
- Fully Static Operation
- Three-State Data Output
- Mask-Programmable Chip Selects for Simplified Memory Expansion
- Single ±10% 5-Volt Power Supply
- TTL Compatible
- Maximum Access Time = 350 ns
- Plug-in Compatible with 2316E
- Pin Compatible with 2708 and MCM2716 EPROMs



MOTOROLA'S PIN COMPATIBLE ROM FAMILY
(Industry Standard Pinouts)



PIN ASSIGNMENT



PIN NAMES	
A0–A10	Address Inputs
S1–S3	Chip Selects
Q0–Q7	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
Input High Voltage	V_{IH}	2.0	–	5.5	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.8	Vdc

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	–	2.5	μAdc
Output High Voltage (I_{OH} = -205 μA)	V_{OH}	2.4	–	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	0.4	Vdc
Output Leakage Current (Three-State) (S = 0.8 V or $\overline{S}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	–	10	μAdc
Supply Current (V_{CC} = 5.5 V, T_A = 0°C)	I_{CC}	–	130	mAdc

ABSOLUTE MAXIMUM RATINGS (See Note 1)

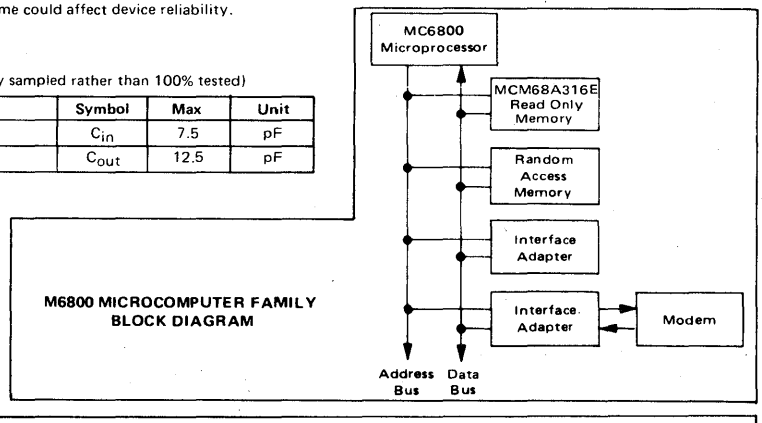
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

CAPACITANCE

(f = 2.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	7.5	pF
Output Capacitance	C_{out}	12.5	pF



M6800 MICROCOMPUTER FAMILY
BLOCK DIAGRAM

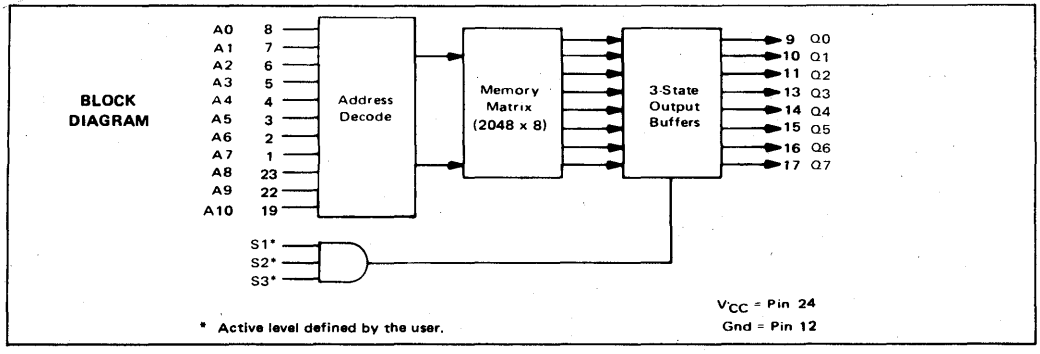
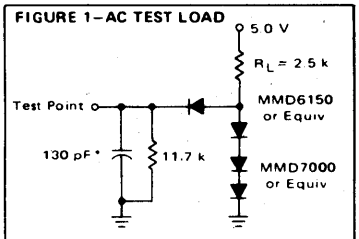


FIGURE 1–AC TEST LOAD



*Includes Jig Capacitance

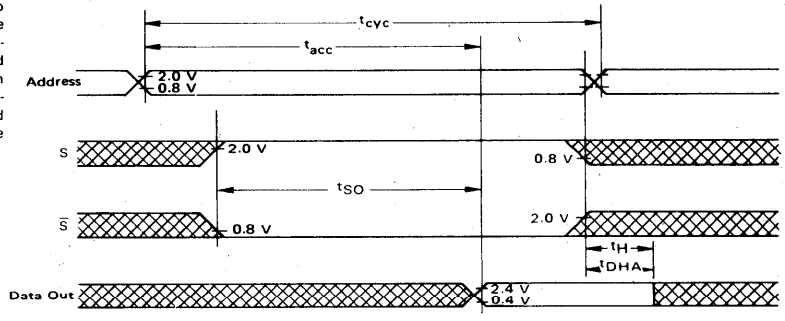
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.
All timing with $t_r = t_f = 20$ ns, Load of Figure 1)

Characteristic	Symbol	Min	Max	Unit
Cycle Time	t_{cyc}	350	–	ns
Access Time	t_{acc}	–	350	ns
Chip Select to Output Delay	t_{SO}	–	150	ns
Data Hold from Address	t_{DHA}	10	–	ns
Data Hold from Deselection	t_H	10	150	ns

TIMING DIAGRAM



CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68A316E, the customer may specify the content of the memory and the method of enabling the outputs.

Information on the general options of the MCM68A316E should be submitted on an Organizational Data form such as that shown in Figure 3. ("No-Connect" must always be the highest order Chip Select(s).)

Information for custom memory content may be sent to Motorola in one of three forms (shown in order of preference):

1. Paper tape output of the Motorola M6800 Software.
2. Hexadecimal coding using IBM Punch Cards.
3. EPROM (TMS2716 or MCM2716).

PAPER TAPE

Included in the software packages developed for the M6800 Microcomputer Family is the ability to produce a paper tape output for computerized mask generation. The assembler directives are used to control allocation of memory, to assign values for stored data, and for controlling the assembly process. The paper tape must specify the full 2048 bytes.

FIGURE 2 – BINARY TO HEXADECIMAL CONVERSION

Binary Data				Hexadecimal Character
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

IBM PUNCH CARDS

The hexadecimal equivalent (from Figure 2) may be placed on 80 column IBM punch cards as follows:

Step	Column	
1	12	Byte "0" Hexadecimal equivalent for outputs Q7 thru Q4 (Q7 = M.S.B.)
2	13	Byte "0" Hexadecimal equivalent for outputs Q3 thru Q0 (Q3 = M.S.B.)
3	14–75	Alternate steps 1 and 2 for consecutive bytes.
4	77–80	Card number (starting 0001) Total number of cards (64)

FIGURE 3 – FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM68A316E MOS READ ONLY MEMORY

Customer:

Company _____

Part No. _____

Originator _____

Phone No. _____

Motorola Use Only:

Quote: _____

Part No.: _____

Specif. No.: _____

Chip Select:

	Active High	Active Low	No Connect
S1	☐	☐	☐
S2	☐	☐	☐
S3	☐	☐	☐

MOTOROLA

MCM68A332

2

4096 X 8-BIT READ ONLY MEMORY

The MCM68A332 is a mask-programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of static operation.

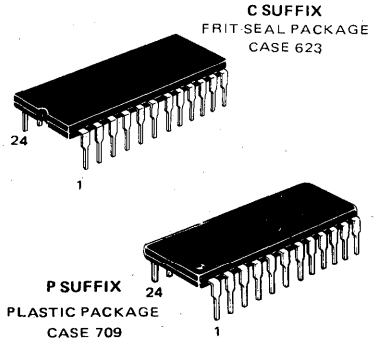
The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. Memory expansion is provided through multiple Chip Select inputs. The active level of the Chip Select inputs and the memory content are defined by the user.

- Fully Static Operation
- Three-State Data Output for OR-Ties
- Mask-Programmable Chip Selects for Simplified Memory Expansion
- Single ±10% 5-Volt Power Supply
- Fully TTL Compatible
- Maximum Access Time = 350 ns
- Directly Compatible with 4732
- Pin Compatible with 2708 and 2716 EPROMs
- Preprogrammed MCM68A332-2 Available

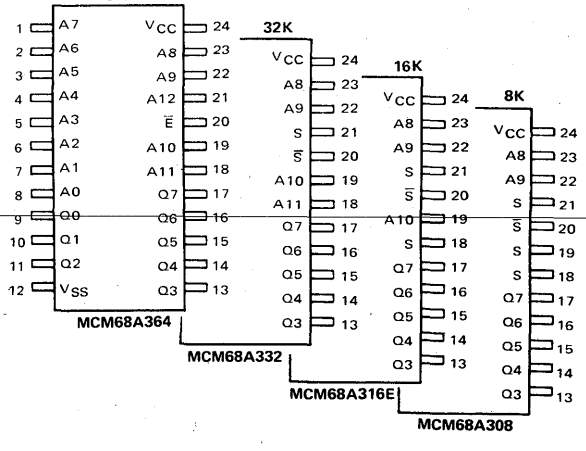
MOS

(N-CHANNEL, SILICON-GATE)

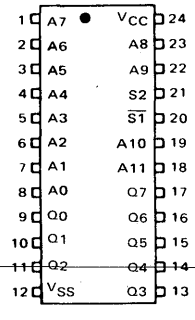
4096 X 8-BIT READ ONLY MEMORY



MOTOROLA'S PIN COMPATIBLE ROM FAMILY
(Industry Standard Pinouts)

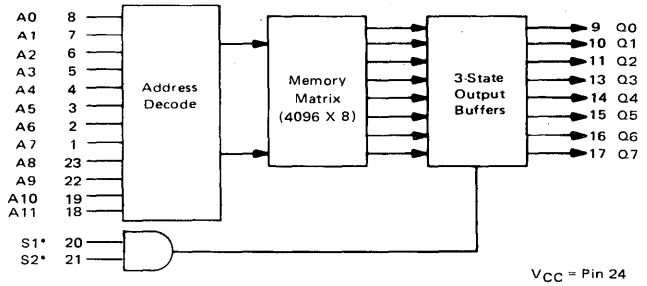


PIN ASSIGNMENT



PIN NAMES	
A0–A11	Address Inputs
S	Programmable Chip Selects
Q0–Q7	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

BLOCK DIAGRAM



* Active level defined by the user.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (V_{CC} must be applied at least 100 μs before proper device operation is achieved.)	V_{CC}	4.5	5.0	5.5	Vdc
Input High Voltage	V_{IH}	2.0	–	5.5	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.8	Vdc

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	–	2.5	μAdc
Output High Voltage (I_{OH} = -205 μA)	V_{OH}	2.4	–	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	0.4	Vdc
Output Leakage Current (Three-State) (S = 0.8 V or $\overline{S}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	–	10	μAdc
Supply Current (V_{CC} = 5.5 V, T_A = 0°C)	I_{CC}	–	80	mAdc

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

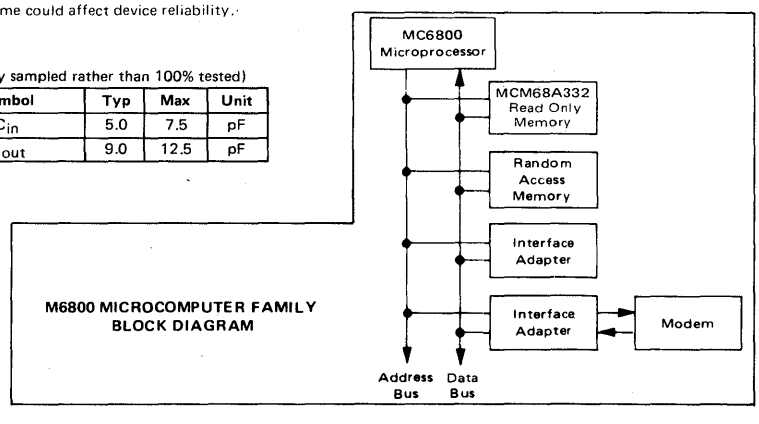
NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

CAPACITANCE

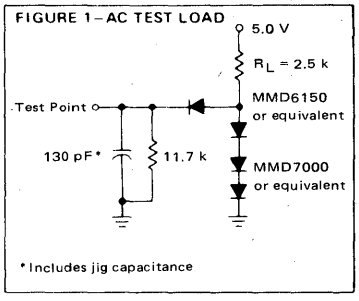
(f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	5.0	7.5	pF
Output Capacitance	C_{out}	9.0	12.5	pF



M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM

FIGURE 1–AC TEST LOAD



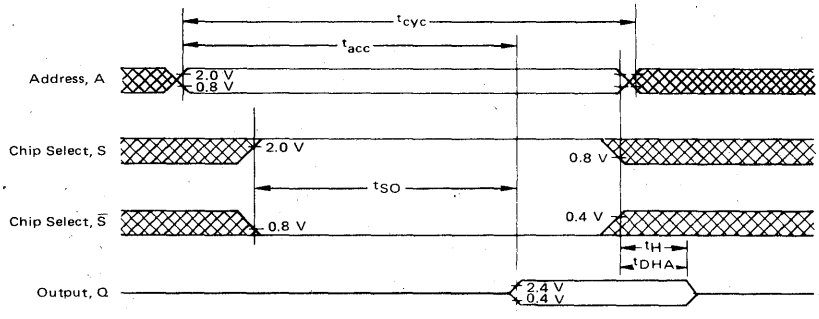
*Includes jig capacitance

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.
All timing with $t_r = t_f = 20$ ns, Load of Figure 1)

Characteristic	Symbol	Min	Max	Unit
Cycle Time	t_{cyc}	350	–	ns
Access Time	t_{acc}	–	350	ns
Chip Select to Output Delay	t_{SO}	–	150	ns
Data Hold from Address	t_{DHA}	10	–	ns
Data Hold from Deselection	t_H	10	150	ns

TIMING DIAGRAM



Waveform Symbol	Input	Output
——— / ———	MUST BE VALID	WILL BE VALID
▨	DON'T CARE ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
⟋ ⟍	–	HIGH IMPEDANCE

MCM68A332 CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68A332, the customer may specify the content of the memory and the method of enabling the outputs.

Information on the general options of the MCM68A332 should be submitted on an Organizational Data form such as that shown in Figure 3. (A "No-Connect" or "Don't Care" must always be the highest order Chip Select(s).)

Information for custom memory content may be sent to Motorola in one of four forms (shown in order of preference):

1. IBM Punch Cards:
   - A. Hexadecimal Format
   - B. Intel Format
   - C. Binary Negative-Postive Format
2. EPROMs—two 16K (MCM2716 or TMS2716) or four 8K (MCM2708)
3. Paper tape output of the Motorola M6800 software
4. Hand punched paper tape

PAPER TAPE

Included in the software packages developed for the M6800 Microcomputer Family is the ability to produce a paper tape output for computerized mask generation. The assembler directives are used to control allocation of memory, to assign values for stored data, and for controlling the assembly process. The paper tape must specify the full 4096 bytes.

IBM PUNCH CARDS, HEXADECIMAL FORMAT

The hexadecimal equivalent (from Figure 2) may be placed on 80 column IBM punch cards as follows:

Step	Column	
1	12	Byte "0" Hexadecimal equivalent for outputs Q7 through Q4 (Q7 = M.S.B.)
2	13	Byte "0" Hexadecimal equivalent for outputs Q3 through Q0 (Q3 = M.S.B.)
3	14–75	Alternate steps 1 and 2 for consecutive bytes.
4	77–79	Card number (starting 001).
5		Total number of cards must equal 128.

FIGURE 2 – BINARY TO HEXADECIMAL CONVERSION

Binary Data				Hexadecimal Character
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

PRE-PROGRAMMED MCM68A332P2, MCM68A332C2

The -2 standard ROM pattern contains sine-lookup and arctan-lookup tables.

Locations 0000 through 2001 contain the sine values. The sine's first quadrant is divided into 1000 parts with sine values corresponding to these angles stored in the ROM. Sin $\pi/2$ is included and is rounded to 0.9999.

The arctan values contain angles in radians corresponding to the arc tangents of 0 through 1 in steps of 0.001 and are contained in locations 2048 through 4049.

Locations 2002 through 2047 and 4050 through 4095 are zero filled.

All values are represented in absolute decimal format with four digit precision. They are stored in BCD format with the two most significant digits in the lower byte and the two least significant digits in the upper byte. The decimal point is assumed to be to the left of the most significant digit.

Example: $\sin\left(\frac{1}{1000}\ \frac{\pi}{2}\right) = 0.0016$ decimal

Address	Contents
0002	0000 0000
0003	0001 0110

FIGURE 3 – FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM68A332 MOS READ ONLY MEMORY

Customer:

Company _____

Part No. _____

Originator _____

Phone No. _____

Motorola Use Only

Quote _____

Part No. _____

Specif. No. _____

Chip Select Options:	Active High	Active Low	No-Connect
S1	☐	☐	☐
S2	☐	☐	☐

MOTOROLA

MCM68A364
MCM68B364

Advance Information

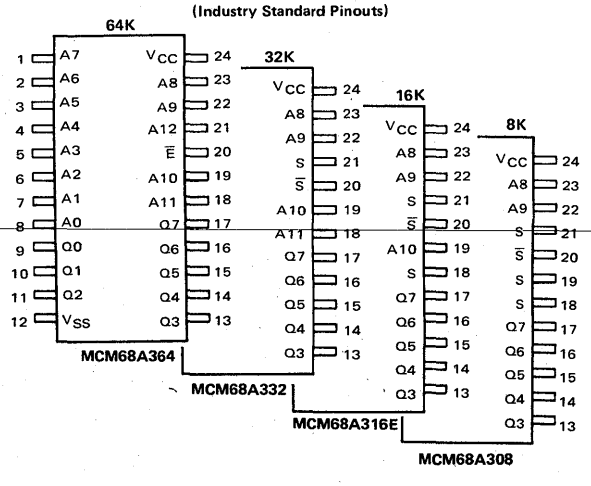
8192 X 8-BIT READ ONLY MEMORY

The MCM68A364/MCM68B364 is a mask-programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of static operation.

The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. The active level of the Chip Enable input and the memory content is defined by the user. The Chip Enable input deselects the output and puts the chip in a power-down mode.

- Fully Static Operation
- Automatic Power Down
- Low Power Dissipation – 150 mW active (typical)
  30 mW standby (typical)
- Single ±10% 5-Volt Power Supply
- High Output Drive Capability (2 TTL Loads)
- Three-State Data Output for OR-Ties
- Mask Programmable Chip Enable
- TTL Compatible
- Maximum Access Time – 250 ns – MCM68B364
  350 ns – MCM68A364
- Pin Compatible with 8K – MCM68A308, 16K – MCM68A316E, and 32K – MCM68A332 Mask-Programmable ROMs

MOTOROLA'S PIN COMPATIBLE ROM FAMILY
(Industry Standard Pinouts)

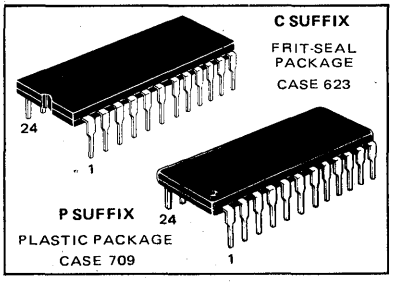


This is advance information and specifications are subject to change without notice.

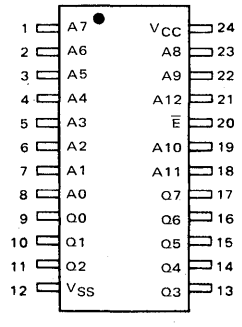
MOS

(N-CHANNEL, SILICON-GATE)

8192 X 8-BIT
READ ONLY MEMORY

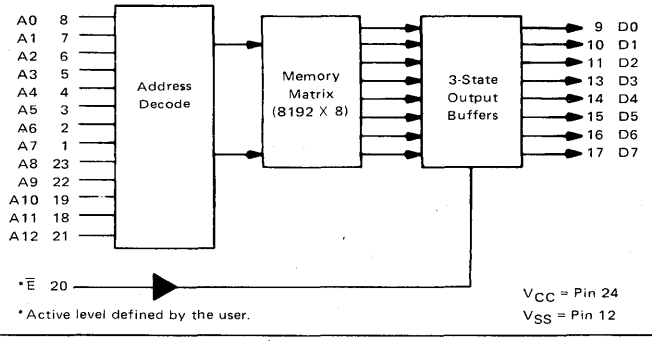


PIN ASSIGNMENT



PIN NAMES	
A0–A12	Address
$\overline{E}$	Chip Enable
Q0–Q7	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

BLOCK DIAGRAM



DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage (V_{CC} must be applied at least 100 μs before proper device operation is achieved)	V_{CC}	4.5	5.0	5.5	Vdc
Input High Voltage	V_{IH}	2.0	–	5.5	Vdc
Input Low Voltage	V_{IL}	−0.3	–	0.8	Vdc

DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	–	–	2.5	μAdc
Output High Voltage (I_{OH} = −205 μA)	V_{OH}	2.4	–	–	Vdc
Output Low Voltage (I_{OL} = 3.2 mA)	V_{OL}	–	–	0.4	Vdc
Output Leakage Current (Three-State) ($\bar{E}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	–	–	10	μAdc
Supply Current — Active (V_{CC} = 5.5 V, T_A = 0°C)	I_{CC}	–	30	60	mAdc
Supply Current — Standby (V_{CC} = 5.5 V, T_A = 0°C, $\bar{E}$ = V_{IH})	I_{SB}	–	6.0	15	mAdc

CAPACITANCE

(f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	7.5	pF
Output Capacitance	C_{out}	12.5	pF

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{in}	−0.3 to +7.0	Vdc
Operating Temperature Range —	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTE 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

AC OPERATING CONDITIONS AND CHARACTERISTICS

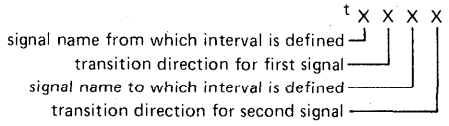
Read Cycle

RECOMMENDED AC OPERATING CONDITIONS

(T_A = 0 to 70°C, V_{CC} = 5.0 V ± 10%. All timing with $t_r = t_f$ = 20 ns, load of Figure 1.)

Parameter	Symbol	MCM68B364		MCM68A364		Unit
		Min	Max	Min	Max	
Address Valid to Address Don't Care (Cycle Time when Chip Enable is held Active)	t_{AVAX}	250	–	350	–	ns
Chip Enable Low to Chip Enable High	t_{ELEH}	250	–	350	–	ns
Address Valid to Output Valid (Access)	t_{AVQV}	–	250	–	350	ns
Chip Enable Low to Output Valid (Access)	t_{ELQV}	–	250	–	350	ns
Address Valid to Output Invalid	t_{AVQX}	10	–	10	–	ns
Chip Enable Low to Output Invalid	t_{ELQX}	10	–	10	–	ns
Chip Enable High to Output High Z	t_{EHQZ}	0	70	0	80	ns
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	ns
Chip Deselection to Power Down Time	t_{PD}	–	100	–	120	ns
Address Valid to Chip Enable Low (Address Setup)	t_{AVEL}	0	–	0	–	ns

TIMING PARAMETER ABBREVIATIONS



The transition definitions used in this data sheet are:

- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

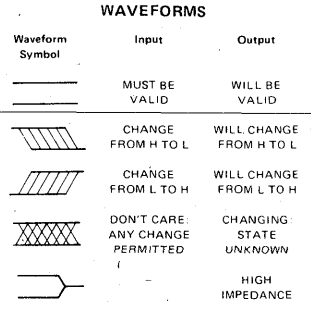
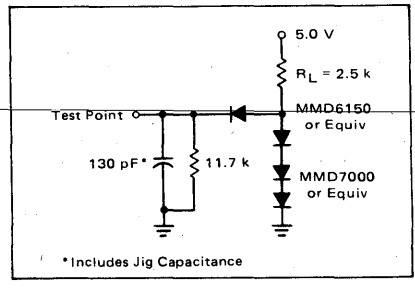


FIGURE 1 – AC TEST LOAD



CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68A364/MCM68B364, the customer may specify the content of the memory and the method of enabling the outputs.

Information on the general options of the MCM68A364/MCM68B364 should be submitted on an Organizational Data form such as that shown in Figure 3.

Information for custom memory content may be sent to Motorola in one of two forms (shown in order of preference):

1. IBM Punch Cards
   A. Hexadecimal Format
   B. INTEL Hexadecimal Format
   C. Binary Negative-Positive Format
2. EPROMs – four 16K (MCM2716, or TMS2716, or eight 8K (MCM2708).

PAPER TAPE

Included in the software packages developed for the M6800 Microcomputer Family is the ability to produce a paper tape output for computerized mask generation. The assembler directives are used to control allocation of memory, to assign values for stored data, and for controlling the assembly process. The paper tape must specify the full 8,192 bytes.

FIGURE 2 – BINARY TO HEXADECIMAL CONVERSION

Binary Data				Hexadecimal Character
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

IBM PUNCH CARDS, HEXADECIMAL FORMAT

The hexadecimal equivalent (from Figure 2) may be placed on 80 column IBM punch cards as follows:

Step	Column	
1	12	Byte "0" Hexadecimal equivalent for outputs Q7 through Q4 (Q7 = M.S.B.)
2	13	Byte "0" Hexadecimal equivalent for outputs Q3 through Q0 (Q3 = M.S.B.)
3	14–75	Alternate steps 1 and 2 for consecutive bytes
4	77–79	Card number (starting 001)
5		Total number of cards must equal 256

FIGURE 3 – FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM68A364/MCM68B364 MOS READ ONLY MEMORY

Customer:

Company _____

Part No. _____

Originator _____

Phone No. _____

Motorola Use Only:

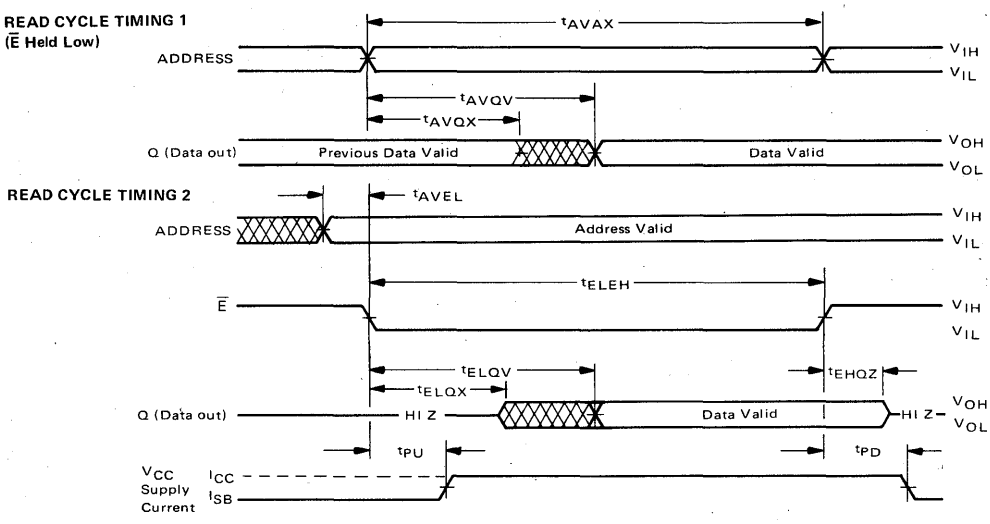
Quote: _____

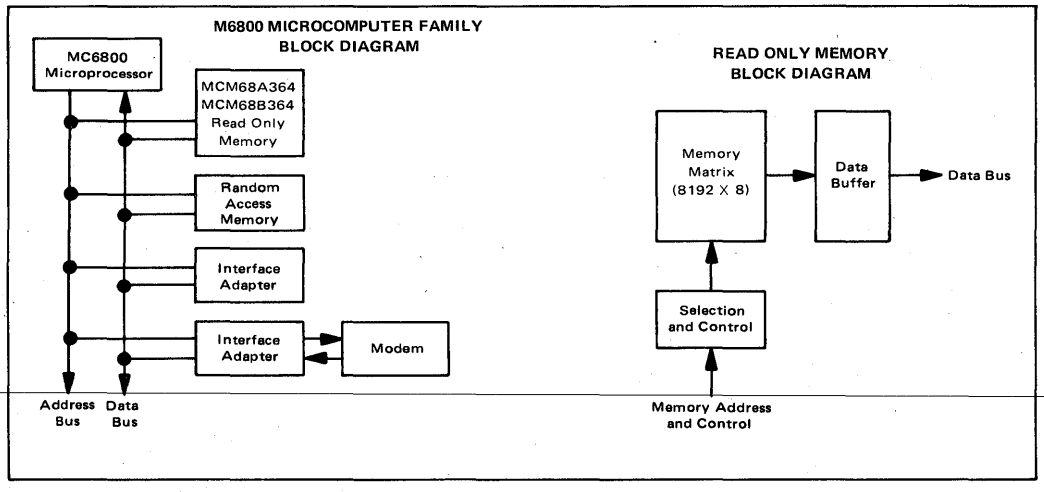
Part No.: _____

Specif. No.: _____

Enable Options:

	Active High	Active Low
Chip Enable	☐	☐


READ CYCLE TIMING 1
(E Held Low)
ADDRESS
tAVAX
VIH
VIL
tAVQV
tAVQX
Q (Data out)
Previous Data Valid
Data Valid
VOH
VOL
READ CYCLE TIMING 2
tAVEL
ADDRESS
Address Valid
tELEH
E
tELQV
tELQX
tEHQZ
Q (Data out)
HI Z
Data Valid
HI Z
tPU
tPD
VCC
Supply
Current
ICC
ISB


M6800 MICROCOMPUTER FAMILY
BLOCK DIAGRAM
MC6800
Microprocessor
MCM68A364
MCM68B364
Read Only
Memory
Random
Access
Memory
Interface
Adapter
Interface
Adapter
Modem
Address
Bus
Data
Bus
READ ONLY MEMORY
BLOCK DIAGRAM
Memory
Matrix
(8192 X 8)
Data
Buffer
Data Bus
Selection
and Control
Memory Address
and Control

PRE-PROGRAMMED MCM68A364P3/C3, MCM68B364P3/C3

The -3 standard ROM pattern contains log (base 10) and antilog (base 10) lookup tables for the 64K ROM.

Locations 0000 through 3599 contain log base 10 values. The arguments for the log table range from 1.00 through 9.99 incrementing in steps of 1/100. Each log value is represented by an eight- digit decimal number with decimal point assumed to be to the left of the most-significant digit.

Antilog (base 10) are stored in locations 4096 through 8095. The arguments range from .000 through .999 incrementing in steps of 1/1000. Each antilog value is represented by an eight- digit decimal number with decimal point assumed to be to the right of the most-significant digit.

Locations 3600 through 4095 and 8096 through 8191 are zero filled.

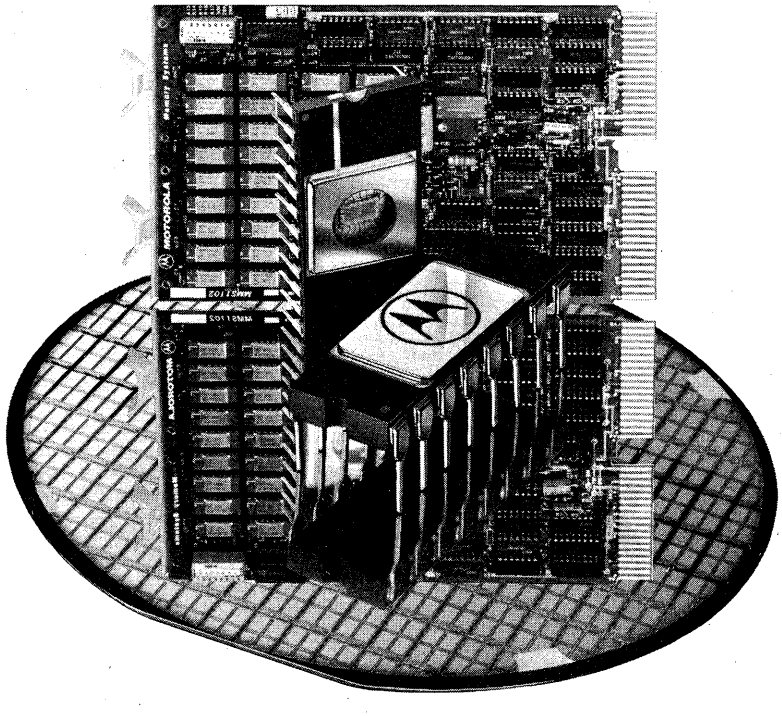
All values are represented in absolute decimal format with eight digit precision. They are stored in BCD format with the two most significant digits in the lower byte and the remaining six digits in the three consequitive locations.

Example: $\log_{10}(1.01) = .00432137$ decimal

Address	Contents	
4	0000	0000
5	0100	0011
6	0010	0001
7	0011	0111

CMOS Memories
RAM, ROM

3



MOTOROLA

MCM14505

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

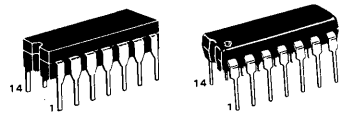
64-BIT (64 x 1) STATIC RANDOM ACCESS MEMORY

64-BIT STATIC RANDOM ACCESS MEMORY

The MCM14505 64-bit random access memory is fully decoded on the chip and organized as 64 one-bit words (64 X 1). Medium speed operation and micropower supply requirements make this device useful for scratch pad or buffer memory applications where power must be conserved or where battery operation is required.

When used with a battery backup, the MCM14505 can be utilized as an alterable read-only memory, allowing the battery to retain information in the memory when the system is powered down, and allowing the battery to charge when power is applied. The micropower requirements of this memory allow quiescent battery operation for great lengths of time without significant discharging.

- Quiescent Current = 50 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Read/Write Control Line
- Wired-OR Output Capability (3-State Output) for Memory Expansion
- Access Time = 180 ns typical at V_{DD} = 10 Vdc
- Write Cycle Time = 275 ns typical at V_{DD} = 10 Vdc
- Fully Buffered Low Capacitance Inputs
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

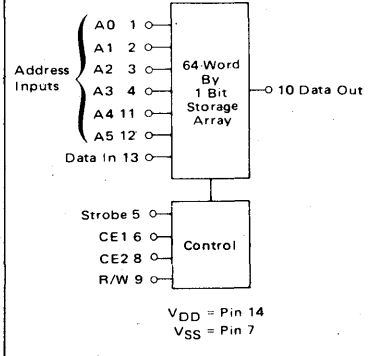
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

BLOCK DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

3

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Noise Immunity #	V_{NL}									Vdc
(V_{out} ≤ 0.8 Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
(V_{out} ≤ 1.0 Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
(V_{out} ≤ 1.5 Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
(V_{out} ≥ 0.8 Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
(V_{out} ≥ 1.0 Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
(V_{out} ≥ 1.5 Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.3	–	0.25	0.35	–	0.18	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.9	–	0.75	1.2	–	0.50	–	
(V_{OL} = 1.5 Vdc)		15	2.2	–	1.7	4.5	–	1.2	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.2	–	0.15	0.35	–	0.1	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.6	–	0.5	1.2	–	0.4	–	
(V_{OL} = 1.5 Vdc)		15	3.9	–	0.75	4.5	–	0.6	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±1.0	–	±0.00001	±1.0	–	±14	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–		–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.050	5.0	–	150	µAdc
		10	–	10	–	0.100	10	–	300	
		15	–	20	–	0.150	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	50	–	0.050	50	–	375	µAdc
		10	–	100	–	0.100	100	–	750	
		15	–	200	–	0.150	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.28 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.56 µA/kHz) f + I_{DD}							
		15	I_T = (3.85 µA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	µAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (2.43 ns/pF) C_L + 58.5 ns		5.0	–	180	360	
t_{TLH} = (1.08 ns/pF) C_L + 36 ns		10	–	90	180	
t_{TLH} = (0.72 ns/pF) C_L + 39 ns		15	–	75	150	
Output Fall Time	t_{THL}					ns
t_{THL} = (2.16 ns/pF) C_L + 52 ns		5.0	–	160	320	
t_{THL} = (0.96 ns/pF) C_L + 32 ns		10	–	80	160	
t_{THL} = (0.69 ns/pF) C_L + 33 ns		15	–	65	130	
Propagation Delay Time	$t_{acc(R)}$					ns
Read Access Time						
$t_{acc(R)}$ = (1.4 ns/pF) C_L + 385 ns		5.0	–	455	750	
$t_{acc(R)}$ = (10.7 ns/pF) C_L + 175 ns		10	–	210	400	
$t_{acc(R)}$ = (0.5 ns/pF) C_L + 105 ns		15	–	130	300	
Strobe Down Time	t_{WL}					ns
		5.0	500	100	–	
		10	125	50	–	
		15	95	75	–	
Address Setup Time	t_{su}					ns
		5.0	300	-100	–	
		10	120	-40	–	
		15	90	-25	–	
Data Setup Time	$t_{su(D)}$					ns
		5.0	200	70	–	
		10	75	25	–	
		15	55	20	–	
Read Setup Time	$t_{su(R)}$					ns
		5.0	270	90	–	
		10	60	20	–	
		15	45	15	–	
Write Setup Time	$t_{su(W)}$					ns
		5.0	400	80	–	
		10	100	25	–	
		15	75	11	–	
Address Release Time	$t_{rel(R)}$					ns
		5.0	75	15	–	
		10	25	10	–	
		15	20	5.0	–	
Data Hold Time	$t_{h(D)}$					ns
		5.0	50	0	–	
		10	15	0	–	
		15	10	0	–	
Read Release Time	$t_{rel(R)}$					ns
		5.0	0	-90	–	
		10	0	-25	–	
		15	0	-10	–	
Write Release Time	$t_{rel(W)}$					ns
		5.0	0	5.0	–	
		10	0	10	–	
		15	0	30	–	
Read Cycle Time	$t_{cyc(R)}$					ns
		5.0	–	500	750	
		10	–	200	400	
		15	–	150	300	
Write Cycle Time	$t_{cyc(W)}$					ns
		5.0	–	440	700	
		10	–	275	550	
		15	–	200	415	
Output Disable Delay	t_{dis}					ns
(10% Output Change into 1.0 kΩ Load)		5.0	–	200	600	
		10	–	80	200	
		15	–	60	150	

*The formula is for the typical characteristics only.

3

FIGURE 1 – READ CYCLE TIMING DIAGRAM

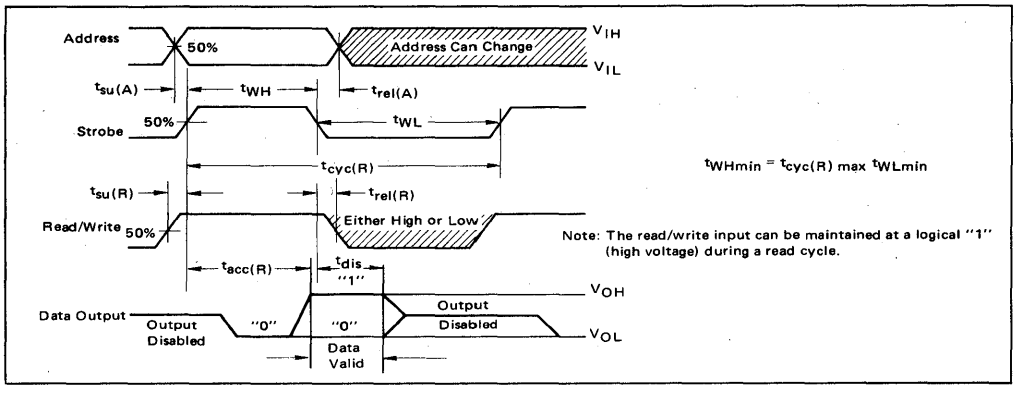


FIGURE 2 – WRITE CYCLE TIMING DIAGRAM

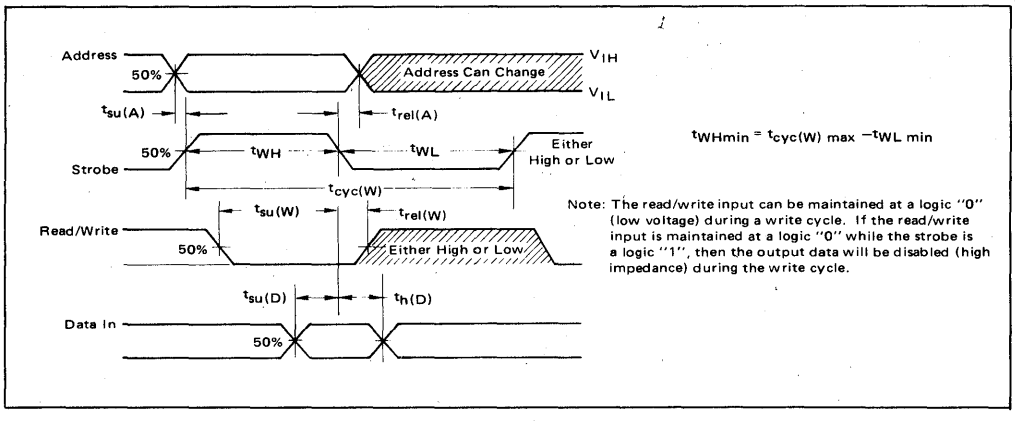


FIGURE 3 – MAXIMUM STROBE PULSE WIDTH versus TEMPERATURE

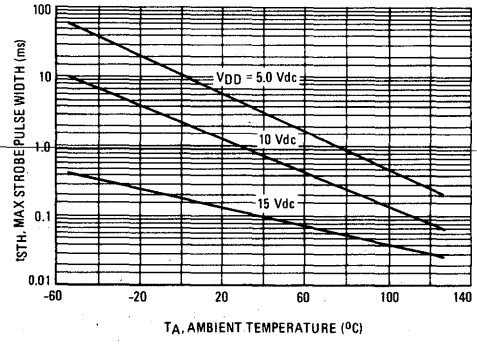


FIGURE 4 – TYPICAL READ ACCESS TIME versus LOAD CAPACITANCE

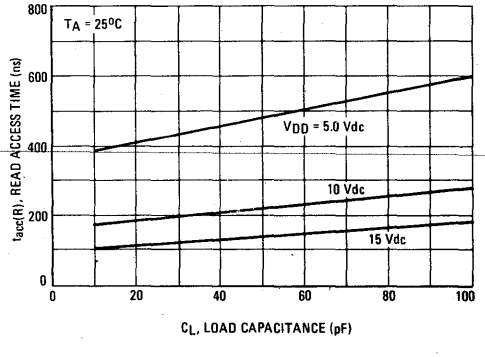
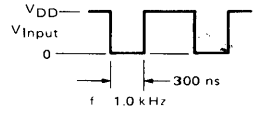
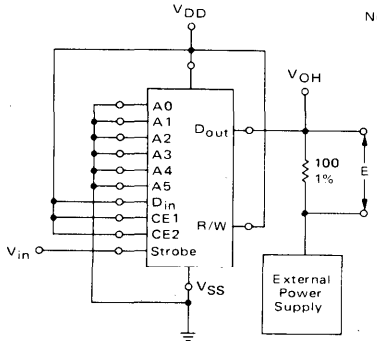


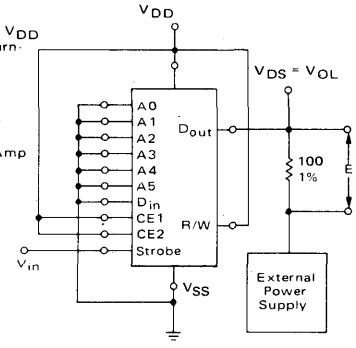
FIGURE 5 – TYPICAL OUTPUT SOURCE CAPABILITY versus TEMPERATURE

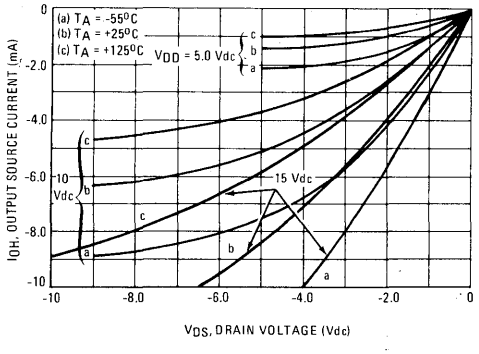
FIGURE 6 – TYPICAL OUTPUT SINK CAPABILITY versus TEMPERATURE





Notes:
1. Cycle R/W to ground and then to V_{DD} prior to measurement to insure turn-on of the device under test.
2. For the P-channel characteristics, $V_{DS} = V_{OH} - V_{DD}$.
3. For the N-channel characteristics, V_{DS} is measured directly.
4. For the drain current, $I_D = \frac{E}{100}$ Amp





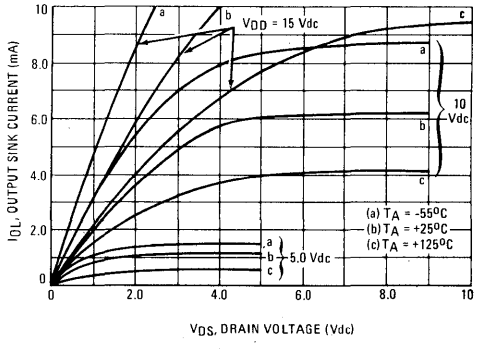
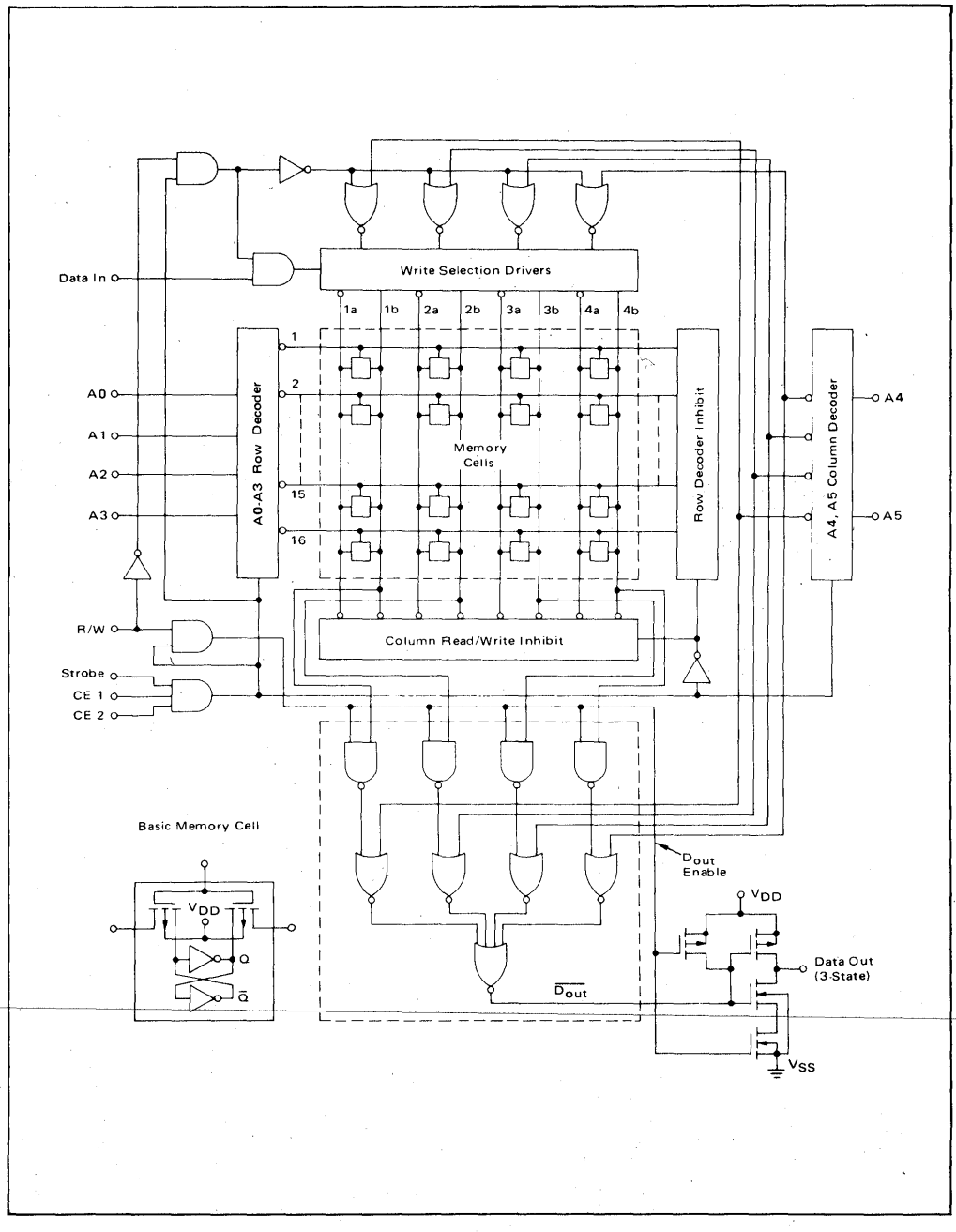


FIGURE 7 – FUNCTIONAL CIRCUIT DIAGRAM



OPERATING CHARACTERISTICS

In considering the operation of the MCM14505 CMOS memory, refer to the functional circuit diagram of Figure 7 and timing diagrams shown in Figures 1 and 2. The basic memory cell is a cross-coupled flip-flop consisting of two inverter gates and two P-channel devices for read/write control. The push-pull cell provides high speed as well as low power.

During a read cycle, when the strobe line is high the write selection drivers are disabled and the data from the selected row is available on columns 1b, 2b, 3b, and 4b. The A4 and A5 address bits are decoded to select output data from one of the four columns. The output data is available on the data output pin only when the strobe and read/write lines are high simultaneously and after the read access time, $t_{acc(R)}$, has occurred (see Figure 1). Note that the output is initially disabled and always goes to the logic "0" state (low voltage) before data is valid. The output is in the high-impedance state (disabled) when the strobe line or the R/W line is in the low state. The memory is strobed for reading or writing only when the strobe, CE1, and CE2 are high simultaneously. The R/W line can be a dc voltage during a read or write cycle and need not be pulsed, as shown in the timing diagrams. For this case the R/W line should be a logic "1" (high) for reading and a logic "0" for writing.

When the strobe line is high, the column read/write inhibit gates and the row decoder inhibit gates are disabled, the selected row is in the low state, and the unselected 15 rows retain their logic "1" level due to the row capacitance that exists when the row decoder inhibit gates are disabled. This capacitive storage mechanism requires a maximum strobe width (see Figure 3) equal to the junction reverse bias RC time constant. When the strobe is returned to a logic "0" the rows are forced to V_{DD} by the row decoder inhibit gates (pullup devices). Similarly the column read/write inhibit gates (pulldown devices) force the column lines to a logic "0" state.

Two column lines are associated with each memory cell in order to write into the cell. The write selection drivers are enabled when the R/W line is a logic "0" and the strobe line is a logic "1". The input data is written into the column selected by the column decoder. For instance, if a "1" is to be written in the memory cell associated with row 1 and column 1, then row 1 would be enabled (logic "0") while column 1b is forced high and column 1a is forced low by the write selection drivers. If a logic "0" is to be written into the cell, then column 1a is forced high and 1b is forced low. The data that is retained in the memory cell is the data that was present on the data input pin at the moment the strobe goes low when R/W is low, or when R/W goes high when the strobe is high.

3

APPLICATIONS INFORMATION

Figure 8 shows a 256-word by n-bit static RAM memory system The outputs of four MCM14505 devices are tied together to form 256 words by 1 bit. Additional bits are attained by paralleling the inputs in groups of four. Memories of larger words can be attained by decoding the most significant bits of the address and ANDing them with the strobe input.

Fan-in and fan-out of the memory is limited only by speed requirements. The extremely low input and output leakage current (100 nA maximum) keep the output voltage levels from changing significantly as more outputs are tied together. With the output levels independent of fan-out, most of the power supply range is available as logic swing, regardless of the number of units wired together. As a result, high noise immunity is maintained under all conditions.

Power dissipation is 0.1 μW per bit at a 1.0-kHz rate for a 5.0-volt power supply, while the static power dissipation is 2.0 nW per bit. This low power allows non-volatile information storage when the memory is powered by a small standby battery.

Figure 9 shows an optional standby power supply circuit for making a CMOS memory "non-volatile". When the usual power fails, a battery is used to sustain operation or maintain stored information. While normal power supply voltage is present, the battery is trickle-charged through a resistor which sets the charging rate. V_B is the sustaining voltage, and V^+ is the ordinary voltage from a power supply. V_{DD} connects to the power pin on the memory. Low-leakage diodes are recommended to conserve battery power.

The memory system shown in Figure 8 can be interfaced directly with the other devices in the McMOS family. No external components are required.

At the inputs to the CMOS memory, TTL devices can interface directly if an open-collector logic gate such as the MC7407 is used as shown in Figure 10. Driver circuits are not required since the input capacitance is low (4.0 to 6.0 pF). The address, data, and read/write inputs do not need to be fast since they can be changed for the duration when the strobe pulse is low, t_{STL} (see Figures 1 and 2). For high-speed operation, a push-pull driver should be used if more than five strobe inputs must be driven at one time. One circuit of the type shown in Figure 10 can be used for every ten strobe inputs.

Figures 11, 12, and 13 show methods of interfacing the memory output to TTL logic at various memory voltages. If a V_{DD} of 5.0 volts is used for slow-speed, low-power applications, one transistor and one resistor must be used (Figure 11). The MCM14505AL will drive one low-power TTL gate directly.

If a V_{DD} of 10 volts is used, the output of the memory device can fan out to two low-power TTL gates (Figure 12a) or to a discrete transistor (Figure 12b). The discrete transistor circuit provides higher speed and/or high fan-out. A pulldown resistor at the base of the transistor is not needed for fast turn-off because of the push-pull output of the memory. Turn-on time of the transistor is much faster in Figure 12b since the voltage rise is only 0.75 volt. The low output capacitance of the MCM14505 means that several outputs can be wire-ORed without significantly degrading performance. The read access time is increased by only 20 ns typically for 16 outputs tied together when Figure 12b is used.

Five low-power TTL gates can be driven from the memory output if a V_{DD} of 15 volts is used (Figure 13a). Figure 13b shows the interface if a discrete transistor is used. The 1.0 kilohm resistor in the base is required to insure that not more than 10 mA flows through the output as listed in the maximum ratings. If a 2.0 kilohm collector resistor is used (fan-out = 3), the turn-on time of the transistor is only slightly faster than in the circuit shown in Figure 12b due to the lower output impedance when V_{DD} = 15 volts. The voltage at the memory data output has to rise to only 1.3 volts to insure driving a fan-out of three TTL devices.

If a 510-ohm collector resistor is used, 20 TTL loads may be driven. The read access time is increased about 20 ns when four memory outputs are tied together since the output voltage must rise to 3.7 volts before the transistor can sink the full I_{OL} for a fan-out of 20 TTL devices. Almost any NPN transistor with a minimum beta of 15 can be used for the interface shown in Figures 11, 12 and 13.

The high source current from the push-pull output stage of the MCM14505 makes for a simpler interface circuit since a low source current memory requires a differential comparator to achieve high-speed operation.

FIGURE 8 – CMOS 256-WORD BY n-BIT STATIC READ/WRITE MEMORY

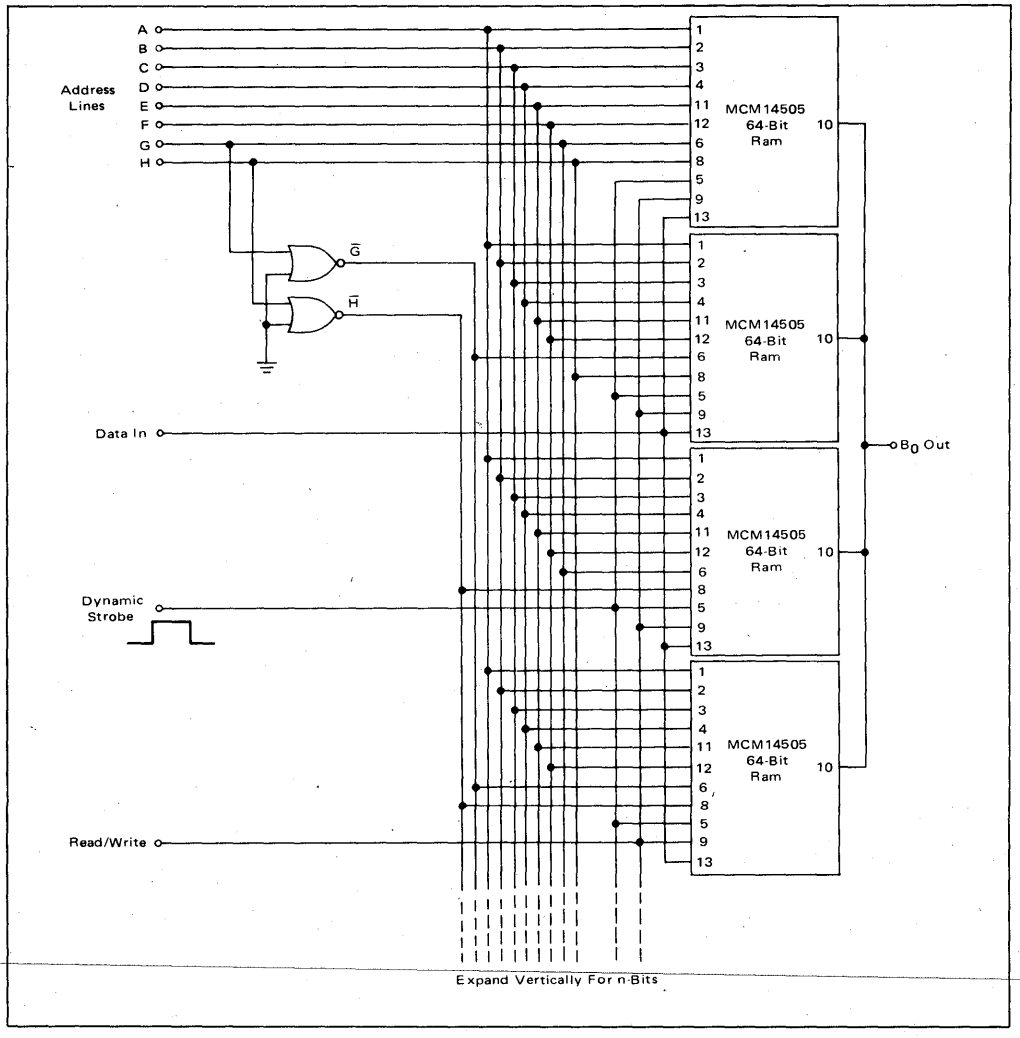


FIGURE 9 – STAND BY BATTERY CIRCUIT

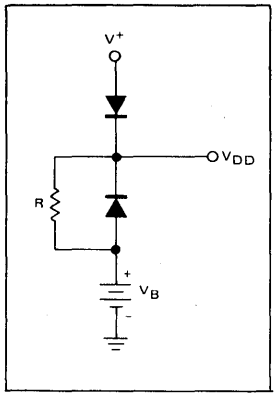


FIGURE 10 – TTL TO CMOS INTERFACE

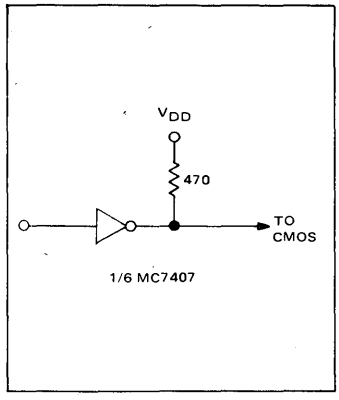


FIGURE 11 – CMOS-TO-TTL INTERFACE FOR V_{DD} = 5.0 V

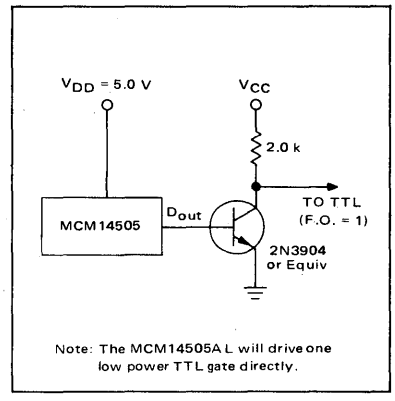


FIGURE 12 – CMOS-TO-TTL INTERFACE FOR V_{DD} = 10 V

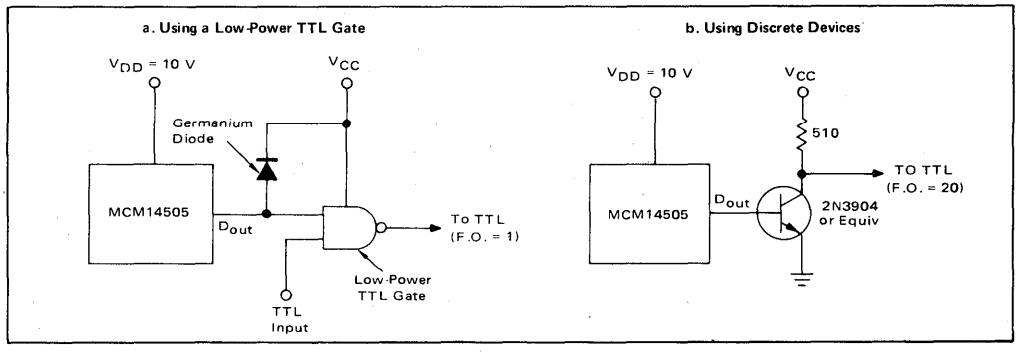
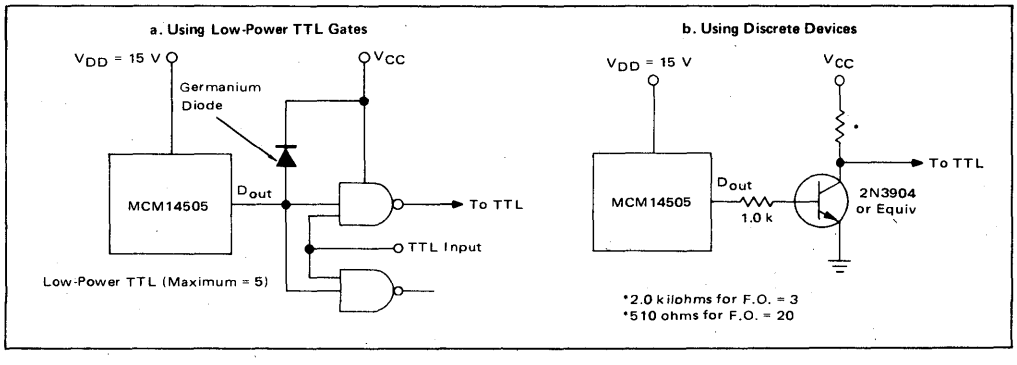


FIGURE 13 – CMOS-TO-TTL INTERFACE FOR V_{DD} = 15 V



MOTOROLA

MCM14537

256-BIT STATIC RANDOM ACCESS MEMORY

The MCM14537 is a static random access memory (RAM) organized in a 256 x 1-bit pattern and constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The circuit consists of eight address inputs (A_n), one data input (D_{in}), one write enable input (WE), one strobe input (ST), two chip enable inputs (CE_n), and one data output (D_{out}).

Using both chip enable inputs as extensions of the address inputs, a 10-bit address scheme may be employed. Four MCM14537 devices may be used to comprise a 1024-bit memory without additional address decoding. The CE and ST inputs are dissimilary designed to enable usage of the memory in a variety of applications. An output latch is provided on the chip for storing the data read or written into memory, making a data-out storage register unnecessary. The CE inputs control the data output for third-state (high output impedance) or active operation which makes the memory very useful in a bus oriented system. When CE2 is high the chip is fully disabled. When CE1 is high the output is in the third state but data can be written into the output latch during a read cycle. This enables the use of the memory for fast reading by using the CE1 input to enable the latch. The memory is also designed so that dc signals can operate the memory with no maximum pulse width required on the CE and ST lines.

Medium speed operation and micropower operation make the device useful in scratch pad and buffer applications where micropower or battery operation and high noise immunity are required.

- Quiescent Current = 0.5 μA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- 3-state Output Capability for Memory Expansion
- Output Data Latch Eliminates Need for Storage Buffer
- Access Time = 700 ns typical @ V_{DD} = 10 Vdc
- Fully Decoded and Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

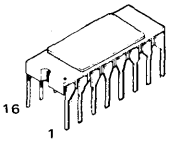
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

256-BIT (256 x 1) STATIC RANDOM ACCESS MEMORY

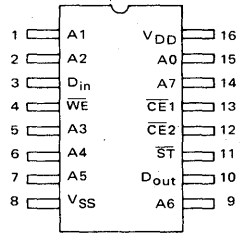


CERAMIC PACKAGE
CASE 690

ORDERING INFORMATION

MCM14XXX — Suffix Denotes
- L Ceramic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Noise Immunity #	V_{NL}									Vdc
(V_{out} ≤ 0.8 Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
(V_{out} ≤ 1.0 Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
(V_{out} ≤ 1.5 Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
(V_{out} ≥ 0.8 Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
(V_{out} ≥ 1.0 Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
(V_{out} ≥ 1.5 Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2	–	-1.0	-1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.8	-1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.2	–	-0.16	-0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	-0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	-3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±1.0	–	±0.00001	±1.0	–	±14	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–		–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	100	–	0.5	100	–	1800	μAdc
(Per Package)		10	–	200	–	1.0	200	–	3600	
		15	–	400	–	1.5	400	–	7200	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	100	–	0.5	100	–	1800	μAdc
(Per Package)		10	–	200	–	1.0	200	–	3600	
		15	–	400	–	1.5	400	–	7200	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.46 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.91 μA/kHz) f + I_{DD}							
		15	I_T = (4.37 μA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	μAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	μAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

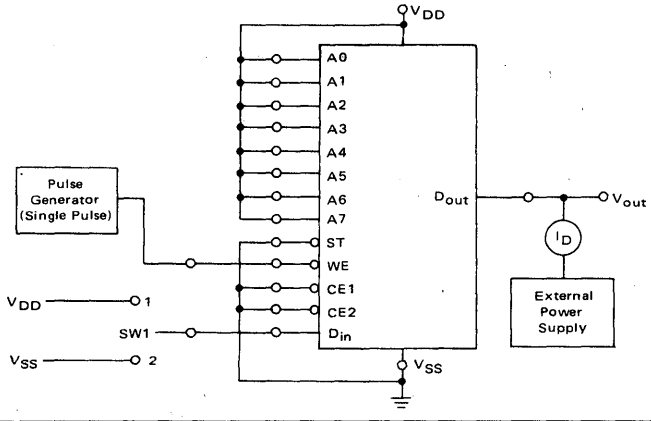
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Figure	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	3	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns			5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns			10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns			15	–	65	130	
Output Fall Time	3	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns			5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns			10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns			15	–	40	80	
Read Access Time from $\overline{ST}$ or $\overline{CE2}$	4, 5	$t_{acc(R)}$					ns
t_{acc} = (1.4 ns/pF) C_L + 2480 ns			5.0	400	2500	6000	
t_{acc} = (0.7 ns/pF) C_L + 690 ns			10	150	700	2000	
t_{acc} = (0.5 ns/pF) C_L + 393 ns			15	115	400	1500	
Output Enable Delay from $\overline{CE1}$ or $\overline{CE2}$	5, 6	$t_{acc(\overline{CE}_n)}$	5.0	70	300	900	ns
			10	25	100	300	
			15	20	70	225	
Setup Time from A_n to $\overline{ST}$ or $\overline{CE2}$	4, 5, 6, 7	$t_{su(A)}$	5.0	1800	600	–	ns
			10	600	200	–	
			15	450	140	–	
Hold Time from A_n to $\overline{ST}$ or $\overline{CE2}$	4, 5, 6, 7	$t_{h(A)}$	5.0	600	200	–	ns
			10	240	80	–	
			15	180	55	–	
Data Hold Time	7	$t_{h(D)}$	5.0	1400	480	–	ns
			10	500	160	–	
			15	375	110	–	
Data Setup Time	7	$t_{su(D)}$	5.0	3600	1200	–	ns
			10	1800	600	–	
			15	1350	420	–	
Write Enable Hold Time	7	$t_{h(\overline{WE})}$	5.0	150	50	–	ns
			10	60	20	–	
			15	45	15	–	
Write Enable Setup Time	7	$t_{su(\overline{WE})}$	5.0	720	240	–	ns
			10	240	80	–	
			15	180	55	–	
Write Enable to D_{out} Disable**	4	$t_{\overline{WE}}$	5.0	720	240	–	ns
			10	240	80	–	
			15	180	55	–	
Strobe or $\overline{CE2}$ Pulse Width When Reading	4, 5, 6	$t_{WL(R)}$	5.0	1350	450	–	ns
			10	450	150	–	
			15	340	100	–	
Strobe, $\overline{CE1}$ or $\overline{CE2}$ Pulse Width When Writing	7	$t_{WL(W)}$	5.0	2400	1200	–	ns
			10	1260	600	–	
			15	945	420	–	
Write Recovery Time	4	$t_{R(W)}$					ns
t_W = (1.4 ns/pF) C_L + 219 ns			5.0	70	240	720	
t_W = (0.7 ns/pF) C_L + 70 ns			10	25	80	240	
t_W = (0.5 ns/pF) C_L + 47.5 ns			15	20	55	180	
$\overline{CE1}$ or $\overline{CE2}$ to D_{out} Disable Delay**	6	$t_{\overline{CE}_n}$	5.0	70	300	900	ns
			10	25	100	300	
			15	20	70	225	
Read Setup Time	4, 5	$t_{su(R)}$	5.0	0	-100	–	ns
			10	0	-40	–	
			15	0	-30	–	
Read Hold Time	4, 5	$t_{h(R)}$	5.0	540	180	–	ns
			10	240	60	–	
			15	180	45	–	
Read Cycle Time	4, 5	$t_{cyc(R)}$	5.0	–	2500	6000	ns
			10	–	700	2100	
			15	–	500	1575	
Write Cycle Time	7	$t_{cyc(W)}$	5.0	–	1400	4800	ns
			10	–	700	2100	
			15	–	500	1575	

* The formula given is for the typical characteristics only.

**10% output change into a 1.0 kΩ load.

FIGURE 1 – TYPICAL OUTPUT SOURCE AND SINK CURRENT CHARACTERISTICS TEST CIRCUIT



Input	Output Source Characteristics	Output Sink Characteristics
$\overline{WE}$	Pulse Once	Pulse Once
D_{in}	SW1 in Position 1	SW1 in Position 2
V_{GS}	$-V_{DD}$	V_{DD}
V_{DS}	$V_{out} - V_{DD}$	V_{out}

FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

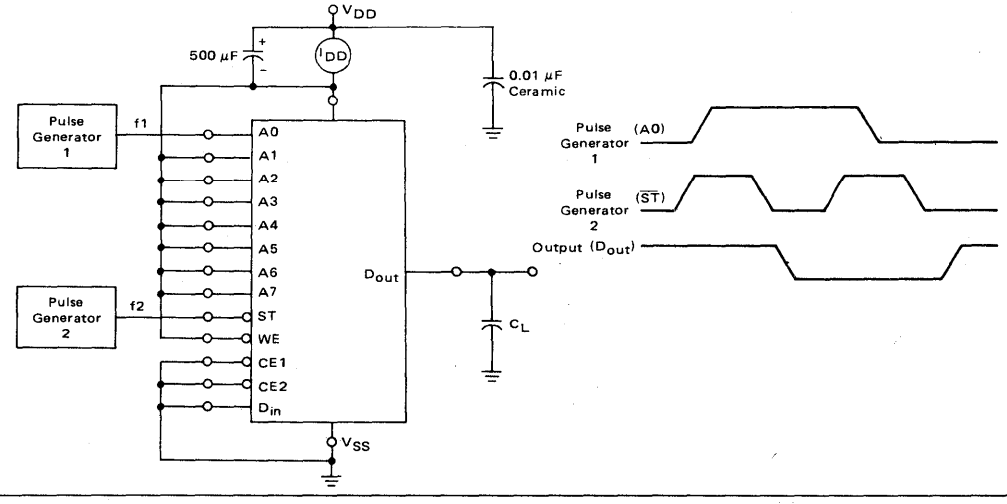
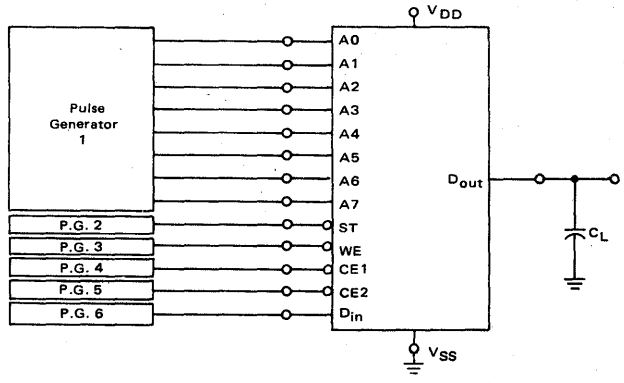
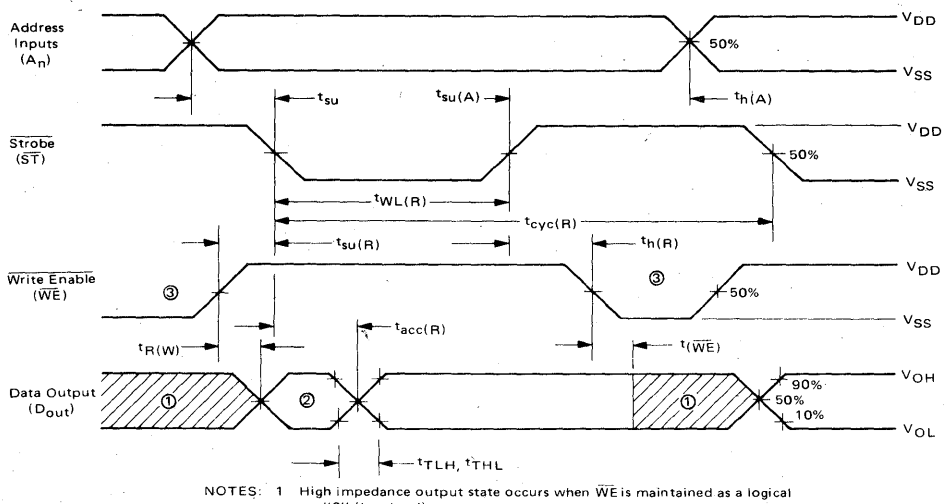


FIGURE 3 – AC TEST CIRCUIT



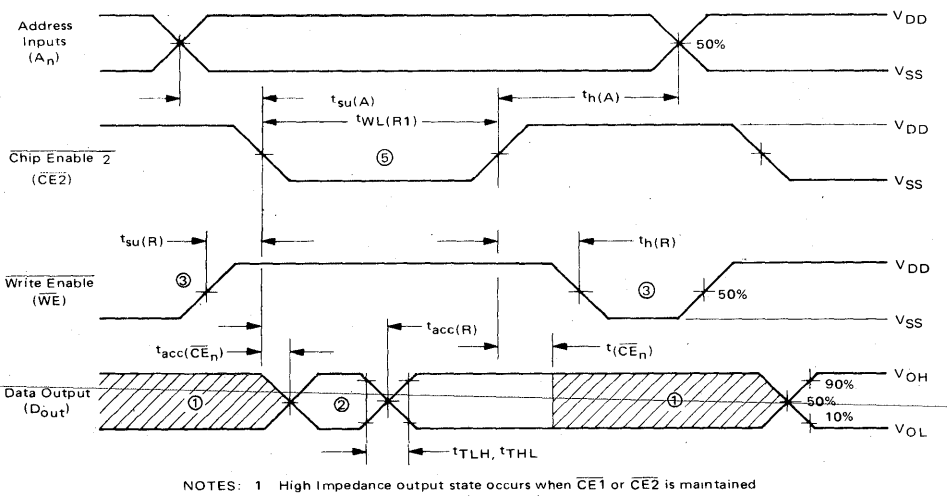
3

FIGURE 4 – READ CYCLE WAVEFORMS UTILIZING STROBE-TO-ACCESS MEMORY



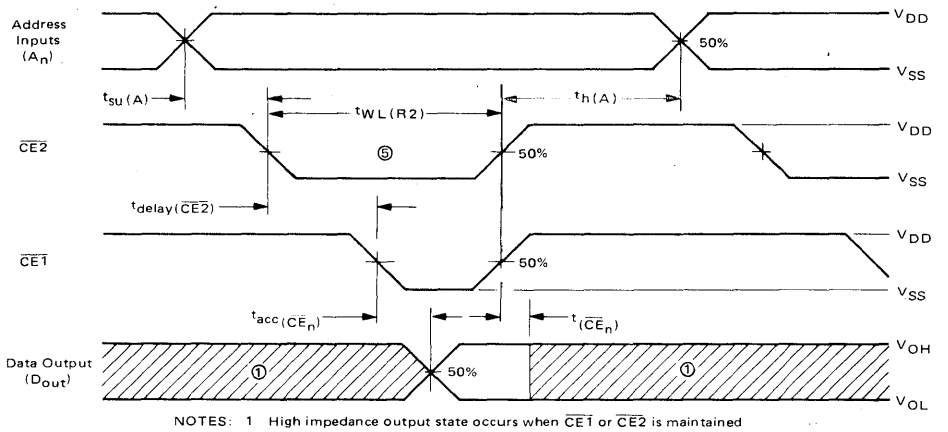
NOTES: 1 High impedance output state occurs when $\overline{WE}$ is maintained as a logical "0" (low level).
2 The output momentarily displays data from the previous state.
3 For read operation, $\overline{WE}$ may be maintained at a logical "1" (high level) during the complete cycle.
4 $\overline{CE1}$ and $\overline{CE2}$ are maintained at a logical "0" state (low level).
5 All input rise and fall times are 20 ns.

FIGURE 5 – READ CYCLE WAVEFORMS UTILIZING $\overline{CE2}$ FOR ACCESS MEMORY



NOTES: 1 High impedance output state occurs when $\overline{CE1}$ or $\overline{CE2}$ is maintained in the logical "1" state (high level).
2 The output momentarily displays data from the previous state.
3 For read operation, $\overline{WE}$ may be maintained at a logical "1" (high level) during the complete cycle.
4 All input rise and fall times are 20 ns.
5 $t_{WL(R1)} \geqslant t_{acc}$ (R) max

FIGURE 6 – READ CYCLE WAVEFORMS UTILIZING $\overline{CE1}$ AND $\overline{CE2}$ TO ACCESS MEMORY

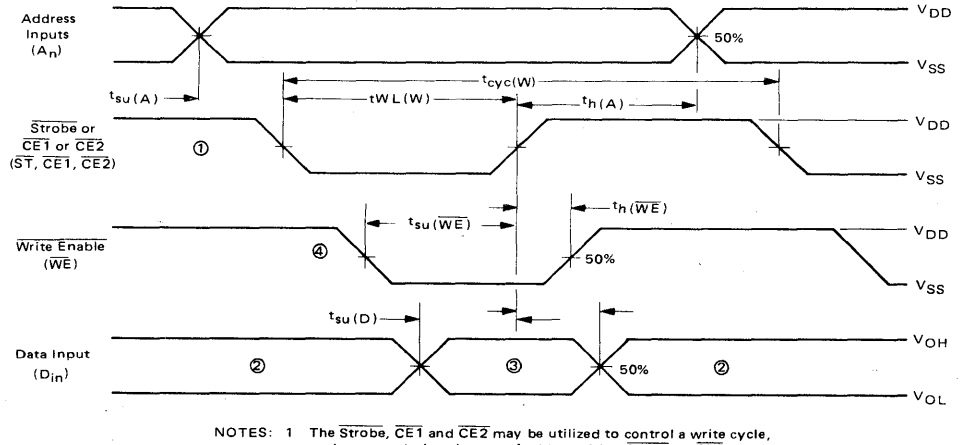


NOTES:
1. High impedance output state occurs when $\overline{CE1}$ or $\overline{CE2}$ is maintained in the logical "1" state (high level).
2. $\overline{WE}$ is maintained at the logical "1" state for this example.
3. All input rise and fall times are 20 ns
4. $t_{delay(\overline{CE2})}$ minimum assuares that only data presently addressed will appear at the output.

$$t_{delay(\overline{CE2})\ min.} = t_{acc_R\ max.} - t_{acc(\overline{CE1})\ min.}$$

5. $t_{WL(R2)} \geqslant t_{delay\ (\overline{CE2})\ min} + t_{acc\ (CE_n)\ max}$

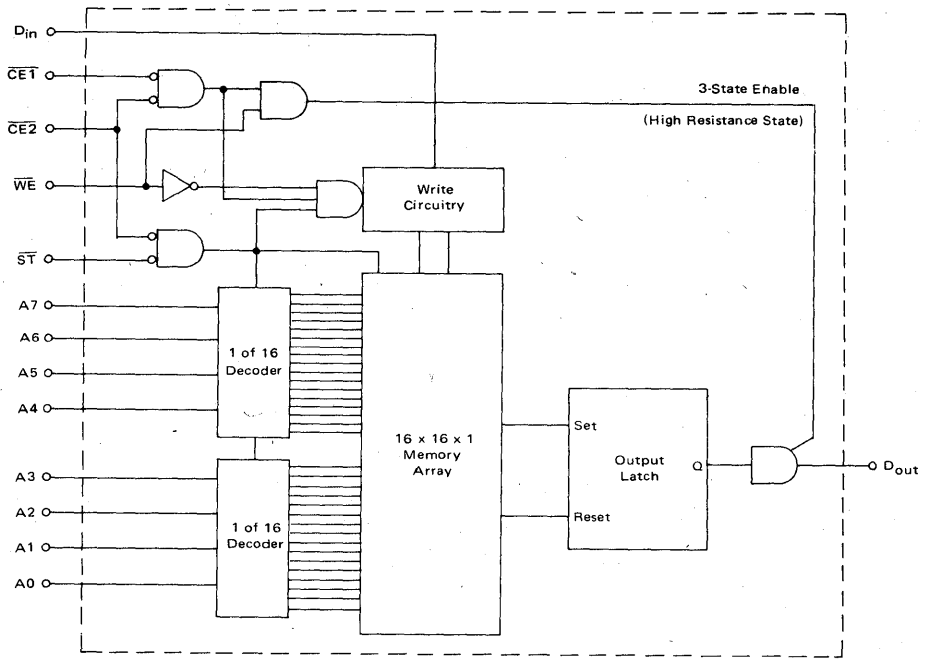
FIGURE 7 – WRITE CYCLE WAVEFORMS



NOTES:
1. The Strobe, $\overline{CE1}$ and $\overline{CE2}$ may be utilized to control a write cycle, however, during changes of address either Strobe or $\overline{CE2}$ must be in the logical "1" state (high level).
2. Data input logic level is don't care during the indicated intervals.
3. Data input logic level must remain fixed.
4. Write Enable may be maintained as a logical "0" during the write cycle.
5. All input rise and fall times are 20 ns.

3

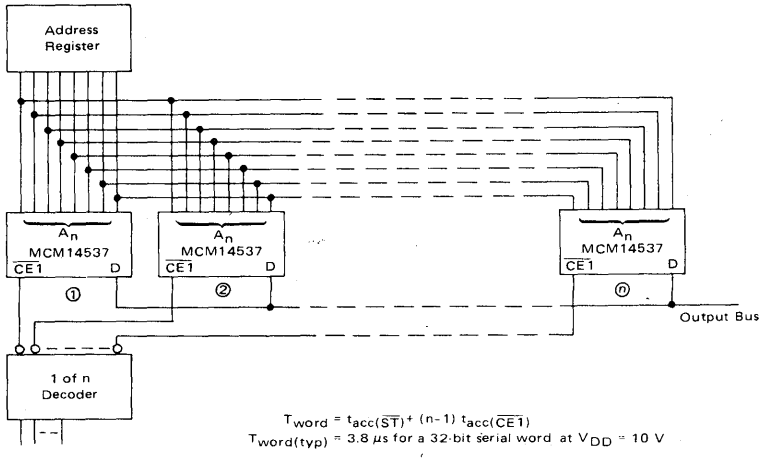
LOGIC/BLOCK DIAGRAM



FUNCTION	$\overline{CE1}$	$\overline{CE2}$	$\overline{ST}$	$\overline{WE}$	D_{in}	D_{out}	COMMENTS
Address changing valid	X	X	1	X	X	R/A	D_{out} will be active if $\overline{CE1}$ and $\overline{CE2}$ = "0" and $\overline{WE}$ = "1".
	X	1	X	X	X	R	$\overline{CE2}$ = "1", fully disables internal logic and output.
Address changing not valid	X	0	0	X	X	R/A	Changing address in this mode may result in altered data.
D_{out} disabled in high resistance state	1	X	X	X	X	R	$\overline{CE1}$ = "1" disables write cycle and D_{out}.
	X	1	X	X	X	R	The chip is fully disabled.
	X	X	X	0	X	R	$\overline{WE}$ = "0" enables writing into memory if $\overline{CE1}$, $\overline{CE2}$, and $\overline{ST}$ = "0".
D_{out} enabled in active state	0	0	X	1	X	A	If $\overline{ST}$ = "1", the output stores and reads the previous data from or written into memory.
Read addressed memory location into output latch.	0	0	0	1	X	A	The output reads the present contents that are addressed.
	1	0	0	1	X	R	The addressed location is read into output latch with output in the "R" state.
Disable reading from memory	X	1	X	X	X	R	Address changing can take place in this condition.
	X	X	1	X	X	R/A	
Write into memory	0	0	0	0	A	R	D_{in} is written into memory and into the output latch
Write disabled	1	X	X	X	X	R	$\overline{WE}$ = "1" is a read enable.
	X	1	X	X	X	R	$\overline{WE}$ = "0" is a write enable.
	X	X	1	X	X	R/A	
	X	X	X	1	X	R/A	

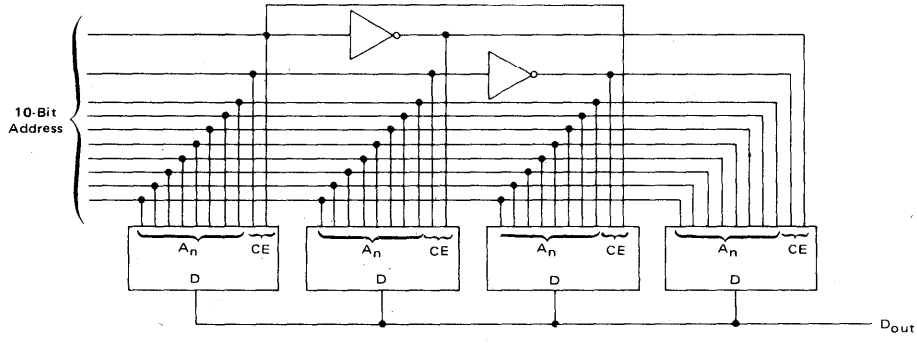
R = High resistance state at D_{out}
A = An active level of either V_{SS} or V_{DD}
R/A = An R or A condition depending on the don't care condition
X = Don't care condition (must be in the "1" or "0" state)
1 = A high level at V_{DD}
0 = A low level at V_{SS}

TYPICAL APPLICATION FOR SERIAL WORDS UTILIZING BUS TECHNIQUES

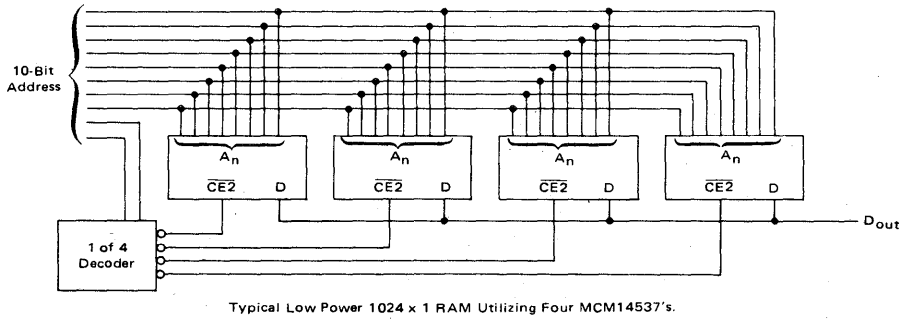


$T_{word} = t_{acc(\overline{ST})} + (n-1)\, t_{acc(\overline{CE1})}$

$T_{word(typ)} = 3.8\ \mu s$ for a 32-bit serial word at $V_{DD} = 10$ V



Typical 1024 x 1 RAM Utilizing Four MCM14537's.



Typical Low Power 1024 x 1 RAM Utilizing Four MCM14537's.

MOTOROLA

MCM14552

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

256-BIT (64 x 4) STATIC RANDOM ACCESS MEMORY

256-BIT STATIC RANDOM ACCESS MEMORY

The MCM14552 is a static random access memory (RAM) organized in a 64 x 4 bit pattern. The three chip enable inputs can be used as extensions of the six address inputs, creating 9-bit address scheme. Eight MCM14552 devices may be used to comprise a 2048-bit memory (512 x 4) without additional address decoding.

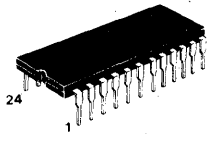
The mode control (M) is used to change the control logic characteristic of the circuit. For example, with M high, the 3-state input (T) fully controls the 3-state characteristic of the output. With M low, the output 3-state characteristic is controlled by chip enable inputs (CE), write enable input (WE) and T.

The memory is designed so that dc signals may operate the memory, with no maximum pulse width restrictions.

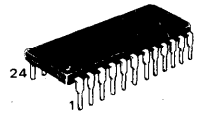
Medium speed, micropower operation, and control flexibility make the device useful in scratch pad or buffer applications where battery operation or high noise immunity are required.

- Quiescent Current = 50 μA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- 3-state Output Capability for Memory Expansion
- Output Data Latch Eliminates Need for Storage Buffer
- Access Time = 700 ns typical @ V_{DD} = 10 Vdc
- Fully Decoded and Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

NOTE: Pin 20(LE)) must be connected to V_{SS}



L SUFFIX
CERAMIC PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

MCM14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

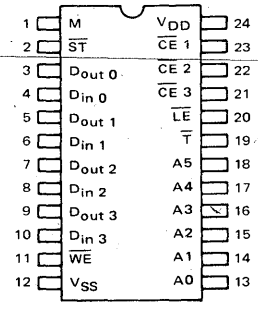
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device	T_A	-55 to +125	°C
CL/CP Device		-40 to +85	
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}.

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±1.0	–	±0.00001	±1.0	–	±14.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–		–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.050	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.100	10	–	300	
		15	–	20	–	0.150	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	50	–	0.050	50	–	375	µAdc
(Per Package)		10	–	100	–	0.100	100	–	750	
		15	–	200	–	0.150	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.98 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (3.96 µA/kHz) f + I_{DD}							
		15	I_T = (5.86 µA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	µAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†*To calculate total supply current at loads other than 50 pF:*
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Figure	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	1	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns			5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 25 ns			10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns			15	–	65	130	
Output Fall Time	1	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns			5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns			10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns			15	–	40	80	
Read Cycle Time	1, 2	$t_{cyc(R)}$	5.0	–	2000	6000	ns
			10	–	750	2200	
			15	–	500	1650	
Write Cycle Time	3, 4	$t_{cyc(W)}$	5.0	–	1200	3600	ns
			10	–	750	2200	
			15	–	500	1650	
Address to $\overline{\text{Strobe}}$ Setup Time	1, 3	$t_{su(A\text{-}\overline{ST})}$	5.0	1500	500	–	ns
			10	450	150	–	
			15	350	120	–	
$\overline{\text{Strobe}}$ to Address Hold Time	1, 3	$t_{h(\overline{ST}\text{-}A)}$	5.0	150	50	–	ns
			10	100	0	–	
			15	75	0	–	
Address to $\overline{\text{Chip Enable}}$ Serup Time	2, 4	$t_{su(A\text{-}\overline{CE})}$	5.0	1800	600	–	ns
			10	600	200	–	
			15	450	150	–	
$\overline{\text{Chip Enable}}$ to Address Hold Time	2, 4	$t_{h(\overline{CE}\text{-}A)}$	5.0	450	150	–	ns
			10	300	100	–	
			15	225	75	–	
$\overline{\text{Strobe}}$ or $\overline{\text{Chip Enable}}$ Pulse Width When Reading	1, 2	$t_{WL(R)}$	5.0	1800	450	–	ns
			10	450	150	–	
			15	350	100	–	
$\overline{\text{Strobe}}$ or $\overline{\text{Chip Enable}}$ Pulse Width When Writing	3, 4	$t_{WL(W)}$	5.0	3600	1200	–	ns
			10	1800	600	–	
			15	1350	400	–	
Read Setup Time	1	$t_{su(R)}$	5.0	0	-100	–	ns
			10	0	-40	–	
			15	0	-30	–	
Read Hold Time	1	$t_{h(R)}$	5.0	540	180	–	ns
			10	240	60	–	
			15	180	45	–	
Data Setup Time	3, 4	$t_{su(D)}$	5.0	1800	600	–	ns
			10	600	200	–	
			15	450	150	–	
Data Hold Time	3, 4	$t_{h(D)}$	5.0	600	200	–	ns
			10	150	50	–	
			15	120	30	–	

*The formula given is for the typical characteristics only.

(continued)

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C) (continued)

Characteristic	Figure	Symbol	V_{DD}	Min	Typ	Max	Unit
Write Enable Setup Time	3, 4	$t_{su(\overline{WE})}$	5.0	720	240	–	ns
			10	240	80	–	
			15	180	55	–	
Write Enable Hold Time	3, 4	$t_{h(\overline{WE})}$	5.0	150	50	–	ns
			10	60	20	–	
			15	45	15	–	
Read Access Time from Strobe	1, 3	$t_{acc(R\text{-}\overline{ST})}$	5.0	–	2000	6000	ns
			10	–	700	2100	
			15	–	350	1600	
Read Access Time from Chip Enable	2	$t_{acc(R\text{-}\overline{CE})}$	5.0	–	2100	6300	ns
			10	–	750	2250	
			15	–	400	1700	
Output Enable/Disable Delay from Chip Enable or Write Enable	2, 4	$t_{R(\overline{CE})}$, $t_{R(\overline{WE})}$	5.0	–	400	1200	ns
			10	–	200	600	
			15	–	150	450	
Three-State Enable/Disable Output Delay	2	$t_{(\overline{T})}$	5.0	–	400	1200	ns
			10	–	160	480	
			15	–	120	360	
Latch to Output Propagation Delay	1	$t_{\overline{LE}}$	5.0	–	500	1500	ns
			10	–	200	600	
			15	–	150	450	

*The formula given is for the typical characteristics only.

3

LOGIC DIAGRAM

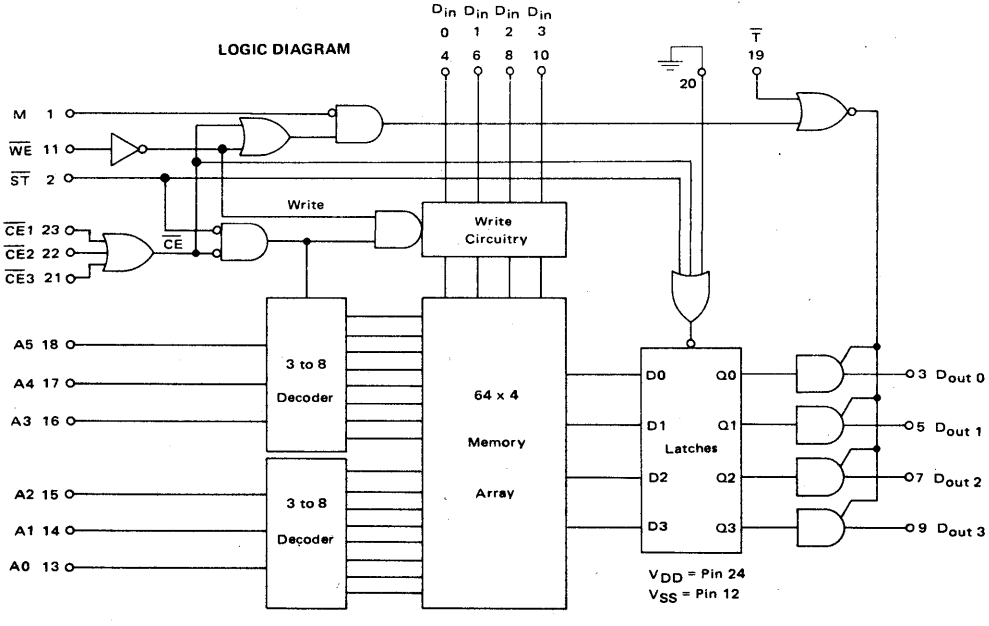
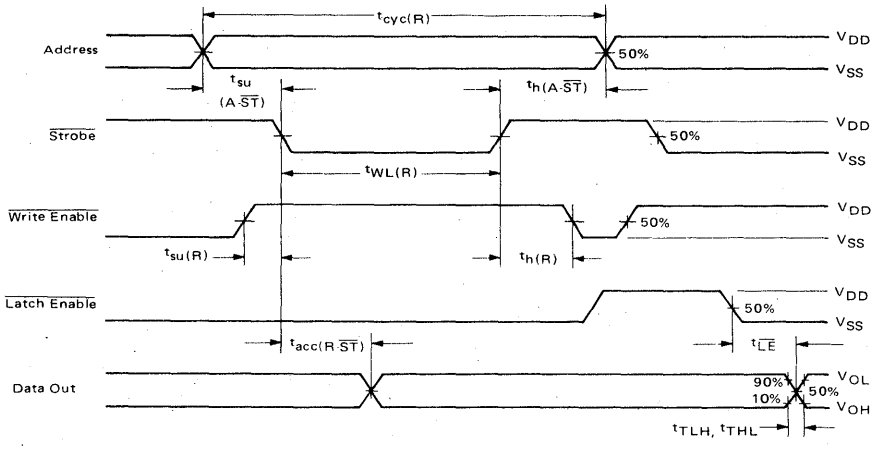
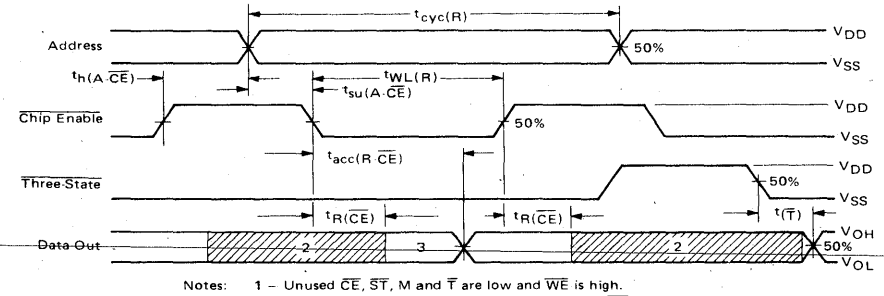


FIGURE 1 – READ CYCLE WAVEFORMS UTILIZING STROBE TO ACCESS MEMORY



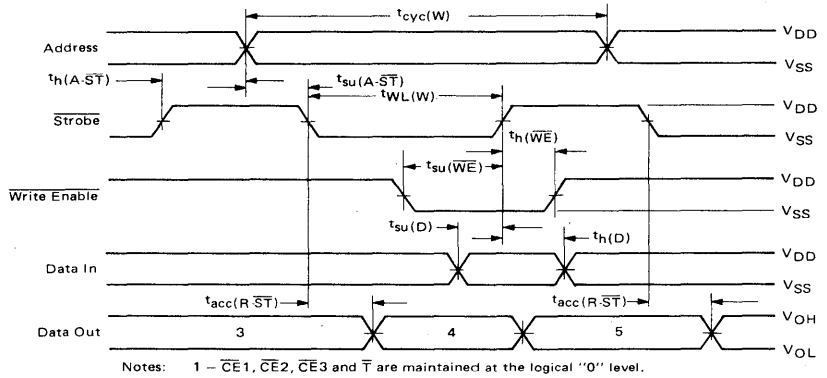
Notes: 1 – $\overline{CE}1$, $\overline{CE}2$, $\overline{CE}3$ and $\overline{T}$ are low, M is high.
2 – $\overline{WE}$ may be held high during the complete read cycle.

FIGURE 2 – READ CYCLE WAVEFORMS UTILIZING CHIP ENABLE TO ACCESS MEMORY



Notes: 1 – Unused $\overline{CE}$, $\overline{ST}$, M and $\overline{T}$ are low and $\overline{WE}$ is high.
2 – High impedance output state occurs when any $\overline{CE}$ is high and M is low, or when $\overline{T}$ is high.
3 – The output displays data from the previous state.
4 – $t_{WL(R)} \geq t_{acc(R\text{-}\overline{CE})max}$.

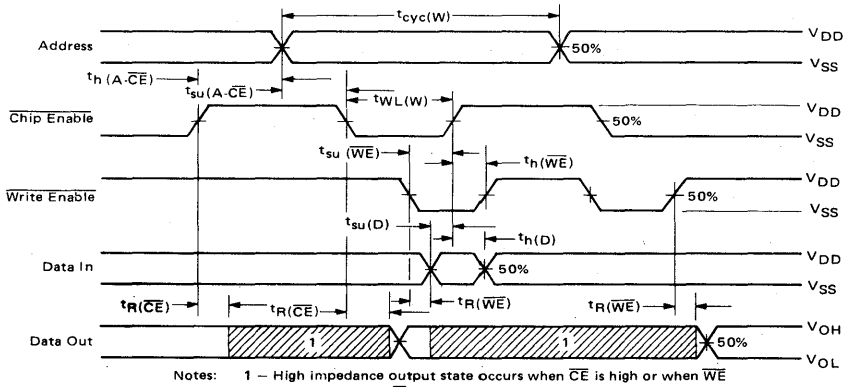
FIGURE 3 – WRITE CYCLE WAVEFORMS UTILIZING STROBE



Notes:
1 – $\overline{CE}1$, $\overline{CE}2$, $\overline{CE}3$ and $\overline{T}$ are maintained at the logical "0" level.
2 – M is maintained at the logical "1" level.
3 – The output displays the contents of the previous state.
4 – The output displays the contents of the presently addressed location as in a read modify write cycle.
5 – The output displays the data that was written into addressed location.

3

FIGURE 4 – WRITE CYCLE WAVEFORM UTILIZING CHIP ENABLE



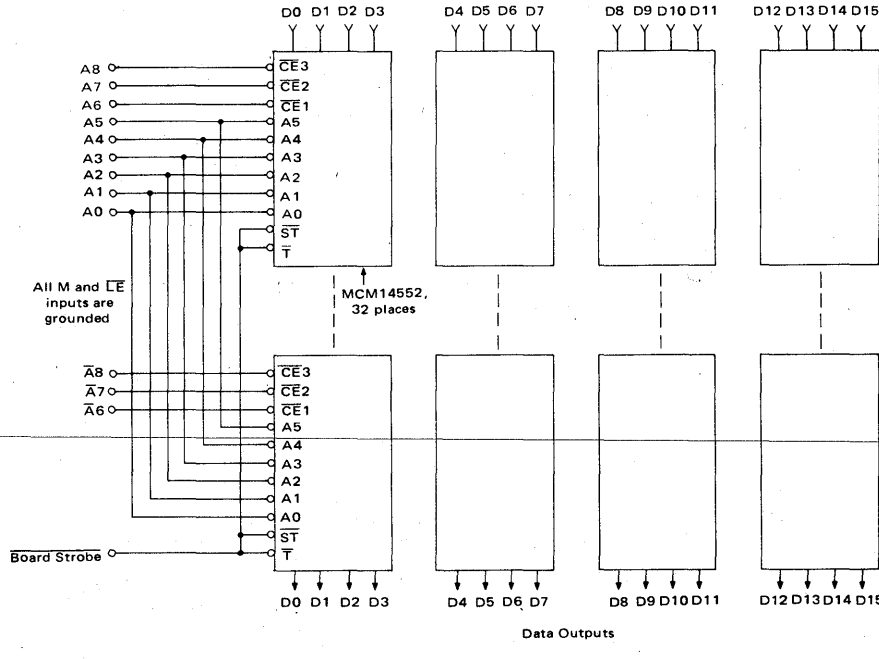
Notes:
1 – High impedance output state occurs when $\overline{CE}$ is high or when $\overline{WE}$ is low, for M and $\overline{T}$ maintained in the low state.
2 – Unused $\overline{CE}$'s, $\overline{ST}$, M and $\overline{T}$ are maintained at the logical "0" level.

TRUTH TABLE

Function	$\overline{CE}$ 1	$\overline{CE}$ 2	$\overline{CE}$ 3	$\overline{T}$	$\overline{LE}$	M	$\overline{ST}$	$\overline{WE}$	D_{in}	D_{out}	Comments
Address Changing Valid	X	X	X	X	X	X	1	X	X	R/A	D_{out} will be active if all $\overline{CE}$ = 0, $\overline{T}$ = 0 and $\overline{WE}$ = 1 or if M = 1 and $\overline{T}$ = 0
	X	X	1	X	X	X	X	X	X	R/A	
	X	1	X	X	X	X	X	X	X	R/A	
	1	X	X	X	X	X	X	X	X	R/A	
Address Changing Not Valid	0	0	0	X	X	X	0	X	X	R/A	D_{out} will be active if $\overline{T}$ = 0 and $\overline{WE}$ = 1 or if M = 1 and $\overline{T}$ = 0
D_{out} Disabled (in high resistance state)	X	X	1	X	X	0	X	X	X	R	Disables write circuitry
	X	1	X	X	X	0	X	X	X	R	
	1	X	X	X	X	0	X	X	X	R	
	X	X	X	1	X	X	X	X	X	R	$\overline{T}$ = 1 always disables D_{out}
	X	X	X	X	X	0	X	0	X	R	M = 0 and write operation disables D_{out}
D_{out} Enabled (in active state)	0	0	0	0	X	X	X	1	X	A	Read operation, D_{out} active
	X	X	X	0	X	1	X	X	X	A	Read or write, D_{out} active
Read Addressed Memory Location Into Output Latch	0	0	0	X	0	X	0	X	X	R/A	If $\overline{WE}$ = 0, D_{in} = D_{out}
Disable Reading From Memory	X	X	1	X	X	X	X	X	X	R/A	
	X	1	X	X	X	X	X	X	X	R/A	
	1	X	X	X	X	X	X	X	X	R/A	
	X	X	X	X	X	X	1	X	X	R/A	
	X	X	X	X	X	X	X	0	X	R/A	
Write Into Memory	0	0	0	X	X	X	0	0	A	R/A	
Write Disabled	X	X	1	X	X	X	X	X	X	R/A	
	X	1	X	X	X	X	X	X	X	R/A	
	1	X	X	X	X	X	X	X	X	R/A	
	X	X	X	X	X	X	1	X	X	R/A	
	X	X	X	X	X	X	X	1	X	R/A	
Output Latch Enabled	0	0	0	X	0	X	0	X	X	R/A	
Output Latch Disabled	X	X	1	X	X	X	X	X	X	R/A	
	X	1	X	X	X	X	X	X	X	R/A	
	1	X	X	X	X	X	X	X	X	R/A	
	X	X	X	X	1	X	X	X	X	R/A	
	X	X	X	X	X	X	1	X	X	R/A	

R = High resistance state at D_{out}
A = An active level of either V_{DD} or V_{SS}
R/A = An R or A condition depending on the don't care condition.
X = Don't care condition (must be in the "1" or "0" state).
1 = A high level at V_{DD}.
0 = A low level at V_{SS}.

FIGURE 5 – 512 WORD x 16 BIT MEMORY BOARD



MOTOROLA

MCM145101

256 X 4 BIT STATIC RAM

The MCM145101 family of CMOS RAMs offers ultra low power and fully static operation with a single 5 volt supply. The CMOS 1024-bit devices are organized in 256 words by 4 bits. Separate data inputs and data outputs permit maximum flexibility in bus-oriented systems. Data retention at a power supply as low as 2.0 volts over temperature readily allows design into applications using battery backup for nonvolatility. The MCM145101 is fully static and does not require clocking in standby mode.

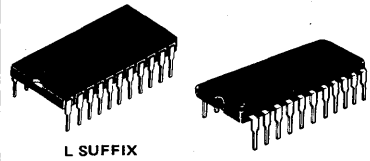
The MCM145101 is fabricated using the Motorola advanced ion-implanted, silicon-gate technology for high performance and high reliability.

- Low Standby Power
- Fast Access Time
- Single + 5.0 Volt Supply
- Fully TTL Compatible—All Inputs and Outputs
- Three-State Output
- Fully Static Operation
- Data Retention to 2.0 Volts
- Direct Replacement for:
  - Intel 5101 Series
  - AMI S5101 Series
  - Hitachi MH435101 Series
- Pin Replacement for Harris HM6501 Series

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

1024-BIT STATIC
RANDOM ACCESS MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 736

P SUFFIX
PLASTIC PACKAGE
CASE 708

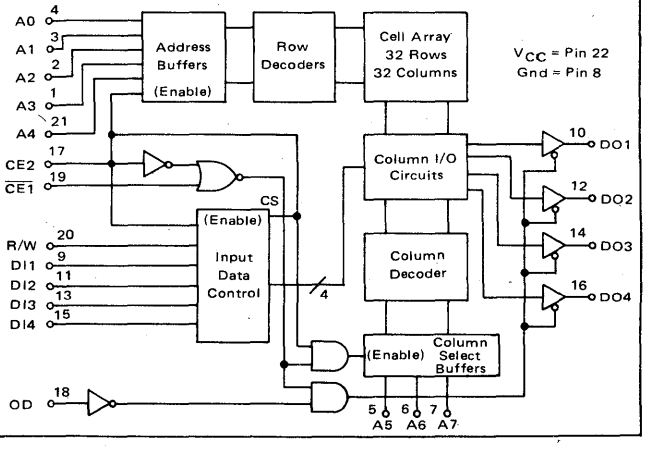
ORDERING INFORMATION

MCM14XXXX — Suffix Denotes
- L
- P
- -1
- -3
- -8
- (Not Used)

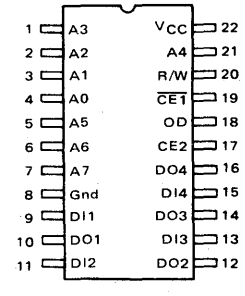
Selections for speed and power (see table)

Type Number	Typical Current @ 2 Vdc (μA)	Typical Current @ 5 Vdc (μA)	Max Access (ns)
MCM145101L, MCM145101P	0.14	0.2	650
MCM145101-1L, MCM145101-1P	0.14	0.2	450
MCM145101-3L, MCM145101-3P	0.70	1.0	650
MCM145101-8L, MCM145101-8P	–	10	800

BLOCK DIAGRAM



PIN ASSIGNMENT



TRUTH TABLE

$\overline{CE1}$	CE2	OD	R/W	D_{In}	Output	Mode
H	X	X	X	X	High Z	Not Selected
X	L	X	X	X	High Z	Not Selected
X	X	H	H	X	High Z	Output Disabled
L	H	H	L	X	High Z	Write
L	H	L	L	X	D_{In}	Write
L	H	L	H	X	D_{Out}	Read

3

MAXIMUM RATINGS (Voltages referenced to V_{SS} Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	-0.5 to +7.0	Vdc
Voltage on Any Pin	V_{in}	-0.3 to V_{CC} +0.3	Vdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

DC CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = 5 V ±5%)

Characteristic	Symbol	MCM145101,-1			MCM145101-3			MCM145101-8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Current	I_{in}(2)	–	5.0	–	–	5.0	–	–	5.0	–	nAdc
Input High Voltage	V_{IH}	2.2	–	V_{CC}	2.2	–	V_{CC}	2.2	–	V_{CC}	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.65	-0.3	–	0.65	-0.3	–	0.65	Vdc
Output High Voltage (I_{OH} = -1.0 mA)	V_{OH}	2.4	–	–	2.4	–	–	2.4	–	–	Vdc
Output Low Voltage (I_{OL} = 2.0 mA)	V_{OL}	–	–	0.4	–	–	0.4	–	–	0.4	Vdc
Output Leakage Current ($\overline{CE1}$ = 2.2 V, V_{OL} = 0 V to V_{CC})	I_{LO}(2)	–	–	±1.0	–	–	±1.0	–	–	±2.0	μAdc
Operating Current (V_{in} = V_{CC}, except $\overline{CE1}$ ≤ 0.65 V, outputs open)	I_{CC1}	–	9.0	22	–	9.0	22	–	11	25	mAdc
Operating Current (V_{in} = 2.2 V, except $\overline{CE1}$ ≤ 0.65 V, outputs open)	I_{CC2}	–	13	27	–	13	27	–	15	30	mAdc
Standby Current (CE2 ≤ 0.2 V)	I_{CCL}(2),(4)	–	–	10	–	–	200	–	–	500	μAdc

CAPACITANCE

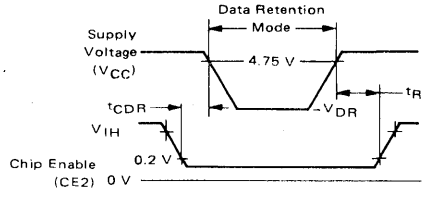
Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	4.0	8.0	pF
Output Capacitance (V_{out} = 0 V)	C_{out}	8.0	12.0	pF

LOW V_{CC} DATA RETENTION CHARACTERISTICS (Excluding MCM145101-8) T_A = 0°C to 70°C

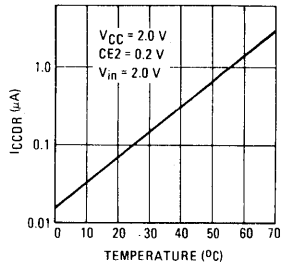
Parameter	Test Conditions		Symbol	Min	Typ.(1)	Max	Units
V_{CC} for Data Retention	CE2 ≤ 0.2 V		V_{DR}	2.0	–	–	Vdc
MCM145101 or MCM145101-1 Data Retention Current		V_{DR} = 2.0 V,	I_{CCDR1}	–	0.14	10	μAdc
MCM145101-3 Data Retention Current		V_{DR} = 2.0 V,	I_{CCDR2}	–	0.70	200	μAdc
Chip Deselect to Data Retention Time			t_{CDR}	0	–	–	ns
Operation Recovery Time			t_R	t_{RC}(3)	–	–	ns

NOTES: 1. Typical values are T_A = 25°C and nominal supply voltage.
2. Current through all inputs and outputs included in I_{CCL} measurement.
3. t_{RC} = Read Cycle Time.
4. Low current state is for CE2 = 0 only.

LOW V_{CC} DATA RETENTION WAVEFORM



TYPICAL I_{CCDR} versus TEMPERATURE



AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted)

AC TEST CONDITIONS

Condition	Value
Input Pulse Levels	+0.65 V to 2.2 V
Input Rise and Fall Times	20 ns
Output Load — 1 TTL Gate and C_L = 100 pF	
Timing Measurement Reference Level	1.5 Volt

3

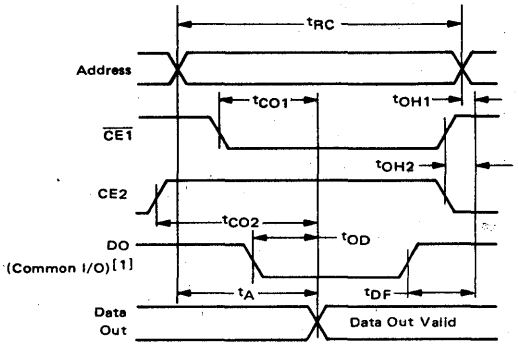
READ CYCLE

Parameter	Symbol	MCM145101-1		MCM145101,-3		MCM145101-8	
		Min	Max	Min	Max	Min	Max
Read Cycle	t_{RC}	450	–	650	–	800	–
Access Time	t_A	–	450	–	650	–	800
Chip Enable ($\overline{CE1}$) to Output	t_{CO1}	–	400	–	600	–	800
Chip Enable (CE2) to Output	t_{CO2}	–	500	–	700	–	850
Output Disable to Output	t_{OD}	–	250	–	350	–	450
Data Output to High Z State	t_{DF}	0	130	0	150	0	200
Previous Read Data Valid with Respect to Address Change	t_{OH1}	0	–	0	–	0	0
Previous Read Data Valid with Respect to Chip Enable	t_{OH2}	0	–	0	–	0	0

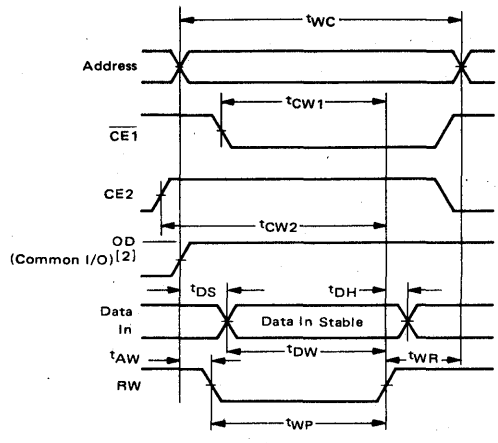
WRITE CYCLE

Write Cycle	t_{WC}	450	–	650	–	800	–
Write Delay	t_{AW}	130	–	150	–	200	–
Chip Enable ($\overline{CE1}$) to Write	t_{CW1}	350	–	550	–	650	–
Chip Enable (CE2) to Write	t_{CW2}	350	–	550	–	650	–
Data Setup	t_{DW}	250	–	400	–	450	–
Data Hold	t_{DH}	50	–	100	–	100	–
Write Pulse	t_{WP}	250	–	400	–	450	–
Write Recovery	t_{WR}	50	–	50	–	100	–
Output Disable Setup	t_{DS}	130	–	150	–	200	–

READ CYCLE TIMING



WRITE CYCLE TIMING



NOTES: 1. OD may be tied low for separate I/O operation.
2. During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.

3

MOTOROLA

MCM146504

Product Preview

4096X1-BIT STATIC RANDOM ACCESS MEMORIES

The MCM146504 is a 4096X1-bit static random access memory, fabricated with high density, high reliability CMOS silicon-gate technology. The device has TTL compatible inputs and outputs. It is designed to retain data at low supply voltages, to further reduce supply current requirements.

The MCM146504 is useful in memory applications where low-power and non-volatility is required. It is assembled in 18 pin dual in-line package with the industry standard pin-outs.

- Single Low Voltage Power Supply
- Static Operation
- Industry Standard 18-Pin Configuration
- Fully TTL Compatible
- Common Data Input and Output Capability
- Three-State Outputs
- Low Power Dissipation – Standby 10 mW (Typical)
- Ideal for Battery Backup Operation
- Access Time – 450 ns (Maximum)
- Pinout and Functional Replacement for
  Harris – HM6504
  Intersil – IM6504

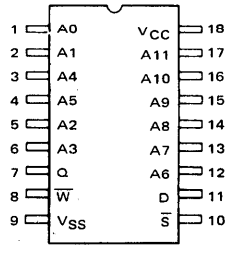
CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

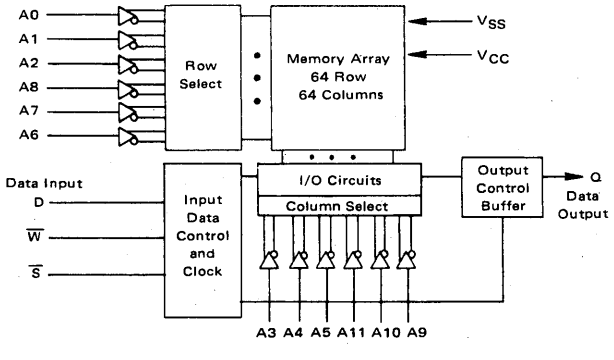
4096X1-BIT STATIC RANDOM ACCESS MEMORIES

3

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A11	Address Input
D	Data Input
Q	Data Output
$\overline{S}$	Chip Select
V_{CC}	Power Supply (+5 V)
V_{SS}	Ground
$\overline{W}$	Write Enable

TRUTH TABLE

$\overline{S}$	$\overline{W}$	D	Q	Mode
H	X	X	HI-Z	Not Selected
L	L	L	HI-Z	Write "0"
L	L	H	HI-Z	Write "1"
L	H	X	Output data	Read

This is advance information and specifications are subject to change without notice.

MOTOROLA

MCM146508
MCM146518

Advance Information

1024 X 1 BIT STATIC RANDOM ADDRESS MEMORY

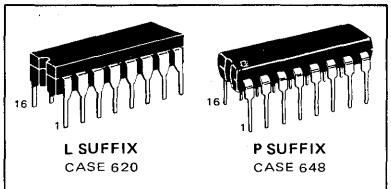
The MCM146508 and MCM146518 are fully static 1024 X 1 RAMS fabricated using high performance silicon gate CMOS technology. They offer low-power operation from a single 5.0 V supply with data retention to 2.0 V. The MCM146508 has the two select lines and the enable line brought out as a single enable line.

- Low Standby and Operating Power
- Single 5.0 V Supply
- Data Retention to 2.0 V
- Fast Access Time
- Address Latches
- Three-State Outputs
- Fully TTL Compatible Inputs/Outputs
- Fully Static Operation
- Direct Replacement for
  Harris HM6508/HM6518
  Intersil IM6508/IM6518

CMOS LSI

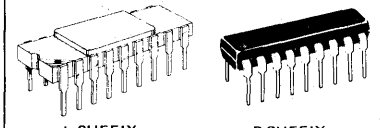
(LOW-POWER COMPLEMENTARY MOS)

1024 X 1 BIT STATIC
RANDOM ACCESS MEMORY



L SUFFIX
CASE 620

P SUFFIX
CASE 648



L SUFFIX
CASE 680

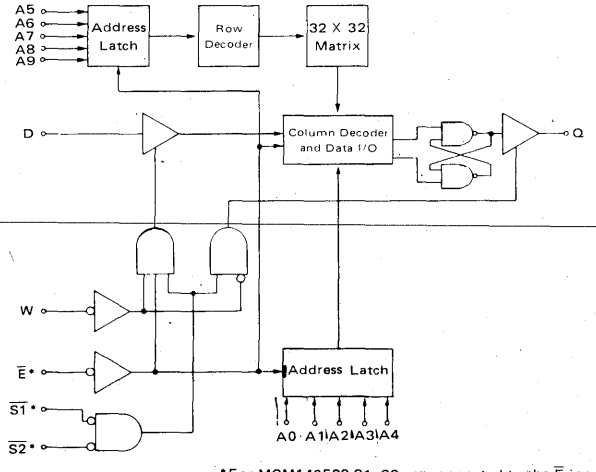
P SUFFIX
CASE 707

MCM14XXXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- See Table 1

TABLE 1

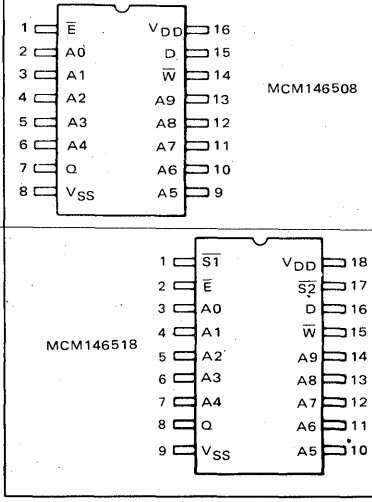
Type Number	Package Suffixes	Typical Current 2 Vdc	Typical Current 5 Vdc	Maximum Access Time	Operating Temperature Range
MCM146508/MCM146518	L/P	0.1 μA	5.0 μA	460 ns	-40 to +85°C
MCM146508-1/MCM146518-1	L/P	0.01 μA	1.0 μA	300 ns	-40 to +85°C
MCM146508-2/MCM146518-2	L	0.01 μA	1.0 μA	300 ns	-55 to +125°C

BLOCK DIAGRAM



*For MCM146508 S1, S2 are connected to the $\overline{E}$ input.

PIN ASSIGNMENT



This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +7.0	Vdc
Input Voltage, All Inputs	V_{in}	-0.3 to V_{DD} + 0.3	Vdc
Operating Temperature Range MCM146508/MCM146518 MCM146508-1/MCM146518-1 MCM146508-2/MCM146518-2	T_A	 -40 to +85 -40 to +85 -55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

DC CHARACTERISTICS (V_{DD} = 5.0 V ±10%, T_A = 25°C)

Characteristic	Symbol	MCM146508-1 MCM146518-1			MCM146508 MCM146518			MCM146508-2 MCM146518-2			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Current	I_{in}	–	5.0	–	–	5.0	–	–	5.0	–	nAdc
Input High Voltage	V_{IH}	V_{DD} - 2.0	–	V_{DD}	V_{DD} - 2.0	–	V_{DD}	–	–	V_{DD}	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.8	-0.3	–	0.8	-0.3	–	0.8	Vdc
Output High Voltage (I_{OH} = -1.0 mA)	V_{OH}	2.4	–	–	2.4	–	–	2.4	–	–	Vdc
Output Low Voltage (I_{OL} = 2.0 mA)	V_{OL}	–	–	0.4	–	–	0.4	–	–	0.4	Vdc
Output Leakage Current (V_{OL} = 0 V to V_{DD})	I_{OL}	–	–	±1.0	–	–	±1.0	–	–	±1.0	μAdc
Standby Current (V_{IH} = $\overline{E}$ = $\overline{S1}$ = $\overline{S2}$ = V_{DD})	I_{DDSB}	–	0.1	10	–	1.0	100	–	1.0	100	nAdc
Data Retention Current (V_{DD} = 2.2 V = V_{IH} = $\overline{E}$ = $\overline{S1}$ = $\overline{S2}$)	I_{DDDR}	–	0.1	1.0	–	0.1	10	–	0.1	10	μAdc
Operating Current (t_{ELEH} = 1.0 μs)	I_{DDOP}	–	–	–	–	–	–	–	–	–	mAdc

CAPACITANCE

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	4.0	8.0	pF
Output Capacitance (V_{out} = 0 V)	C_{out}	8.0	12	pF

AC OPERATING CONDITIONS

Condition	Value
Input Pulse Levels	+0.8 V to V_{DD} - 2.0 V
Input Rise and Fall Times	20 ns
Output Load	1 TTL Gate and C_L = 50 pF
Timing Measurement Reference Level	1.5 V
Supply Voltage	5.0 V ±10%
Temperature Range MCM146508/MCM146518 MCM146508-1/MCM146518-1 MCM146508-2/MCM146518-2	 -40°C to +85°C -40°C to +85°C -55°C to +125°C

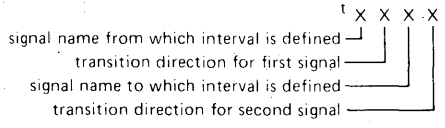
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

AC CHARACTERISTICS

Parameter	Symbol	MCM146508-1 MCM146518-1		MCM146508-2 MCM146518-2		MCM146508 MCM146518		Unit
		Min	Max	Min	Max	Min	Max	
Read or Write Cycle Time	t_{ELEL}	500	–	500	–	760	–	ns
Enable Pulse Width, Low	t_{ELEH}	300	–	300	–	460	–	ns
Enable Pulse Width, High	t_{EHEL}	200	–	200	–	300	–	ns
Enable Access Time	t_{ELQV}	–	300	–	300	–	460	ns
Address Setup	t_{AVEL}	7.0	–	7.0	–	15	–	ns
Address Hold	t_{ELAX}	90	–	90	–	150	–	ns
Data Setup	t_{DVWH}	200	–	200	–	300	–	ns
Data Hold	t_{WHDX}	0	–	0	–	0	–	ns
Write Pulse Width	t_{WLWH}	200	–	200	–	300	–	ns
Write Enable to Output Disable	t_{WLQZ}	–	180	–	180	–	285	ns
Output Disable (MC146508 Only)	t_{EHQZ}	–	180	–	180	–	285	ns
Output Disable (MC146518 Only)	t_{SHQZ}	–	180	–	180	–	285	ns
Write Disable to Output Enable	t_{WHQX}	–	180	–	180	–	285	ns
Output Enable (MC146508 Only)	t_{ELQX}	–	180	–	180	–	285	ns
Output Enable (MC146518 Only)	t_{SLQX}	–	180	–	180	–	285	ns
Select to Write Pulse Setup	t_{WLSH}	200	–	200	–	300	–	ns
Select to Write Pulse Hold	t_{SLWH}	200	–	200	–	300	–	ns
Enable to Write Pulse Setup	t_{WLEH}	200	–	200	–	300	–	ns
Enable to Write Pulse Hold	t_{ELWH}	200	–	200	–	300	–	ns

3

TIMING PARAMETER ABBREVIATIONS



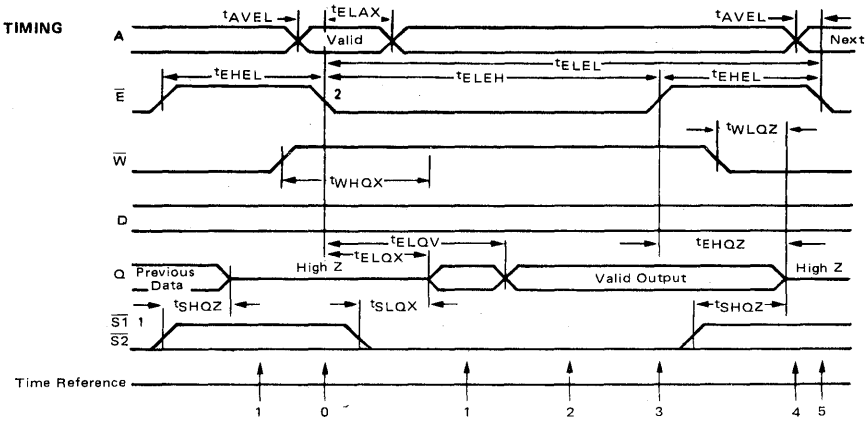
The transition definitions used in this data sheet are:

- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

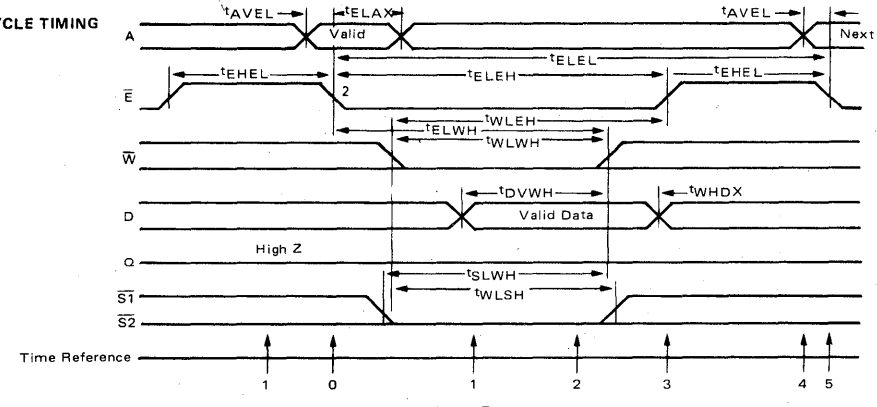
READ CYCLE TIMING



TRUTH TABLE

Time Reference	Inputs					Output	Function
	$\overline{E}$	$\overline{S}$	$\overline{W}$	A	D	Q	
-1	H	H	X	X	X	Z	Disabled
0	↘	X	H	V	X	Z	Address Latched
1	L	L	H	X	X	X	Output Enabled
2	L	L	H	X	X	V	Output Valid
3	↗	L	H	X	X	V	Output Latched
4	H	H	X	X	X	Z	Disabled (Same as -1)
5	↘	X	H	V	X	Z	Next Cycle (Same as 0)

WRITE CYCLE TIMING



TRUTH TABLE

Time Reference	Inputs					Output	Function
	$\overline{E}$	$\overline{S}$	$\overline{W}$	A	D	Q	
-1	H	X	X	X	X	Z	Disabled
0	↘	X	X	V	X	Z	Address Latched
1	L	L	L	X	V	Z	Write Mode
2	L	↗	L	X	V	Z	Data Written
3	↗	X	X	X	X	Z	Write Completed
4	H	X	X	X	X	Z	Disabled (Same as -1)
5	↘	X	X	V	X	Z	Next Cycle (Same as 0)

NOTES:
1. MCM146518 selected only if both $\overline{S1}$ and $\overline{S2}$ are low and deselected if either $\overline{S1}$ or $\overline{S2}$ is high. $\overline{S1}$ and $\overline{S2}$ are connected to $\overline{E}$ on the MCM146508.
2. The address within the memory will change only on falling $\overline{E}$.

MOTOROLA

MCM14524

1024-BIT READ ONLY MEMORY

The MCM14524 is a complementary MOS mask programmable Read Only Memory (ROM). This device is ordered as a factory special with its unique pattern specified by the user.

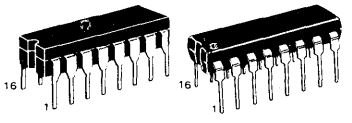
This ROM is organized in a 256 x 4-bit pattern. The contents of a specified address (< A0, A1, A2, A3, A4, A5, A6, A7 >) will appear at the four data outputs (B0, B1, B2, B3) following the negative going edge of the clock. When the clock goes high, the data present at the output will be latched. The memory Enable may be taken low asynchronously, forcing the data outputs low and resetting the output latches. This device finds application wherever low power or high noise immunity is a design consideration.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} typical
- Quiescent Current – 10 nA/package typical @ 5 Vdc
- Single Supply Operation – Either Positive or Negative
- Memory Enable Allows Expansion
- Output Latches Provide a Useful Storage Register
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load to Two HTL Loads Over the Rated Temperature Range

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

1024-BIT
(256 x 4)
READ ONLY MEMORY



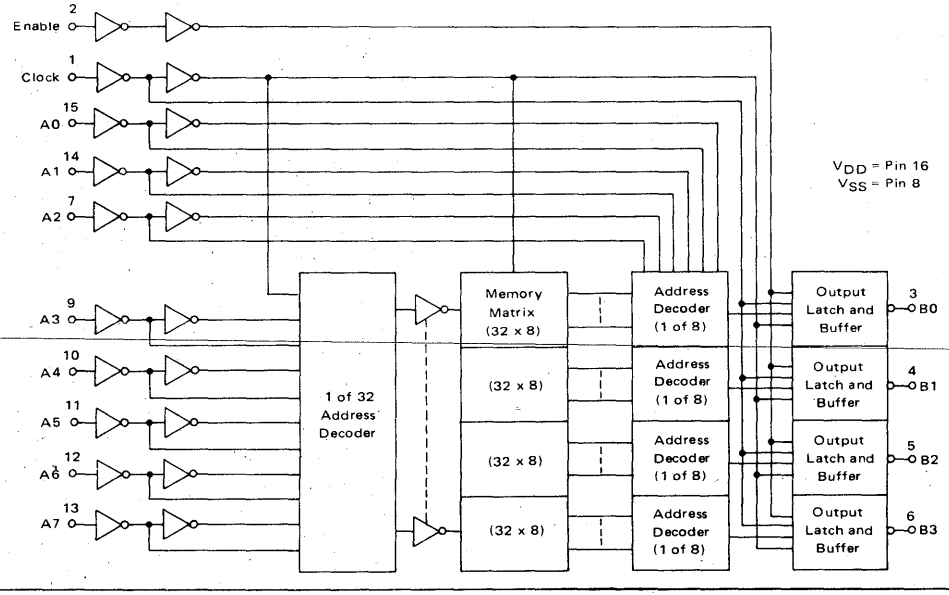
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.01	–	0	0.01	–	0.05	
"1" Level	V_{OH}	5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.99	–	14.99	15	–	14.95	–	
Noise Immunity #	V_{NL}									Vdc
(V_{out} = 0.8 Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
(V_{out} = 1.0 Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
(V_{out} = 1.5 Vdc)		15	3.75	–	3.75	6.75	–	3.75	–	
(V_{out} = 0.8 Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
(V_{out} = 1.0 Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
(V_{out} = 1.5 Vdc)		15	3.65	–	3.75	6.75	–	3.75	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2	–	-1.0	-1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.8	-1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.2	–	-0.16	-0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	-0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	-3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±1.0	–	±0.00001	±1.0	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	μAdc
		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	50	–	0.010	50	–	375	μAdc
		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (1.6\ \mu A/kHz)\ f + I_{DD}$							μAdc
		10	$I_T = (3.2\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (4.8\ \mu A/kHz)\ f + I_{DD}$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$$

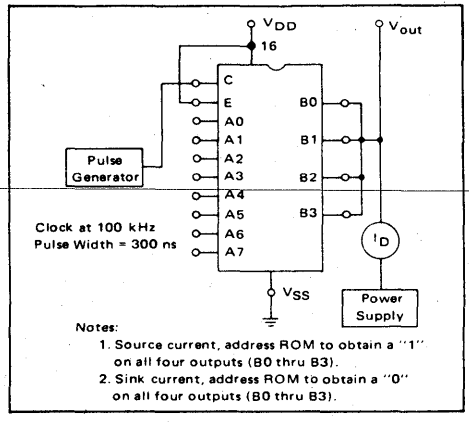
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH}, t_{THL} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH}, t_{THL} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Clock Read Access Delay Time	t_{acc_C}					ns
t_{acc_C} = (1.7 ns/pF) C_L + 1265 ns		5.0	–	1350	4000	
t_{acc_C} = (0.66 ns/pF) C_L + 517 ns		10	–	550	1600	
t_{acc_C} = (0.5 ns/pF) C_L + 325 ns		15	–	350	1200	
Enable Access Delay Time	$t_{acc_{En}}$					ns
$t_{acc_{En}}$ = (1.7 ns/pF) C_L + 160 ns		5.0	–	245	615	
$t_{acc_{En}}$ = (0.66 ns/pF) C_L + 77 ns		10	–	110	265	
$t_{acc_{En}}$ = (0.5 ns/pF) C_L + 50 ns		15	–	75	190	
Clock Pulse Width*	t_{WH}	5.0	450	150	–	ns
		10	165	55	–	
		15	125	35	–	
	t_{WL}	5.0	3600	1200	–	ns
		10	1425	475	–	
		15	1070	300	–	
Maximum Low Clock Pulse Width #	t_{WL}	5.0	2.0	10	–	ms
		10	0.9	3.0	–	
		15	0.1	0.3	–	
Address Setup-Time	$t_{su(A)}$	5.0	0	0	–	ns
		10	0	0	–	
		15	0	0	–	
Address Hold Time	$t_{h(A)}$	5.0	0	0	–	ns
		10	0	0	–	
		15	0	0	–	
Clock to Enable Setup Time	$t_{su(cl)}$	5.0	4275	1425	–	ns
		10	1725	575	–	
		15	1295	400	–	
Clock to Enable Hold Time	$t_{h(cl)}$	5.0	150	0	–	ns
		10	75	0	–	
		15	55	0	–	

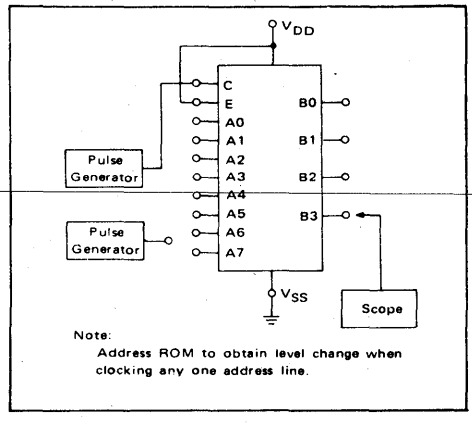
*The clock can remain high indefinitely with the data remaining latched.
#If clock stays low too long, the dynamically stored data will leak off and will have to be recalled.

FIGURE 1 – OUTPUT DRIVE CURRENT TEST CIRCUIT



Notes:
1. Source current, address ROM to obtain a "1" on all four outputs (B0 thru B3).
2. Sink current, address ROM to obtain a "0" on all four outputs (B0 thru B3).

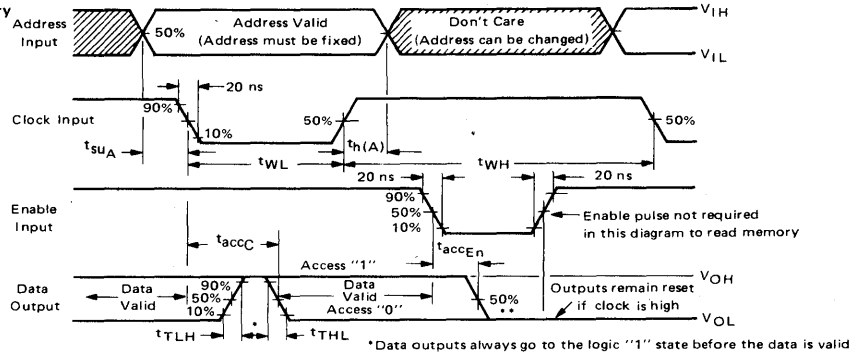
FIGURE 2 – SWITCHING TIME TEST CIRCUIT (Refer to timing diagram)



Note:
Address ROM to obtain level change when clocking any one address line.

MEMORY READ CYCLE TIMING DIAGRAMS

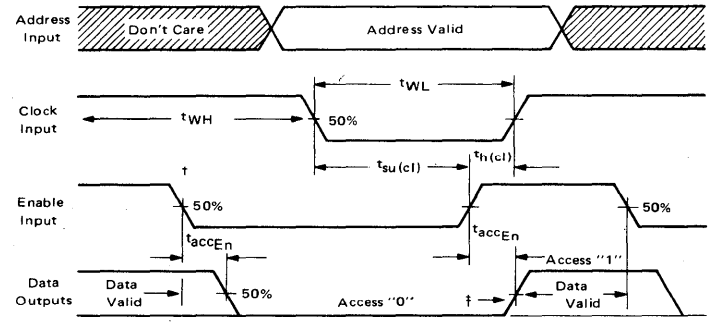
a) Using Clock to Read Memory



*Data outputs always go to the logic "1" state before the data is valid between accessing successive "0's"

**Outputs forced to "0" by Enable.

b) Using the Enable to Read Memory



† In this mode of operation, the negative going edge of Enable should occur on or before the clock negative edge.

‡The data outputs are valid without the logic "1" pulse occurring during the access cycle as shown in a) above.

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM14524, the customer may specify the content of the memory.

Address Inputs:

Words are numbered 0 through 255 and are addressed using sequential addressing of Address leads A0 through A7 with A0 as the least significant digit.

Logic "0" is defined as a "low" Address input (V_{IL}).
Logic "1" is defined as a "high" Address input (V_{IH}).

WORD \ ADDRESS	A7	A6	A5	A4	A3	A2	A1	A0
Word 0	0	0	0	0	0	0	0	0
Word 1	0	0	0	0	0	0	0	1
Word 2	0	0	0	0	0	0	1	0
Word 3	0	0	0	0	0	0	1	1
. .	.	.	.	.	.	.	.	.
. .	.	.	.	.	.	.	.	.
. .	.	.	.	.	.	.	.	.
Word 255	1	1	1	1	1	1	1	1

TRUTH TABLE

CLOCK	ENABLE	B0	B1	B2	B3
V_{DD} ⎍ V_{SS}	1	⟨Address⟩*	⟨Address⟩*	⟨Address⟩*	⟨Address⟩*
V_{SS} ⎍ V_{DD}	1	OUTPUT DATA LATCHES			
X	0	0	0	0	0

X = Don't Care

*Indicates contents of specified Address will appear at outputs as stated above.

BINARY TO HEXADECIMAL CONVERSION TABLE

BINARY WORD DESIRED	CARD CHARACTER
0 0 0 0	0
0 0 0 1	1
0 0 1 0	2
0 0 1 1	3
0 1 0 0	4
0 1 0 1	5
0 1 1 0	6
0 1 1 1	7
1 0 0 0	8
1 0 0 1	9
1 0 1 0	A
1 0 1 1	B
1 1 0 0	C
1 1 0 1	D
1 1 1 0	E
1 1 1 1	F

Two methods may be used to transmit the custom memory pattern to Motorola.

METHOD A: PUNCHED COMPUTER CARDS

A binary coded decimal equivalent of each desired output may be punched in standard computer cards (four cards are required for all 256 words) in numerical (word number) order. 64 words per card are punched in columns 12 thru 75 using the Binary to Hexadecimal conversion table. Columns 77 and 78 are used to number the cards, which must be in numerical order. Please use characters as shown in the table when punching computer cards.

ROM SAMPLE WORD PROGRAMMING FOR PUNCHED CARD

WORD NUMBER	ADDRESS INPUTS								SAMPLE WORD OUTPUTS				CARD CHARACTER
	A7	A6	A5	A4	A3	A2	A1	A0	B3	B2	B1	B0	
0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1	0	0	1	1	3
2	0	0	0	0	0	0	1	0	0	0	1	1	3
3	0	0	0	0	0	0	1	1	0	0	0	0	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.
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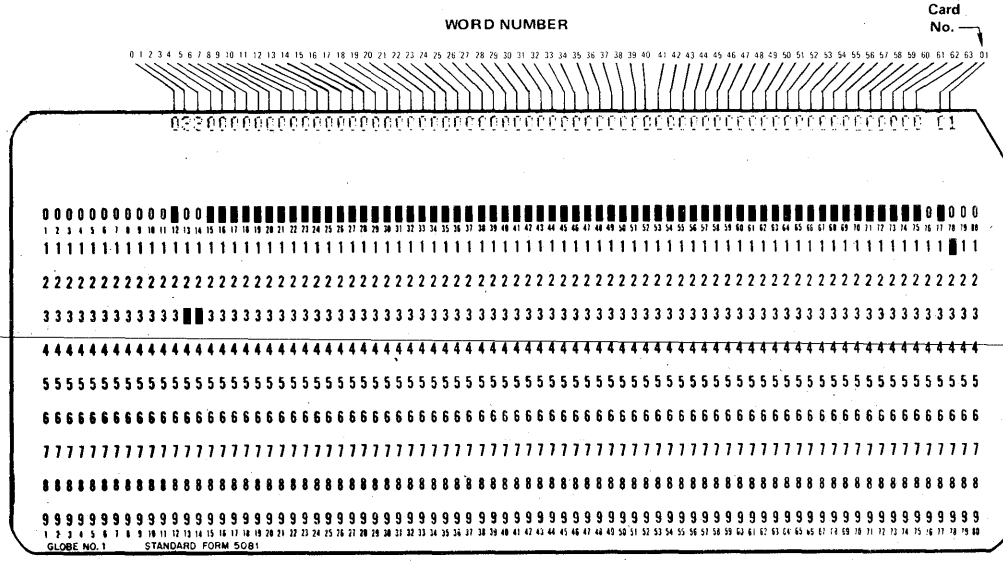
255	1	1	1	1	1	1	1	1	1	0	1	0	A

Shown in columns 12 – 15 on card below



METHOD B: TRUTH TABLE

For customers who do not have access to punch cards, Motorola will accept Truth Tables. When filling out the table, use the 0 to F hexidecimal character in column "C".

CUSTOM PROGRAM for the MCM14524 Read Only Memory

WORD	C
0	
1	
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43	
44	
45	
46	
47	
48	
49	
50	

WORD	C
51	
52	
53	
54	
55	
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100	
101	

WORD	C
102	
103	
104	
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WORD	C
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WORD	C
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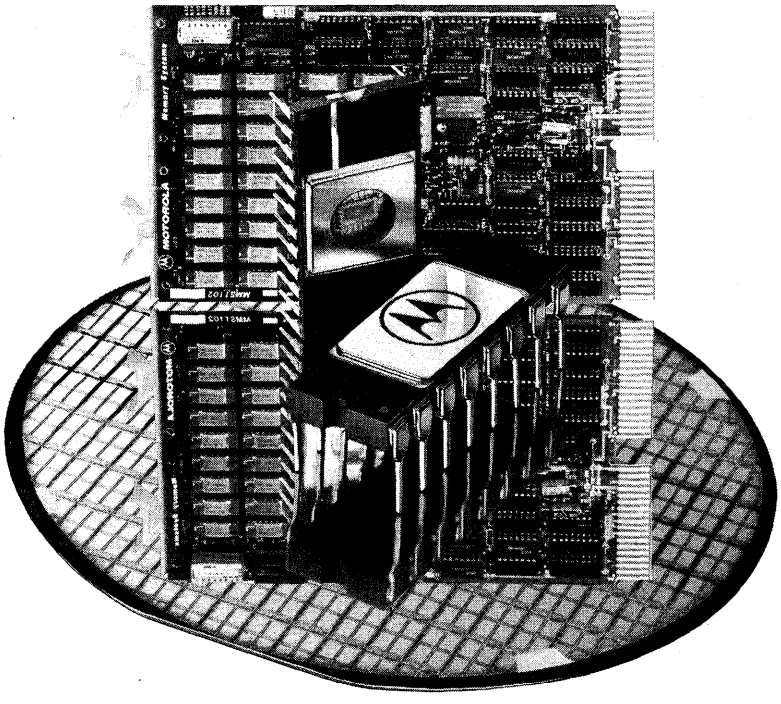
255	



Bipolar Memories
TTL, MECL-RAM, PROM

4

4

MOTOROLA

MCM93415

1024-BIT RANDOM ACCESS MEMORY

The MCM93415 is a 1024-bit Read/Write RAM organized 1024 words by 1 bit.

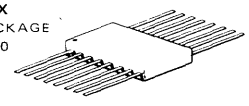
The MCM93415 is designed for buffer control storage and high performance main memory applications, and has a typical access time of 35 ns.

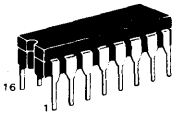
The MCM93415 has full decoding on-chip, separate data input and data output lines, and an active low chip select. The device is fully compatible with standard DTL and TTL logic families and features an uncommitted collector output for ease of memory expansion.

- Uncommitted Collector Output
- TTL Inputs and Output
- Non-Inverting Data Output
- High Speed –
  Access Time – 35 ns Typical
  Chip Select – 15 ns Typical
- Power Dissipation Decreases with Increasing Temperature
- Power Dissipation 0.5 mW/Bit Typical
- Organized 1024 Words X 1 Bit

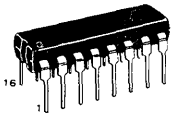
TTL
1024 X 1 BIT
RANDOM ACCESS MEMORY

F SUFFIX
CERAMIC PACKAGE
CASE 650



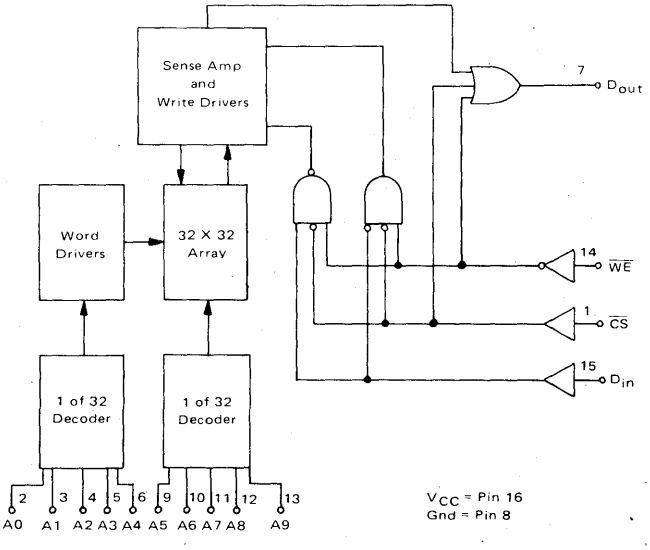


D SUFFIX
CERAMIC PACKAGE
CASE 620



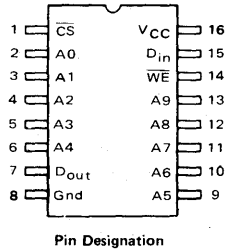
P SUFFIX
PLASTIC PACKAGE
CASE 648

BLOCK DIAGRAM



VCC = Pin 16
Gnd = Pin 8

PIN ASSIGNMENT



Pin Designation

$\overline{CS}$	Chip Select
A0 – A9	Address Inputs
$\overline{WE}$	Write Enable
D_{in}	Data Input
D_{out}	Data Output

4

FUNCTIONAL DESCRIPTION

The MCM93415 is a fully decoded 1024-bit Random Access Memory organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, A0 to A9.

The Chip Select input provides for memory array expansion. For large memories, the fast chip select access time permits the decoding of Chip Select ($\overline{CS}$) from the address without affecting system performance.

The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$, Pin 14). With $\overline{WE}$ held low and the chip selected, the data at D_{in} is written into the addressed location. To read, $\overline{WE}$ is held high and the chip selected. Data in the specified location is presented at D_{out} and is non-inverted.

Uncommitted collector outputs are provided to allow wired-OR applications. In any application an external pull-up resistor of R_L value must be used to provide a high at the output when it is off. Any R_L value within the range specified below may be used.

$$\frac{V_{CC}(Min)}{I_{OL} - FO(1.6)} \leq R_L \leq \frac{V_{CC}(Min) - V_{OH}}{n(I_{CEX}) + FO(0.04)}$$

R_L is in kΩ
n = number of wired-OR outputs tied together
FO = number of TTL Unit Loads (UL) driven
I_{CEX} = Memory Output Leakage Current
V_{OH} = Required Output High Level at Output Node
I_{OL} = Output Low Current

The minimum R_L value is limited by output current sinking ability. The maximum R_L value is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}. One Unit Load = 40 μA High/1.6 mA Low.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature	
Ceramic Package (D and F Suffix)	-55°C to +165°C
Plastic Package (P Suffix)	-55°C to +125°C
Operating Junction Temperature, T_J	
Ceramic Package (D and F Suffix)	< 165°C
Plastic Package (P Suffix)	< 125°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
Input Voltage (dc)	-0.5 V to +5.5 V
Voltage Applied to Outputs (Output High)	-0.5 V to +5.5 V
Output Current (dc) (Output Low)	+20 mA
Input Current (dc)	-12 mA to +5.0 mA

TRUTH TABLE

Inputs			Output	
$\overline{CS}$	$\overline{WE}$	D_{in}	Open Collector	Mode
H	X	X	H	Not Selected
L	L	L	H	Write "0"
L	L	H	H	Write "1"
L	H	X	D_{out}	Read

H = High Voltage Level
L = Low Voltage Level
X = Don't Care (High or Low)

NOTE 1: Device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

4

GUARANTEED OPERATING RANGES (Note 2)

Part Number	Supply Voltage (V_{CC}) Min	Nom	Max	Ambient Temperature (T_A)
MCM93415DC, PC	4.75 V	5.0 V	5.25 V	0°C to +75°C
MCM93415FM, DM	4.50 V	5.0 V	5.50 V	-55°C to +125°C

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

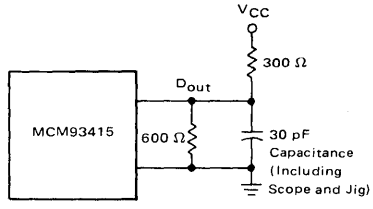
Symbol	Characteristic	Limits Min	Max	Unit	Conditions	
V_{OL}	Output Low Voltage		0.45	Vdc	V_{CC} = Min, I_{OL} = 16 mA	
V_{IH}	Input High Voltage	2.1		Vdc	Guaranteed Input High Voltage for All Inputs	
V_{IL}	Input Low Voltage		0.8	Vdc	Guaranteed Input Low Voltage for All Inputs	
I_{IL}	Input Low Current		-400	μAdc	V_{CC} = Max, V_{in} = 0.4 V	
I_{IH}	Input High Current		40	μAdc	V_{CC} = Max, V_{in} = 4.5 V	
			1.0	mAdc	V_{CC} = Max, V_{in} = 5.25 V	
I_{CEX}	Output Leakage Current		100	μAdc	V_{CC} = Max, V_{out} = 4.5 V	
V_{CD}	Input Diode Clamp Voltage		-1.5	Vdc	V_{CC} = Max, I_{in} = -10 mA	
I_{CC}	Power Supply Current		130	mAdc	T_A = Max	V_{CC} = Max, All Inputs Grounded
			155	mAdc	T_A = 0°C	
			170	mAdc	T_A = Min	

AC OPERATING CONDITIONS AND CHARACTERISTICS

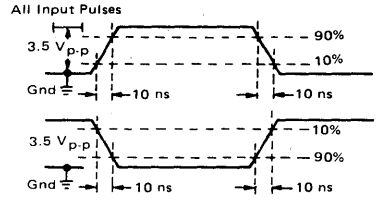
(Full operating voltage and temperature unless otherwise noted)

AC TEST LOAD AND WAVEFORM

Loading Condition



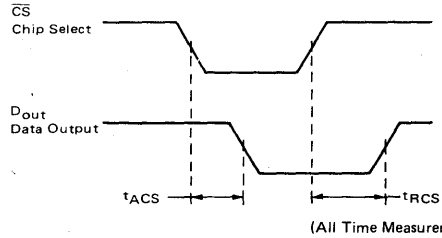
Input Pulses



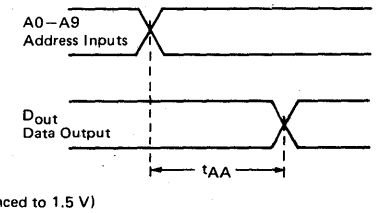
Symbol	Characteristic (Notes 2, 3)	MCM93415DC, PC Min	MCM93415DC, PC Max	MCM93415DM, FM Min	MCM93415DM, FM Max	Unit	Conditions
READ MODE	DELAY TIMES					ns	
t_{ACS}	Chip Select Time		35		45		See Test Circuit
t_{RCS}	Chip Select Recovery Time		35		50		and Waveforms
t_{AA}	Address Access Time		45		60		
WRITE MODE	DELAY TIMES					ns	
t_{WS}	Write Disable Time		35		45		See Test Circuit
t_{WR}	Write Recovery Time		40		50		and Waveforms
	INPUT TIMING REQUIREMENTS					ns	
t_W	Write Pulse Width (to guarantee write)	30		40			See Test Circuit
t_{WSD}	Data Setup Time Prior to Write	5		5			and Waveforms
t_{WHD}	Data Hold Time After Write	5		5			
t_{WSA}	Address Setup Time (at t_W = Min)	10		15			
t_{WHA}	Address Hold Time	10		10			
t_{WSCS}	Chip Select Setup Time	5		5			
t_{WHCS}	Chip Select Hold Time	5		5			

READ OPERATION TIMING DIAGRAM

Propagation Delay from Chip Select

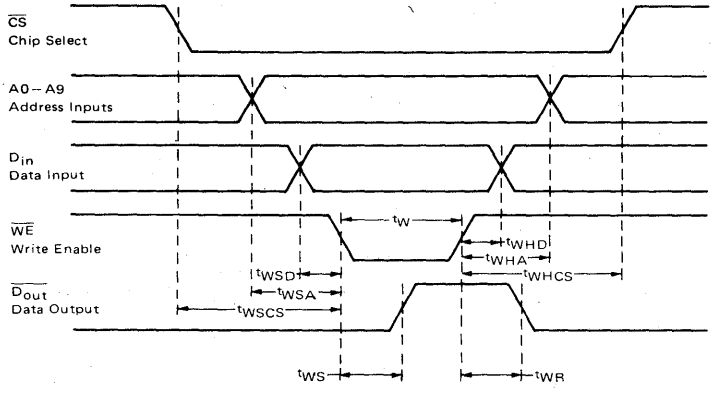


Propagation Delay from Address Inputs



(All Time Measurements Referenced to 1.5 V)

WRITE CYCLE TIMING



(All Time Measurements Referenced to 1.5 V)

4

NOTE 2: DC and AC specifications limits guaranteed with 500 linear feet per minute blown air. Contact your Motorola Sales Representative if extended temperature or modified operating conditions are desired.

Package	θ_{JA} (Junction to Ambient)		θ_{JC} (Junction to Case)
	Blown	Still	
D Suffix	50°C/W	85°C/W	15°C/W
F Suffix	55°C/W	90°C/W	15°C/W
P Suffix	65°C/W	100°C/W	25°C/W

NOTE 3: The AC limits are guaranteed to be the worst case bit in the memory.

MOTOROLA

MCM93425

1024-BIT RANDOM ACCESS MEMORY

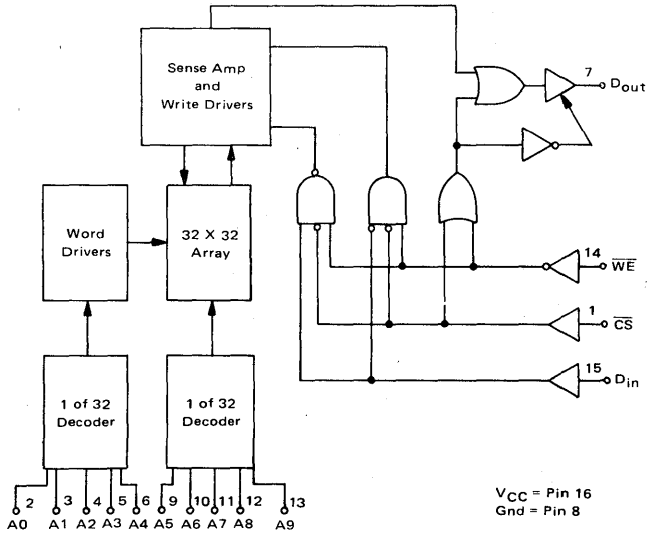
The MCM93425 is a 1024-bit Read/Write RAM, organized 1024 words by 1 bit.

The MCM93425 is designed for high performance main memory and control storage applications and has a typical address time of 35 ns.

The MCM93425 has full decoding on-chip, separate data input and data output lines, and an active low-chip select and write enable. The device is fully compatible with standard DTL and TTL logic families. A three-state output is provided to drive bus-organized systems and/or highly capacitive loads.

- Three-State Output
- TTL Inputs and Output
- Non-Inverting Data Output
- High Speed –
  - Access Time – 35 ns Typical
  - Chip Select – 15 ns Typical
- Power Dissipation – 0.5 mW/Bit Typical
- Power Dissipation Decreases With Increasing Temperature

BLOCK DIAGRAM

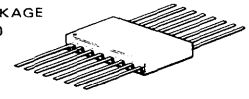


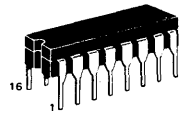
V_{CC} = Pin 16
Gnd = Pin 8

NOTE: Logic driving sense amp/write drivers depicts negative-only write used on C4m.

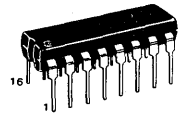
TTL
1024 X 1 BIT
RANDOM ACCESS MEMORY

F SUFFIX
CERAMIC PACKAGE
CASE 650



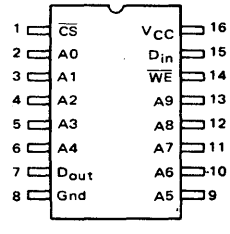


D SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



Pin Description

$\overline{CS}$	Chip Select
A0–A9	Address Inputs
$\overline{WE}$	Write Enable
D_{in}	Data Input
D_{out}	Data Output

4

FUNCTIONAL DESCRIPTION

The MCM93425 is a fully decoded 1024-bit Random Access Memory organized 1024 words by one bit. Word selection is achieved by means of a 10-bit address, A0–A9.

The Chip Select ($\overline{CS}$) input provides for memory array expansion. For large memories, the fast chip select time permits the decoding of chip select from the address without increasing address access time.

The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$, Pin 14). With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{in} is written into the addressed location. To read, $\overline{WE}$ is held high and $\overline{CS}$ held low. Data in the specified location is presented at D_{out} and is non-inverted.

The three-state output provides drive capability for higher speeds with capacitive load systems. The third state (high impedance) allows bus organized systems where multiple outputs are connected to a common bus.

During writing, the output is held in the high-impedance state.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature	
Ceramic Package (D and F Suffix)	−55°C to +165°C
Plastic Package (P Suffix)	−55°C to +125°C
Operating Junction Temperature, T_J	
Ceramic Package (D and F Suffix)	<165°C
Plastic Package (P Suffix)	<125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Input Voltage (dc)	−0.5 V to +5.5 V
Voltage Applied to Outputs (Output High)	−0.5 V to +5.5 V
Output Current (dc) (Output Low)	+20 mA
Input Current (dc)	−12 mA to +5.0 mA

TRUTH TABLE

Inputs			Output	
$\overline{CS}$	$\overline{WE}$	D_{in}	D_{out}	Mode
H	X	X	High Z	Not Selected
L	L	L	High Z	Write "0"
L	L	H	High Z	Write "1"
L	H	X	D_{out}	Read

H = High Voltage Level
L = Low Voltage Level
X = Don't Care (High or Low)

NOTE 1: Device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

GUARANTEED OPERATING RANGES (Notes 2 and 3)

Part Number	Supply Voltage (V_{CC})			Ambient Temperature (T_A)
	Min	Nom	Max	
MCM93425DC, PC	4.75 V	5.0 V	5.25 V	0°C to +75°C
MCM93425FM, DM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

4

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

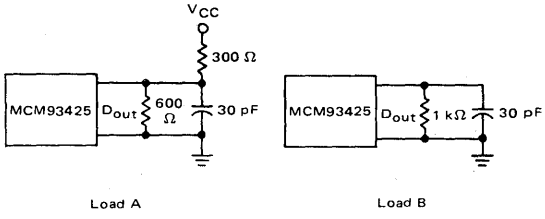
Symbol	Characteristic		Limits Min	Limits Max	Units	Conditions	
V_{OL}	Output Low Voltage			0.45	Vdc	V_{CC} = Min, I_{OL} = 16 mA	
V_{IH}	Input High Voltage		2.1		Vdc	Guaranteed Input High Voltage for all Inputs	
V_{IL}	Input Low Voltage			0.8	Vdc	Guaranteed Input Low Voltage for all Inputs	
I_{IL}	Input Low Current			−400	μAdc	V_{CC} = Max, V_{in} = 0.4 V	
I_{IH}	Input High Current			40	μAdc	V_{CC} = Max, V_{in} = 4.5 V	
				1.0	mAdc	V_{CC} = Max, V_{in} = 5.25 V	
I_{off}	Output Current (High Z)			50	μAdc	V_{CC} = Max, V_{out} = 2.4 V	
				−50		V_{CC} = Max, V_{out} = 0.5 V	
I_{OS}	Output Current Short Circuit to Ground			−100	mAdc	V_{CC} = Max	
V_{OH}	Output High Voltage	MCM93425DC, PC	2.4		Vdc	I_{OH} = −10.3 mA, V_{CC} = 5.0 V ±5%	
		MCM93425FM, DM	2.4		Vdc	I_{OH} = −5.2 mA	
V_{CD}	Input Diode Clamp Voltage			−1.5	Vdc	V_{CC} = Max, I_{in} = −10 mA	
I_{CC}	Power Supply Current			130	mAdc	T_A = Max	V_{CC} = Max, All Inputs Grounded
				155	mAdc	T_A = 0°C	
				170	mAdc	T_A = Min	

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted)

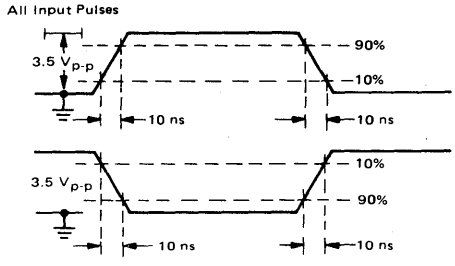
AC TEST LOAD AND WAVEFORMS

Loading Conditions



Load A Load B

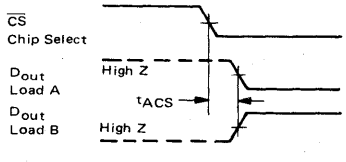
Input Pulses



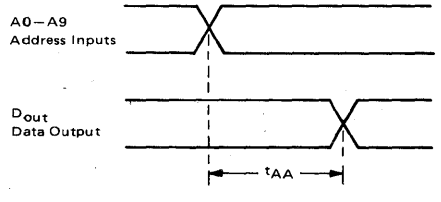
Symbol	Characteristic (Notes 2, 4)	MCM93425DC, PC Min	MCM93425DC, PC Max	MCM93425DM, FM Min	MCM93425DM, FM Max	Units	Conditions
READ MODE	DELAY TIMES					ns	
t_{ACS}	Chip Select Time		35		45		See Test Circuit
t_{ZRCS}	Chip Select to High Z		35		50		and Waveforms
t_{AA}	Address Access Time		45		60		
WRITE MODE	DELAY TIMES					ns	
t_{ZWS}	Write Disable to High Z		35		45		See Test Circuit
t_{WR}	Write Recovery Time		40		50		and Waveforms
	INPUT TIMING REQUIREMENTS					ns	
t_W	Write Pulse Width (to guarantee write)	30		40			See Test Circuit
t_{WSD}	Data Setup Time Prior to Write	5		5			and Waveforms
t_{WHD}	Data Hold Time After Write	5		5			
t_{WSA}	Address Setup Time (at t_W = Min)	10		15			
t_{WHA}	Address Hold Time	10		10			
t_{WSCS}	Chip Select Setup Time	5		5			
t_{WHCS}	Chip Select Hold Time	5		5			

READ OPERATION TIMING DIAGRAM

Propagation Delay from Chip Select

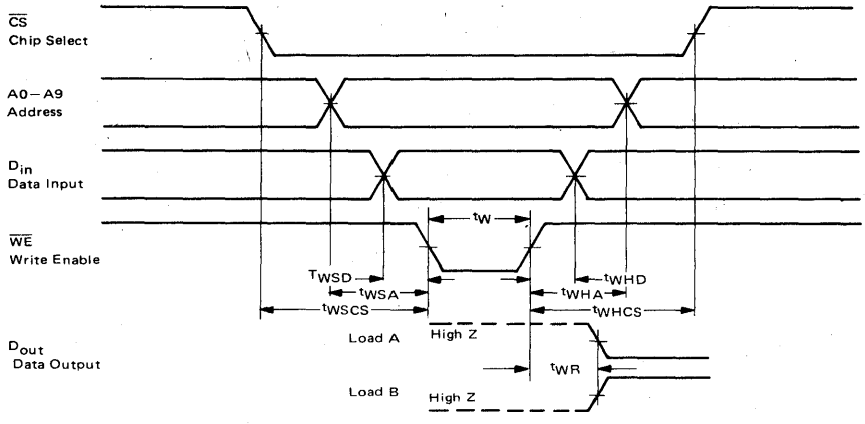


Propagation Delay from Address Inut



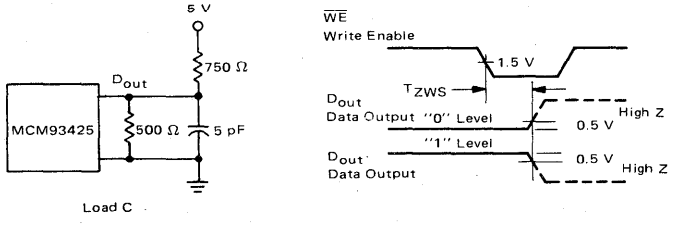
(All time measurements referenced to 1.5 V)

WRITE CYCLE TIMING

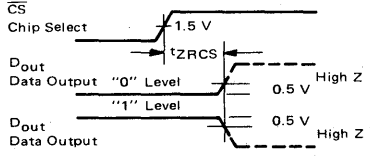


(All above measurements reference to 1.5 V)

WRITE ENABLE TO HIGH Z DELAY



Propagation Delay from Chip Select to High Z



(All t_{ZXXX} parameters are measured at a delta of 0.5 V from the logic level and using Load C)

NOTE 2: DC and AC specifications limits guaranteed with 500 linear feet per minute blown air. Contact your Motorola Sales Representative if extended temperature or modified operating conditions are desired.

Package	θ_{JA} (Junction to Ambient)		θ_{JC} (Junction to Case)
	Blown	Still	
D Suffix	50°C/W	85°C/W	15°C/W
F Suffix	55°C/W	90°C/W	15°C/W
P Suffix	65°C/W	100°C/W	25°C/W

NOTE 3: Output short circuit conditions must not exceed 1 second duration.
NOTE 4: The maximum address access time is guaranteed to be the worst case bit in the memory.

MOTOROLA

MCM5303
MCM5003
MCM5304
MCM5004

MTTL

512-BIT PROGRAMMABLE READ ONLY MEMORY

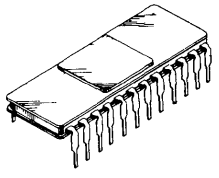
512-BIT PROGRAMMABLE READ ONLY MEMORY

The MCM5303/5003 and MCM5304/5004 are monolithic bipolar 512-bit Programmable Read Only Memories (PROMs) organized as 64 eight-bit words. These memories are field programmable, i.e., the user can custom program these memories himself. Metal interconnections establish each bit initially in the logic "0" state. By "blowing" appropriate nichrome resistors and thus breaking metalization links these bits can be changed to the logic "1" state to meet specific program requirements. Detailed programming instructions are contained in this data sheet.

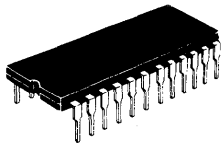
The MCM5303/5003 and MCM5304/5004 have six address inputs to select the proper word and two chip enable inputs, as well as outputs for each of the eight bits.

The MCM5303 and MCM5304 are specified over an operating temperature range of -55°C to +125°C. The MCM5003 and MCM5004 are specified over an operating temperature range of 0°C to +70°C.

The MCM5303 and MCM5003 have positive enables with open collector outputs. The MCM5304 and MCM5004 have positive enables with 2.0 kilohm pullup resistors on the collector outputs.



AL SUFFIX
CASE 684
CERAMIC PACKAGE



L SUFFIX
CERAMIC PACKAGE
CASE 623

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	Vdc
Input Voltage	V_{in}	-1.0 to +5.5	Vdc
Output Voltage (Open collectors)	V_{OH}	-0.5 to +7.0	Vdc
Thermal Resistance	θ_{JA}	100	°C/W
Operating Temperature Range MCM5303, MCM5304 MCM5003, MCM5004	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +165	°C

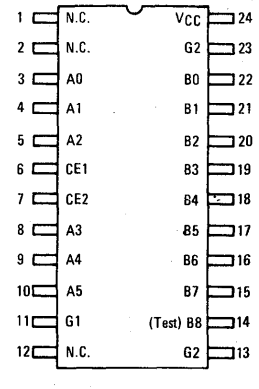
FEATURES:

- Positive Logic for Both Inputs and Outputs
  Logic "0" = Output Device ON (V_{OL})
  Logic "1" = Output Device OFF (V_{OH})
- Logic Levels Compatible with MDTL and All MTTL Families
- Ninth Bit Available for Circuit Test
- Access Time < 75 ns
- Outputs Sink 12 mA Open Collector, 10 mA with Pullup Resistors
- Field Programmable by Blowing Nichrome Links
- Hermetic Package

APPLICATIONS:

- Look Up Tables
- Micro Programs
- Decode Functions
- Code Conversion
- Number Conversion
- Random Logic
- Character Generation

PIN ASSIGNMENT



4

DC ELECTRICAL CHARACTERISTICS (T_A = -55°C to +125°C for MCM5303 and MCM5304, 0°C to +70°C for MCM5003 and MCM5004 unless otherwise noted)

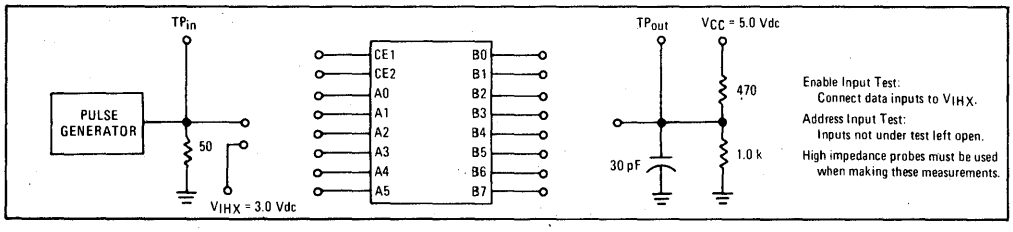
Characteristic		Symbol	Min	Max	Unit
Input Forward Current (V_{IL} = 0.4 Vdc, V_{CC} = 5.25 Vdc)		I_{IL}	–	1.6	mAdc
Input Leakage Current (V_{IH} = V_{CC} = 5.25 Vdc)		I_{IH}	–	100	μAdc
Logic "0" Output Voltage*		V_{OL}			Vdc
(T_A = 0°C to +125°C for MCM5303 and MCM5304, 0°C to +70°C for MCM5003 and MCM5004)					
(I_{OL} = 12 mAdc, V_{CC} = 4.75 Vdc)	Open Collectors		–	0.45	
(I_{OL} = 10 mAdc, V_{CC} = 4.75 Vdc)	Pullup Resistors		–	0.45	
(T_A = -55°C for MCM5303 and MCM5304)					
(I_{OL} = 12 mAdc, V_{CC} = 4.75 Vdc)	Open Collectors		–	0.50	
(I_{OL} = 10 mAdc, V_{CC} = 4.75 Vdc)	Pullup Resistors		–	0.50	
Logic "1" Output Voltage (I_{OH} = −0.5 mAdc, V_{CC} = 4.75 Vdc)	Pullup Resistors	V_{OH}	2.5	–	Vdc
Output Leakage Current (V_{CC} = V_{CEX} = 5.25 Vdc)	Open Collectors	I_{CEX}	–	200	μAdc
Power Supply Drain Current		I_{CC}			mAdc
(Enable and all other inputs	Open Collectors		–	95	
grounded, V_{CC} = 5.0 Vdc)	Pullup Resistors		–	120	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, T_A = 25°C)

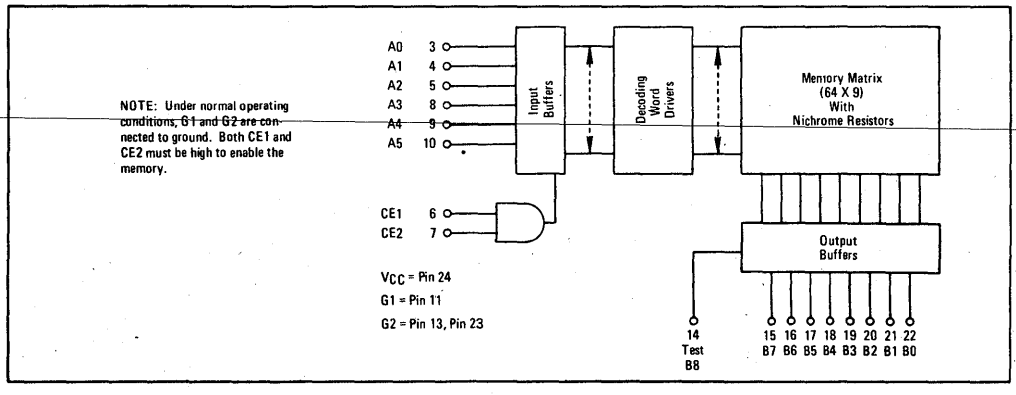
Access Times* (30pF Load)				ns
Address to Output	t_{AO}	25	120	
Enable to Output	t_{EO}	25	120	

*Pin 13 is schematically connected to G2. For optimum propagation delay and V_{OL} characteristics, externally tie Pin 13 to Pin 23 (G2).

SWITCHING TIME TEST CIRCUIT



BLOCK DIAGRAM



PROGRAMMING THE MCM5303/5003 AND MCM5304/5004

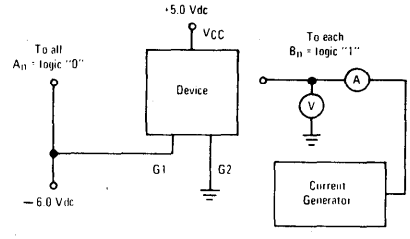
The table and diagram below give instructions for field programming the MCM5303/5003 and MCM5304/5004. All data given is for ambient temperatures of 25°C. If necessary, further programming aid can be obtained from Motorola engineering and product marketing personnel by contacting your nearest Motorola sales office.

Programming Voltage Limits

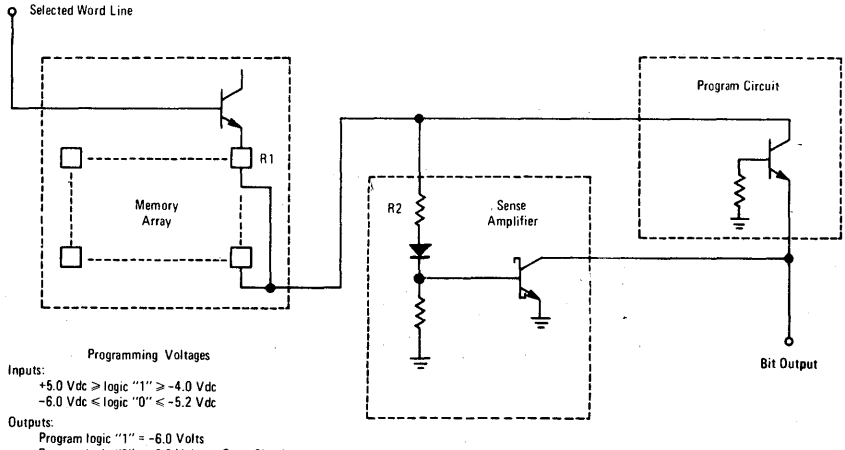
	Symbol	Value	Unit
Address and Chip Enable Voltages	V_{IH} V_{IL}	−4.0 to +5.0 −6.0 to −5.2	Vdc
Power Supply Voltage	V_{CC}	+5.0 ±5%	Vdc
G1 Voltage	V_{G1}	-6.0 ±5%	Vdc
G2 Voltage	V_{G2}	0.0	Vdc
Program Voltage at Desired Bit Output	V_{BP}	-6.0 ±5%	Vdc

Programming Procedure

1. Select the address code desired. Connect low (logic "0") inputs to −6.0 Vdc nominal. Leave high (logic "1") inputs unconnected.
2. With the output voltage of a 120-mA current generator clamped to −6.0 Vdc, apply a negative-going current pulse of 800 ms duration to any output to be programmed as a logic "1".
3. Repeat step 2 for each output to be programmed as a logic "1", one bit at a time.
4. Select next address code desired and repeat steps 2 and 3.



Link Programming Diagram



TRUTH TABLE FORMAT

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
WORD 0								
WORD 1								
WORD 2								
WORD 3								
WORD 4								
WORD 5								
WORD 6								
WORD 7								
WORD 8								
WORD 9								
WORD 10								
WORD 11								
WORD 12								
WORD 13								
WORD 14								
WORD 15								
WORD 16								
WORD 17								
WORD 18								
WORD 19								
WORD 20								
WORD 21								
WORD 22								
WORD 23								
WORD 24								
WORD 25								
WORD 26								
WORD 27								
WORD 28								
WORD 29								
WORD 30								
WORD 31								

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
WORD 32								
WORD 33								
WORD 34								
WORD 35								
WORD 36								
WORD 37								
WORD 38								
WORD 39								
WORD 40								
WORD 41								
WORD 42								
WORD 43								
WORD 44								
WORD 45								
WORD 46								
WORD 47								
WORD 48								
WORD 49								
WORD 50								
WORD 51								
WORD 52								
WORD 53								
WORD 54								
WORD 55								
WORD 56								
WORD 57								
WORD 58								
WORD 59								
WORD 60								
WORD 61								
WORD 62								
WORD 63								

WHY THE NINTH BIT?

The ninth bit was designed into the MCM5303/MCM5003 and the MCM5304/MCM5004 because field-programmable ROMs present testing problems not encountered with conventional mask-programmable ROMs.

Three areas of testing are affected: Program Element Testing, Functional Testing, and AC Testing. The ninth bit helps to solve the problem of Program Element Testing by assuring that links can be blown without destroying any of the normal 64x8 bit array.

Functional and ac performance are assured by verifying that changes do occur at the outputs as the addresses change. This is important in that all of the outputs are in a logic "0" state regardless of the address selected, and no way is available to determine whether the functions are correctly operating without the ninth testing bit.

MOTOROLA

MCM7620
MCM7621

MTTL

2048-BIT PROGRAMMABLE READ ONLY MEMORIES

MCM7620 – 512 X 4 – Open-Collector
MCM7621 – 512 X 4 – Three-State

2048-BIT PROGRAMMABLE READ ONLY MEMORY

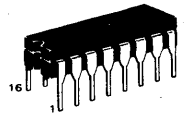
The MCM7620/MCM7621 have common dc electrical characteristics and identical programming requirements. They are fully decoded, high-speed, field-programmable ROMs and are available with open-collector or three-state outputs. All bits are manufactured storing a logical "1" (outputs high), and can be selectively programmed for logical "0" (outputs low).

The field-programmable PROM can be custom programmed to any pattern using a simple programming procedure. Schottky bipolar circuitry provides fast access time, and features temperature and voltage compensation to minimize access time variations.

All pinouts are compatible to industry-standard PROMs and ROMs.

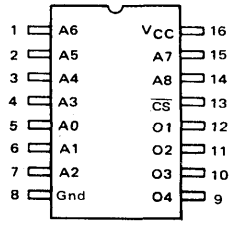
In addition to the conventional storage array, extra test rows and columns are included to assure high programmability, and guarantee parametric and ac performance. Fuses in these test rows and columns are blown prior to shipment.

- Common dc Electrical Characteristics and Programming Procedure
- Simple, High-Speed Programming Procedure (0.1 Second per 1024 Bits, Typical)
- Expandable – Open-Collector or Three-State Outputs and Chip Enable Inputs
- Inputs and Outputs TTL-Compatible
  Low Input Current – 250 μA Logic "0", 40 μA Logic "1"
  Full Output Drive – 16 mA Sink, 2.0 mA Source
- Fast Access Time – Guaranteed for Worst-Case N^2 Sequencing, Over Commercial and Military Temperature and Voltage Ranges
- Pin-Compatible with Industry-Standard PROMs and ROMs



CERAMIC PACKAGE
CASE 620

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage (operating)	V_{CC}	+7.0	Vdc
Input Voltage	V_{in}	+5.5	Vdc
Output Voltage (operating)	V_{OH}	+7.0	Vdc
Supply Current	I_{CC}	650	mAdc
Input Current	I_{in}	-20	mAdc
Output Sink Current	I_o	100	mAdc
Operating Temperature Range MCM76xxDM MCM76xxDC	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Maximum Junction Temperature	T_J	+175	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. (While programming, follow the programming specifications.)

4

DC OPERATING CONDITIONS AND CHARACTERISTICS

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}				Vdc
MCM76xxDM		4.50	5.0	5.50	
MCM76xxDC		4.75	5.0	5.25	
Input High Voltage	V_{IH}	2.0	–	–	Vdc
Input Low Voltage	V_{IL}	–	–	0.8	Vdc

DC CHARACTERISTICS

			Open-Collector Output			Three-State Output			
Symbol	Parameter	Test Conditions	Min	Typ	Max	Min	Typ	Max	Unit
I_{RA}, I_{RE}	Address/Enable "1"	V_{IH} = V_{CC} Max	–	–	40	–	–	40	μAdc
I_{FA}, I_{FE}	Input Current "0"	V_{IL} = 0.45 V	–	-0.1	-0.25	–	-0.1	-0.25	mAdc
V_{OH}	Output Voltage "1"	I_{OH} = -2.0 mA, V_{CC} = V_{CC} Min	N/A	–	–	2.4	3.4	–	Vdc
V_{OL}	"0"	I_{OL} = +16 mA, V_{CC} = V_{CC} Min	–	0.35	0.45	–	0.35	0.45	Vdc
I_{OHE}	Output Disabled "1"	V_{OH}, V_{CC} = V_{CC} Max	–	–	100	–	–	100	μAdc
I_{OLE}	Current "0"	V_{OL} = +0.3 V, V_{CC} = V_{CC} Max	–	–	N/A	–	–	-100	μAdc
I_{OH}	Output Leakage "1"	V_{OH}, V_{CC} = V_{CC} Max	–	–	100	–	–	N/A	μAdc
V_{CL}	Input Clamp Voltage	I_{in} = -10 mA	–	–	-1.5	–	–	-1.5	Vdc
I_{OS}	Output Short Circuit Current	V_{CC} = V_{CC} Max, V_{out} = 0.0 V One Output Only for 1 s Max	N/A	–	N/A	15	–	70	mAdc
I_{CC}	Power Supply Current MCM7620/MCM7621	V_{CC} = V_{CC} Max All Inputs Grounded	–	60	100	–	60	100	mAdc

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Typ	Unit
Input Capacitance	C_{in}	8.0	pF
Output Capacitance	C_{out}	8.0	pF

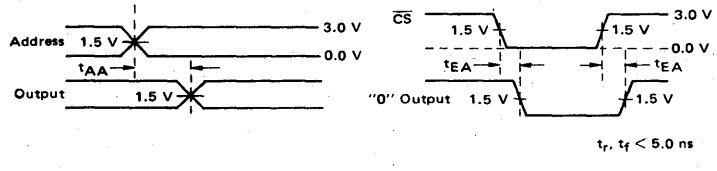
4

AC OPERATING CONDITIONS AND CHARACTERISTICS

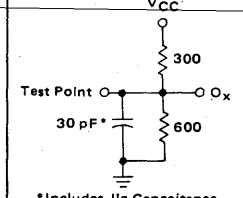
(Full operating voltage and temperature unless otherwise noted)

		0 to +70°C		-55 to +125°C		
Characteristic	Symbol	Typ	Max	Typ	Max	Unit
Address to Output Access Time	t_{AA}	45	70	45	85	ns
Chip Enable Access Time MCM7620/7621	t_{EA}	15	25	15	30	ns

TIMING DIAGRAM



AC TEST LOAD



PROGRAMMING

The PROMs are manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the sepcifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. These PROMs can be programmed automatically or by the manual procedure shown below.

PROGRAMMING PROCEDURE

1. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL-compatible. An open circuit should not be used to address the PROM.
2. Disable the chip by applying input highs (V_{IH}) to the $\overline{CS}$ input. The chip select is TTL-compatible. An open circuit should not be used to disable the chip.
3. Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open to achieve the disable.
4. Raise V_{CC} to V_{PH} with rise time equal to t_r.
5. After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.
7. Lower V_{CC} to 4.5 Volts following a delay of t_d from the last programming enable pulse applied to an output.
8. Enable the PROM for verification by applying a logic "0" (V_{IL}) to the $\overline{CS}$ input.
9. If any bit does not verify as programmed, repeat Steps 2 through 8 until the bit has received a total of 1.0 ms of programming time. Bits which do not program within 1.0 ms may be considered programming rejects. Multiple pulses of durations shorter than 1.0 ms may be used to enhance programming speed.
10. Repeat Steps 1 through 9 for all other bits to be programmed in the PROM.
11. Programming rejects returned to the factory must be accompanied by data giving address with desired and actual output data of a location in which a programming failure has occurred.

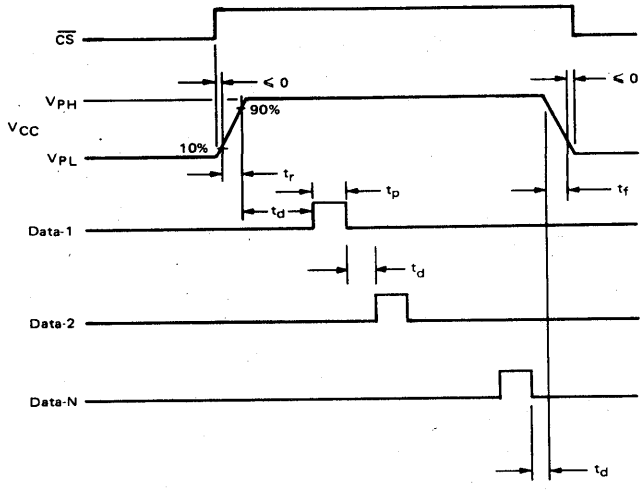
4

TABLE 1
PROGRAMMING SPECIFICATIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	Address Input	2.4	5.0	5.0	V
V_{IL}	Voltage(1)	0.0	0.4	0.8	V
V_{PH}	Programming/Verify	11.75	12.0	12.25	V
V_{PL}	Voltage to V_{CC}	4.5	4.5	5.5	V
I_{CCP}	Programming Voltage Current Limit Programming (V_{CC})	600	600	650	mA
t_r	Voltage Rise and	1	1	10	µs
t_f	Fall Time	1	1	10	µs
t_d	Programming Delay	10	10	100	µs
t_p	Programming Pulse Width	100	–	1000	µs
DC	Programming Duty Cycle	–	50	90	%
	Output Voltage				
V_{OPE}	Enable	10.0	10.5	11.0	V
V_{OPD}	Disable(2)	4.5	5.0	5.5	V
I_{OPE}	Output Voltage Enable Current	2	4	10	mA
T_C	Case Temperature	–	25	75	°C

(1) Address and chip select should not be left open for V_{IH}.
(2) Disable condition will be met with output open circuit.

FIGURE 1 – TYPICAL PROGRAMMING WAVEFORMS



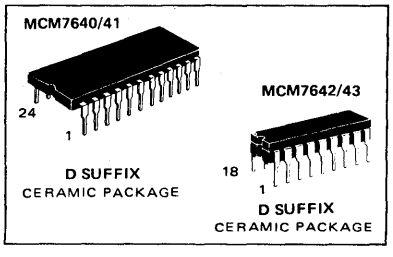
MOTOROLA

MCM7640 thru MCM7643

MTTL

4096-BIT PROGRAMMABLE READ ONLY MEMORIES

MCM7640 – 512 x 8 – Open-Collector
MCM7641 – 512 x 8 – Three-State
MCM7642 – 1024 x 4 – Open-Collector
MCM7643 – 1024 x 4 – Three-State



4096-BIT PROGRAMMABLE READ ONLY MEMORY

The MCM7640 through 43 PROMs comprise a completely compatible family having common dc electrical characteristics and identical programming requirements. They are fully-decoded, high-speed, field-programmable ROMs and are available in commonly used organizations, with both open-collector and three-state outputs. All bits are manufactured storing a logical "1" (outputs high), and can be selectively programmed for logical "0" (outputs low).

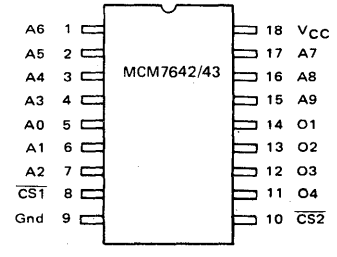
The field-programmable PROM can be custom programmed to any pattern using a simple programming procedure. Schottky bipolar circuitry provides fast access time, and features temperature and voltage compensation to minimize access time variations.

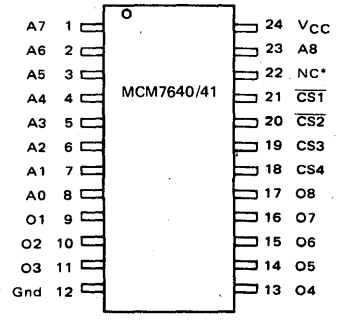
All pinouts are compatible to industry-standard PROMs and ROMs.

In addition to the conventional storage array, extra test rows and columns are included to assure high programmability, and guarantee parametric and ac performance. Fuses in these test rows and columns are blown prior to shipment.

- Common dc Electrical Characteristics and Programming Procedure
- Simple, High-Speed Programming Procedure
  (0.1 Second per 1024 Bits, Typical)
- Expandable – Open-Collector or Three-State Outputs and Chip Enable Inputs
- Inputs and Outputs TTL-Compatible
  Low Input Current – 250 μA Logic "0", 40 μA Logic "1"
  Full Output Drive – 16 mA Sink, 2.0 mA Source
- Fast Access Time – Guaranteed for Worst-Case N^2 Sequencing; Over Commercial and Military Temperature and Voltage Ranges
- Pin-Compatible with Industry-Standard PROMs and ROMs

PIN ASSIGNMENT





*No Connection

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage (operating)	V_{CC}	+7.0	Vdc
Input Voltage	V_{in}	+5.5	Vdc
Output Voltage (operating)	V_{OH}	+7.0	Vdc
Supply Current	I_{CC}	650	mAdc
Input Current	I_{in}	-20	mAdc
Output Sink Current	I_o	100	mAdc
Operating Temperature Range MCM76xxDM MCM76xxDC	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Maximum Junction Temperature	T_J	+175	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. (While programming, follow the programming specifications.)

4

DC OPERATING CONDITIONS AND CHARACTERISTICS

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}				Vdc
MCM76xxDM		4.50	5.0	5.50	
MCM76xxDC		4.75	5.0	5.25	
Input High Voltage	V_{IH}	2.0	–	–	Vdc
Input Low Voltage	V_{IL}	–	–	0.8	Vdc

DC CHARACTERISTICS

			Open-Collector Output			Three-State Output			
Symbol	Parameter	Test Conditions	Min	Typ	Max	Min	Typ	Max	Unit
I_{RA}, I_{RE}	Address/Enable "1"	$V_{IH} = V_{CC}$ Max	–	–	40	–	–	40	µAdc
I_{FA}, I_{FE}	Input Current "0"	V_{IL} = 0.45 V	–	-0.1	-0.25	–	-0.1	-0.25	mAdc
V_{OH}	Output Voltage "1"	I_{OH} = -2.0 mA, $V_{CC} = V_{CC}$ Min	N/A	–	–	2.4	3.4	–	Vdc
V_{OL}	"0"	I_{OL} = +16 mA, $V_{CC} = V_{CC}$ Min	–	0.35	0.45	–	0.35	0.45	Vdc
I_{OHE}	Output Disabled "1"	V_{OH}, $V_{CC} = V_{CC}$ Max	–	–	100	–	–	100	µAdc
I_{OLE}	Current "0"	V_{OL} = +0.3 V, $V_{CC} = V_{CC}$ Max	–	–	N/A	–	–	-100	µAdc
I_{OH}	Output Leakage "1"	V_{OH}, $V_{CC} = V_{CC}$ Max	–	–	100	–	–	N/A	µAdc
V_{CL}	Input Clamp Voltage	I_{in} = -10 mA	–	–	-1.5	–	–	-1.5	Vdc
I_{OS}	Output Short Circuit Current	$V_{CC} = V_{CC}$ Max, V_{out} = 0.0 V One Output Only for 1 s Max	N/A	–	N/A	15	–	70	mAdc
I_{CC}	Power Supply Current	$V_{CC} = V_{CC}$ Max							
	MCM7640/MCM7641	All Inputs Grounded	–	100	140	–	100	140	mAdc
	MCM1642/MCM7643		–	100	140	–	100	140	mAdc

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Typ	Unit
Input Capacitance	C_{in}	8.0	pF
Output Capacitance	C_{out}	8.0	pF

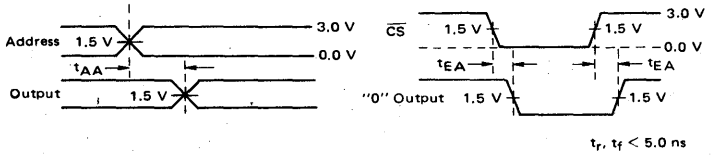
4

AC OPERATING CONDITIONS AND CHARACTERISTICS

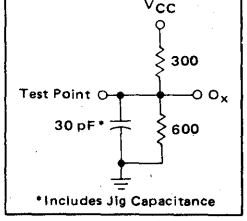
(Full operating voltage and temperature unless otherwise noted)

		0 to +70°C		-55 to +125°C		
Characteristic	Symbol	Typ	Max	Typ	Max	Unit
Address to Output Access Time	t_{AA}	45	70	45	85	ns
Chip Enable Access Time	t_{EA}					ns
MCM7640/7641		30	40	30	50	
MCM7642/7643		15	25	15	30	

TIMING DIAGRAM



AC TEST LOAD



PROGRAMMING

The PROMs are manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the sepcifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. These PROMs can be programmed automatically or by the manual procedure shown below.

PROGRAMMING PROCEDURE

1. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL-compatible. An open circuit should not be used to address the PROM.
2. Disable the chip by applying input highs (V_{IH}) to the $\overline{CS}$ input(s). CS inputs (MCM7640/41 only) must remain at V_{IH} for program and verify. The chip select is TTL-compatible. An open circuit should not be used to disable the chip.
3. Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open to achieve the disable.
4. Raise V_{CC} to V_{PH} with rise time equal to t_r.
5. After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.
7. Lower V_{CC} to 4.5 Volts following a delay of t_d from the last programming enable pulse applied to an output.
8. Enable the PROM for verification by applying a logic "0" (V_{IL}) to the $\overline{CS}$ input(s).
9. If any bit does not verify as programmed, repeat Steps 2 through 8 until the bit has received a total of 1.0 ms of programming time. Bits which do not program within 1.0 ms may be considered programming rejects. Multiple pulses of durations shorter than 1.0 ms may be used to enhance programming speed.
10. Repeat Steps 1 through 9 for all other bits to be programmed in the PROM.
11. Programming rejects returned to the factory must be accompanied by data giving address with desired and actual output data of a location in which a programming failure has occurred.

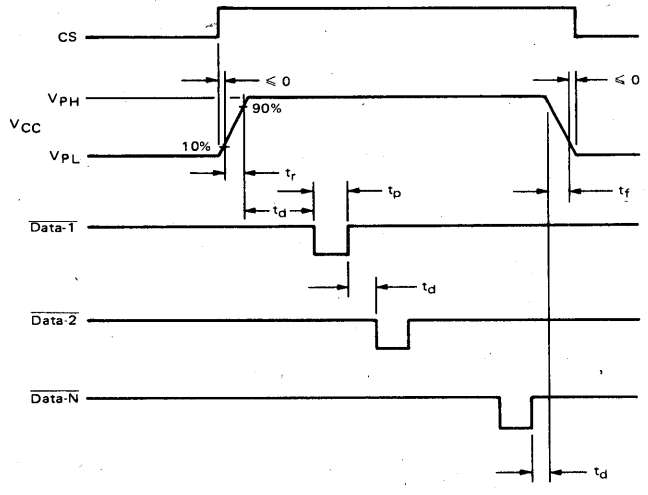
4

TABLE 1
PROGRAMMING SPECIFICATIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	Address Input	2.4	5.0	5.0	V
V_{IL}	Voltage(1)	0.0	0.4	0.8	V
V_{PH}	Programming/Verify	11.75	12.0	12.25	V
V_{PL}	Voltage to V_{CC}	4.5	4.5	5.5	V
I_{CCP}	Programming Voltage Current Limit Programming (V_{CC})	600	600	650	mA
t_r	Voltage Rise and	1	1	10	μs
t_f	Fall Time	1	1	10	μs
t_d	Programming Delay	10	10	100	μs
t_p	Programming Pulse Width	100	–	1000	μs
DC	Programming Duty Cycle	–	50	90	%
	Output Voltage				
V_{OPE}	Enable	10.0	10.5	11.0	V
V_{OPD}	Disable(2)	4.5	5.0	5.5	V
I_{OPE}	Output Voltage Enable Current	2	4	10	mA
T_C	Case Temperature	–	25	75	°C

(1) Address and chip select should not be left open for V_{IH}.
(2) Disable condition will be met with output open circuit.

FIGURE 1 – TYPICAL PROGRAMMING WAVEFORMS



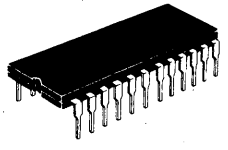
4

MOTOROLA

MCM7680
MCM7681

MTTL
8192-BIT PROGRAMMABLE READ ONLY MEMORIES

MCM7680 – 1024 X 8 – Open-Collector
MCM7681 – 1024 X 8 – Three-State



CERAMIC PACKAGE
CASE 623

8192-BIT PROGRAMMABLE READ ONLY MEMORY

The MCM7680/81 together with the MCM7620/21, MCM7640/43 comprise a complete, compatible family having common dc electrical characteristics and identical programming requirements. They are fully decoded, high-speed, field-programmable ROMs and are available in commonly used organizations, with both open-collector and three-state outputs. All bits are manufactured storing a logical "1" (outputs high), and can be selectively programmed for logical "0" (outputs low).

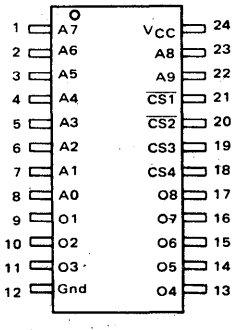
The field-programmable PROM can be custom-programmed to any pattern using a simple programming procedure. Schottky bipolar circuitry provides fast access time, and features temperature and voltage compensation to minimize access time variations.

Pinouts are compatible to industry-standard PROMs and ROMs. In addition, the MCM7680 and 81 are pin compatible replacement for the 512 X 8 with pin 2 connected as A9 on the 1024 X 8.

In addition to the conventional storage array, extra test rows and columns are included to assure high programmability, and guarantee parametric and ac performance. Fuses in these test rows and columns are blown prior to shipment.

- Common dc Electrical Characteristics and Programming Procedure
- Simple, High-Speed Programming Procedure (0.1 second per 1024 Bits, Typical)
- Expandable – Open-Collector or Three-State Outputs and Chip Enable Inputs
- Inputs and Outputs TTL-Compatible
  Low Input Current – 250 μA Logic "0", 40 μA Logic "1"
  Full Output Drive – 16 mA Sink, 2.0 mA Source
- Fast Access Time – Guaranteed for Worst-Case N^2 Sequencing, Over Commercial and Military Temperature Ranges
- Pin-Compatible with Industry-Standard PROMs and ROMs

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage (operating)	V_{CC}	+7.0	Vdc
Input Voltage	V_{in}	+5.5	Vdc
Output Voltage (operating)	V_{OH}	+7.0	Vdc
Supply Current	I_{CC}	650	mAdc
Input Current	I_{in}	-20	mAdc
Output Sink Current	I_o	100	mAdc
Operating Temperature Range MCM76xxDM MCM76xxDC	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Maximum Junction Temperature	T_J	+175	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. (While programming, follow the programming specifications.)

4

DC OPERATING CONDITIONS AND CHARACTERISTICS

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}				Vdc
MCM76xxDM		4.50	5.0	5.50	
MCM76xxDC		4.75	5.0	5.25	
Input High Voltage	V_{IH}	2.0	–	–	Vdc
Input Low Voltage	V_{IL}	–	–	0.8	Vdc

DC CHARACTERISTICS

			Open-Collector Output			Three-State Output			
Symbol	Parameter	Test Conditions	Min	Typ	Max	Min	Typ	Max	Unit
I_{RA}, I_{RE}	Address/Enable "1"	V_{IH} = V_{CC} Max	–	–	40	–	–	40	μAdc
I_{FA}, I_{FE}	Input Current "0"	V_{IL} = 0.45 V	–	-0.1	-0.25	–	-0.1	-0.25	mAdc
V_{OH}	Output Voltage "1"	I_{OH} = -2.0 mA, V_{CC} = V_{CC} Min	N/A	–	–	2.4	3.4	–	Vdc
V_{OL}	"0"	I_{OL} = +16 mA, V_{CC} = V_{CC} Min	–	0.35	0.45	–	0.35	0.45	Vdc
I_{OHE}	Output Disabled "1"	V_{OH}, V_{CC} = V_{CC} Max	–	–	100	–	–	100	μAdc
I_{OLE}	Current "0"	V_{OL} = +0.3 V, V_{CC} = V_{CC} Max	–	–	N/A	–	–	-100	μAdc
I_{OH}	Output Leakage "1"	V_{OH}, V_{CC} = V_{CC} Max	–	–	100	–	–	N/A	μAdc
V_{CL}	Input Clamp Voltage	I_{in} = -10 mA	–	–	-1.5	–	–	-1.5	Vdc
I_{OS}	Output Short Circuit Current	V_{CC} = V_{CC} Max, V_{out} = 0.0 V One Output Only for 1 s Max	N/A	–	N/A	15	–	70	mAdc
I_{CC}	Power Supply Current	V_{CC} = V_{CC} Max							
	MCM7680/MCM7681DC	All Inputs Grounded	–	110	150	–	110	150	mAdc
	MCM7680/MCM7681DM		–	110	170	–	110	170	mAdc

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Typ	Unit
Input Capacitance	C_{in}	8.0	pF
Output Capacitance	C_{out}	8.0	pF

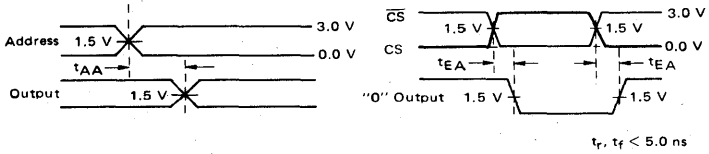
4

AC OPERATING CONDITIONS AND CHARACTERISTICS

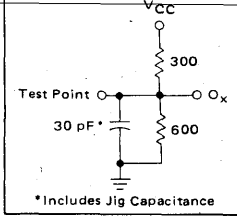
(Full operating voltage and temperature unless otherwise noted)

		0 to +70°C		-55 to +125°C		
Characteristic	Symbol	Typ	Max	Typ	Max	Unit
Address to Output Access Time	t_{AA}	45	70	45	85	ns
Chip Enable Access Time MCM7680/81	t_{EA}	30	40	30	50	ns

TIMING DIAGRAM



AC TEST LOAD



PROGRAMMING

The PROMs are manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the sepcifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. These PROMs can be programmed automatically or by the manual procedure shown below.

PROGRAMMING PROCEDURE

1. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL-compatible. An open circuit should not be used to address the PROM.
2. Disable the chip by applying inputs highs (V_{IH}) to the $\overline{CS}$ inputs. CS inputs must remain at V_{IH} for program and verify. The chip select is TTL-compatible. An open circuit should not be used to disable the chip.
3. Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open to achieve the disable.
4. Raise V_{CC} to V_{PH} with rise time equal to t_r.
5. After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.
7. Lower V_{CC} to 4.5 Volts following a delay of t_d from the last programming enable pulse applied to an output.
8. Enable the PROM for verification by applying a logic "0" (V_{IL}) to the $\overline{CS}$ inputs.
9. If any bit does not verify as programmed, repeat Steps 2 through 8 until the bit has received a total of 1.0 ms of programming time. Bits which do not program within 1.0 ms may be considered programming rejects. Multiple pulses of durations shorter than 1.0 ms may be used to enhance programming speed.
10. Repeat Steps 1 through 9 for all other bits to be programmed in the PROM.
11. Programming rejects returned to the factory must be accompanied by data giving address with desired and actual output data of a location in which a programming failure has occurred.

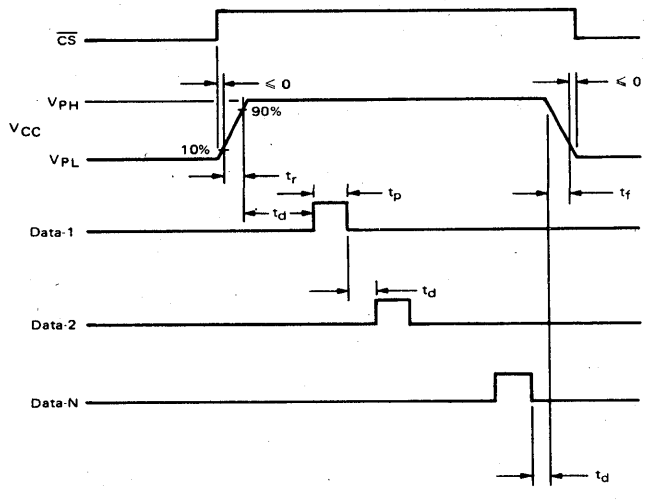
4

TABLE 1
PROGRAMMING SPECIFICATIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	Address Input	2.4	5.0	5.0	V
V_{IL}	Voltage(1)	0.0	0.4	0.8	V
V_{PH}	Programming/Verify	11.75	12.0	12.25	V
V_{PL}	Voltage to V_{CC}	4.5	4.5	5.5	V
I_{CCP}	Programming Voltage Current Limit Programming (V_{CC})	600	600	650	mA
t_r	Voltage Rise and	1	1	10	μs
t_f	Fall Time	1	1	10	μs
t_d	Programming Delay	10	10	100	μs
t_p	Programming Pulse Width	100	–	1000	μs
DC	Programming Duty Cycle	–	50	90	%
	Output Voltage				
V_{OPE}	Enable	10.0	10.5	11.0	V
V_{OPD}	Disable(2)	4.5	5.0	5.5	V
I_{OPE}	Output Voltage Enable Current	2	4	10	mA
T_C	Case Temperature	–	25	75	°C

(1) Address and chip select should not be left open for V_{IH}.
(2) Disable condition will be met with output open circuit.

FIGURE 1 – TYPICAL PROGRAMMING WAVEFORMS



4

MOTOROLA

MCM7684
MCM7685

Advance Information

8192-BIT PROGRAMMABLE READ ONLY MEMORY

The MCM7684/85 together with the MCM7620/21/40/41/42/43/80/81 comprise a complete, compatible family having common dc electrical characteristics and identical programming requirements. They are fully decoded, high-speed, field-programmable ROMs and are available in commonly used organizations, with both open-collector and three-state outputs. All bits are manufactured storing a logical "1" (outputs high), and can be selectively programmed for logical "0" (outputs low).

The field-programmable PROM can be custom-programmed to any pattern using a simple programming procedure. Schottky bipolar circuitry provides fast access time, and features temperature and voltage compensation to minimize access time variations.

Pinouts are compatible to industry-standard PROMs and ROMs. In addition, the MCM7684 and 85 are pin compatible replacement for the 1024 X 4 with pin 8 connected as A10 on the 2048 X 4.

In addition to the conventional storage array, extra test rows and columns are included to assure high programmability, and guarantee parametric and ac performance. Fuses in these test rows and columns are blown prior to shipment.

- Common dc Electrical Characteristics and Programming Procedure
- Simple, High-Speed Programming Procedure (0.1 second per 1024 Bits, Typical)
- Expandable – Open-Collector or Three-State Outputs and Chip Enable Input
- Inputs and Outputs TTL-Compatible
  Low Input Current – 250 μA Logic "0", 40 μA Logic "1"
  Full Output Drive – 16 mA Sink, 2.0 mA Source
- Fast Access Time – Guaranteed for Worst-Case N^2 Sequencing, Over Commercial and Military Temperature Ranges
- Pin-Compatible with Industry-Standard PROMs and ROMs

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage (operating)	V_{CC}	+7.0	Vdc
Input Voltage	V_{in}	+5.5	Vdc
Output Voltage (operating)	V_{OH}	+7.0	Vdc
Supply Current	I_{CC}	650	mAdc
Input Current	I_{in}	-20	mAdc
Output Sink Current	I_O	100	mAdc
Operating Temperature Range MCM76xxDM MCM76xxDC	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Maximum Junction Temperature	T_J	+175	°C

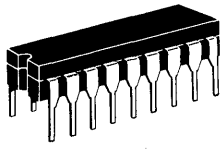
NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. (While programming, follow the programming specifications.)

This is advance information and specifications are subject to change without notice.

MTTL

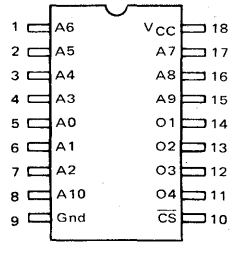
8192-BIT PROGRAMMABLE READ ONLY MEMORIES

MCM7684 – 2048 X 4 – Open-Collector
MCM7685 – 2048 X 4 – Three-State



D SUFFIX
CERAMIC PACKAGE
CASE 726

PIN ASSIGNMENT



4

DC OPERATING CONDITIONS AND CHARACTERISTICS

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}				Vdc
MCM76xxDM		4.50	5.0	5.50	
MCM76xxDC		4.75	5.0	5.25	
Input High Voltage	V_{IH}	2.0	–	–	Vdc
Input Low Voltage	V_{IL}	–	–	0.8	Vdc

DC CHARACTERISTICS

(Over Recommended Operating Temperature Range)

				Open-Collector Output			Three-State Output			
Symbol	Parameter		Test Conditions	Min	Typ	Max	Min	Typ	Max	Unit
I_{RA}, I_{RE}	Address/Enable	"1"	$V_{IH} = V_{CC}$ Max	–	–	40	–	–	40	μAdc
I_{FA}, I_{FE}	Input Current	"0"	V_{IL} = 0.45 V	–	-0.1	-0.25	–	-0.1	-0.25	mAdc
V_{OH}	Output Voltage	"1"	I_{OH} = -2.0 mA, V_{CC} Min	N/A	–	–	2.4	3.4	–	Vdc
V_{OL}		"0"	I_{OL} = +16 mA, V_{CC} Min	–	0.35	0.45	–	0.35	0.45	Vdc
I_{OHZ}	Output Disabled	"1"	V_{OH}, V_{CC} Max	–	–	100	–	–	100	μAdc
I_{OLZ}	Current	"0"	V_{OL} = +0.3 V, V_{CC} Max	–	–	N/A	–	–	-100	μAdc
I_{OH}	Output Leakage	"1"	V_{OH}, V_{CC} Max	–	–	100	–	–	N/A	μAdc
V_{IC}	Input Clamp Voltage		I_{in} = -10 mA	–	–	-1.5	–	–	-1.5	Vdc
I_{OS}	Output Short Circuit Current		V_{CC} Max, V_{out} = 0.0 V One Output Only for 1 s Max	N/A	–	N/A	15	–	70	mAdc
I_{CC}	Power Supply Current		V_{CC} Max All Inputs Grounded							
	MCM7684/MCM7685 DC			–	80	120	–	80	120	mAdc
	MCM7684/MCM7685 DM			–	80	140	–	80	140	mAdc

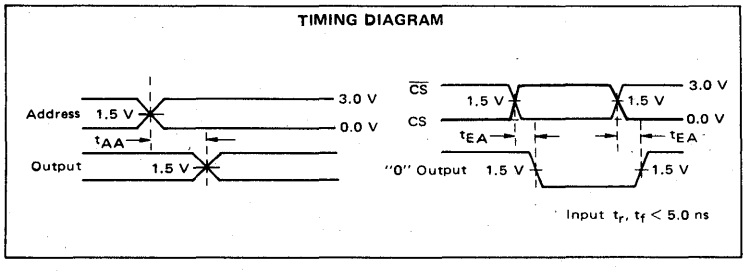
CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

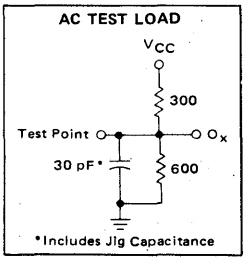
Characteristic	Symbol	Typ	Unit
Input Capacitance	C_{in}	8.0	pF
Output Capacitance	C_{out}	8.0	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted)

		0 to +70°C		-55 to +125°C		
Characteristic	Symbol	Typ	Max	Typ	Max	Unit
Address to Output Access Time	t_{AA}	45	70	45	85	ns
Chip Enable Access Time	t_{EA}	15	25	15	30	ns





PROGRAMMING

The PROMs are manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the sepcifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. These PROMs can be programmed automatically or by the manual procedure shown below.

PROGRAMMING PROCEDURE

1. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL-compatible. An open circuit should not be used to address the PROM.
2. Disable the chip by applying an input high (V_{IH}) to the $\overline{CS}$ input. The chip select is TTL-compatible. An open circuit should not be used to disable the chip.
3. Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open to achieve the disable.
4. Raise V_{CC} to V_{PH} with rise time equal to t_r.
5. After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.
7. Lower V_{CC} to 4.5 Volts following a delay of t_d from the last programming enable pulse applied to an output.
8. Enable the PROM for verification by applying a logic "0" (V_{IL}) to the $\overline{CS}$ inputs.
9. If any bit does not verify as programmed, repeat Steps 2 through 8 until the bit has received a total of 1.0 ms of programming time. Bits which do not program within 1.0 ms may be considered programming rejects. Multiple pulses of durations shorter than 1.0 ms may be used to enhance programming speed.
10. Repeat Steps 1 through 9 for all other bits to be programmed in the PROM.
11. Programming rejects returned to the factory must be accompanied by data giving address with desired and actual output data of a location in which a programming failure has occurred.

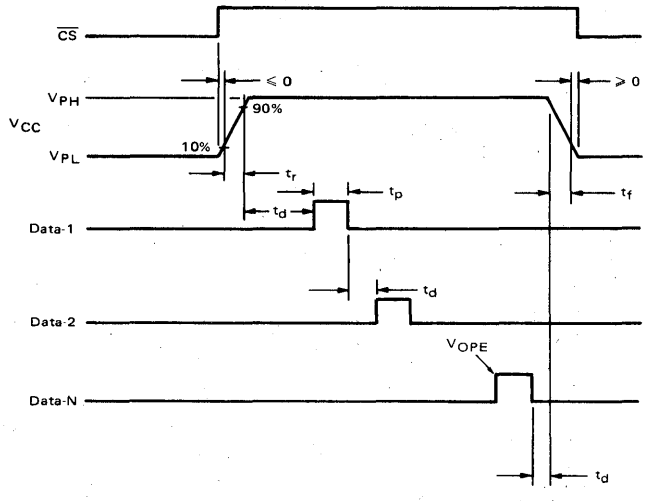
4

TABLE 1
PROGRAMMING SPECIFICATIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH} V_{IL}	Address Input Voltage(1)	2.4 0.0	5.0 0.4	5.0 0.8	V V
V_{PH} V_{PL}	Programming/Verify Voltage to V_{CC}	11.75 4.5	12.0 4.5	12.25 5.5	V V
I_{CCP}	Programming Voltage Current Limit Programming (V_{CC})	600	600	650	mA
t_r t_f	Voltage Rise and Fall Time	1 1	1 1	10 10	µs µs
t_d	Programming Delay	10	10	100	µs
t_p	Programming Pulse Width	100	–	1000	µs
DC	Programming Duty Cycle	–	50	90	%
V_{OPE} V_{OPD}	Output Voltage Enable Disable(2)	10.0 4.5	10.5 5.0	11.0 5.5	V V
I_{OPE}	Output Voltage Enable Current	2	4	10	mA
T_C	Case Temperature	–	25	75	°C

(1) Address and chip select should not be left open for V_{IH}.
(2) Disable condition will be met with output open circuit.

FIGURE 1 – TYPICAL PROGRAMMING WAVEFORMS



4

MECL MEMORIES
GENERAL INFORMATION

Complete information is available in the MECL Data Book. Contact your sales representative or authorized distributor for information.

TABLE 1 — LIMITS BEYOND WHICH DEVICE LIFE MAY BE IMPAIRED

Characteristic	Symbol	Rating	Unit
Supply Voltage	V_{EE}	−8.0 to 0	V
Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	V
Output Source Current — Continuous Surge	I_{out}	50 100	mA
Junction Temperature — Ceramic Package① Plastic Package	T_J	165 150	°C
Storage Temperature	T_{stg}	−55 to +150	°C

① Maximum T_J may be exceeded ($\leq$ 250°C) for short periods of time ($\leq$ 240 hours) without significant reduction in device life.

TABLE 2 — LIMITS BEYOND WHICH PERFORMANCE MAY BE DEGRADED

Characteristic	Symbol	Rating	Unit
Supply Voltage (V_{CC} = 0)②	V_{EE}	−4.94 to −5.46	V
Output Drive — MCM10100 Series MCM10500 Series	—	50 Ω to −2.0 V 100 Ω to −2.0 V	Ω
Operating Temperature Range③ MCM10100 Series MCM10500 Series	T_A	 0 to 75 −55 to +125	°C

② Functionality only. Data sheet limits are specified for −5.19 to −5.21 V.
③ With airflow $\geq$ 500 lfpm.

4

TABLE 3 – DC TEST PARAMETERS

Each MECL 10,000 series device has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 linear feet per minute is maintained. V_{EE} = −5.2 V ±0.010 V.

Forcing Function	Parameter	−55°C MCM10500*	0°C MCM10100**	25°C MCM10100**	25°C MCM10500*	75°C MCM10100**	125°C MCM10500*
V_{IHmax} =	V_{OHmax}	−0.880	−0.840	−0.810	−0.780	−0.720	−0.630
	V_{OHmin}	−1.080	−1.000	−0.960	−0.930	−0.900	−0.825
	V_{OHAmin}	−1.100	−1.020	−0.980	−0.950	−0.920	−0.845
V_{IHAmin}		−1.255	−1.145	−1.105	−1.105	−1.045	−1.000
V_{ILAmin}		−1.510	−1.490	−1.475	−1.475	−1.450	−1.400
	V_{OLAmin}	−1.635	−1.645	−1.630	−1.600	−1.605	−1.525
	V_{OLAmax}	−1.655	−1.665	−1.650	−1.620	−1.625	−1.545
V_{ILmin} =	V_{OLmin}	−1.920	−1.870	−1.850	−1.850	−1.830	−1.820
V_{ILmin}	I_{INLmin}	0.5	0.5	0.5	0.5	0.3	0.3

*Driving 100 Ω to −2.0 V.
**Driving 50 Ω to −2.0 V.

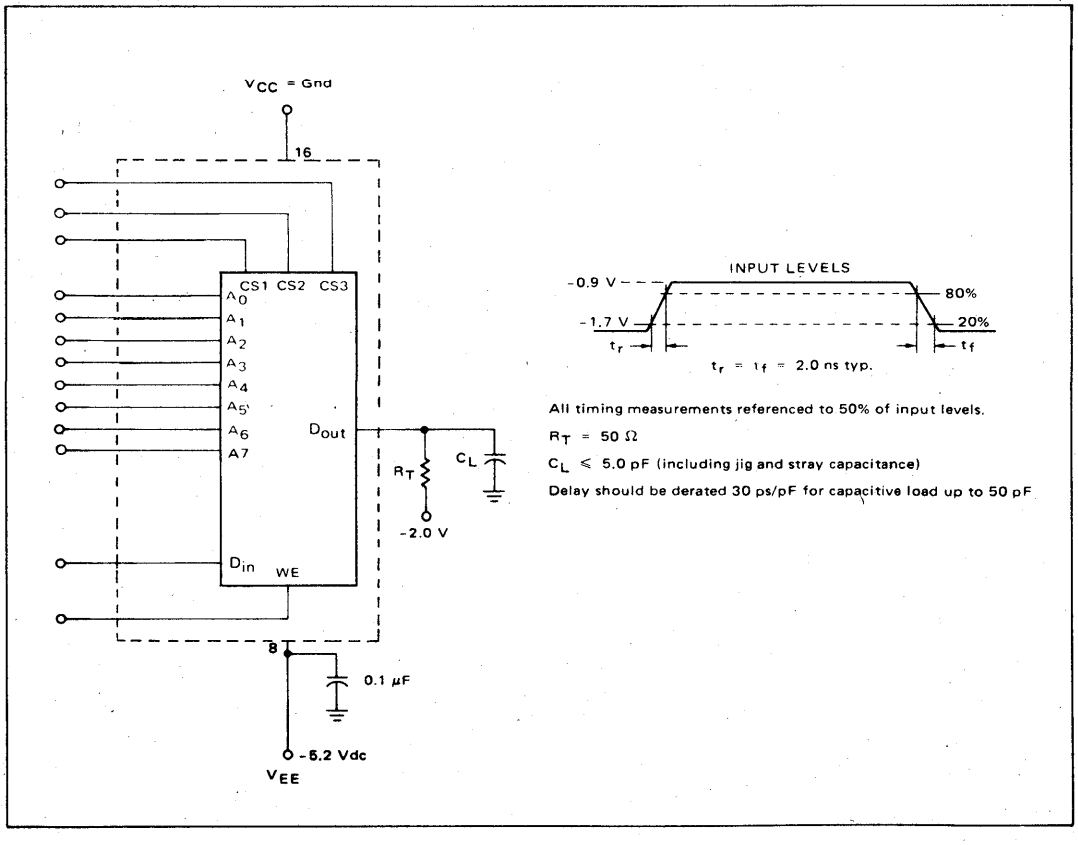


FIGURE 1 – SWITCHING TIME TEST CIRCUIT

FIGURE 2 – CHIP SELECT ACCESS TIME WAVEFORM

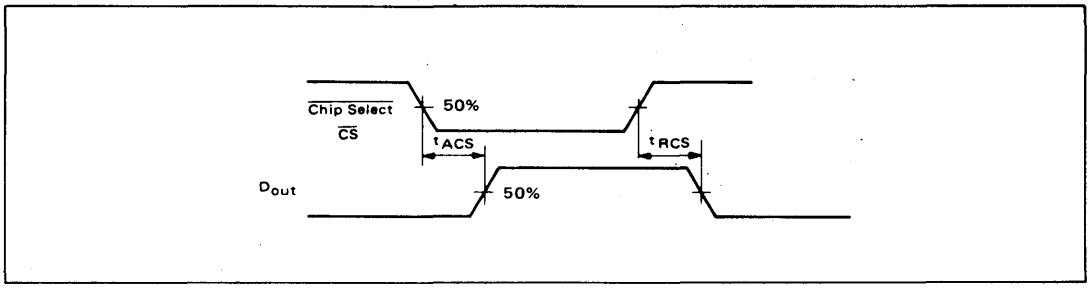


FIGURE 3 – ADDRESS ACCESS TIME WAVEFORM

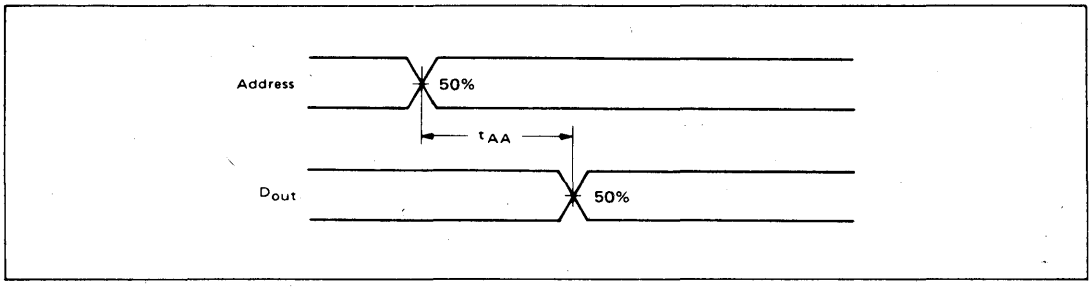
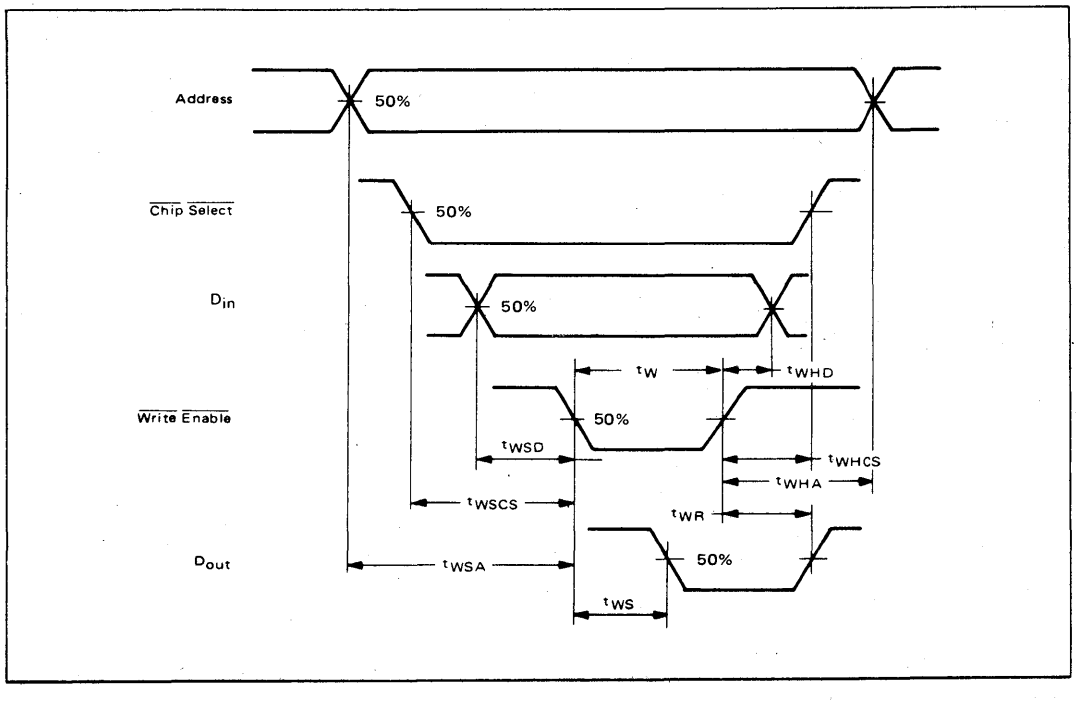


FIGURE 4 – SETUP AND HOLD WAVEFORMS (WRITE MODE)



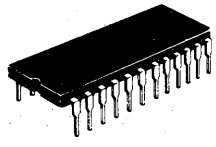
4

MCM10143

8 X 2 MULTIPORT REGISTER FILE (RAM)

8 x 2 MULTIPORT REGISTER FILE (RAM)

The MCM10143 is an 8 word by 2 bit multiport register file (RAM) capable of reading two locations and writing one location simultaneously. Two sets of eight latches are used for data storage in this LSI circuit.



L SUFFIX
CERAMIC PACKAGE
CASE 623

WRITE

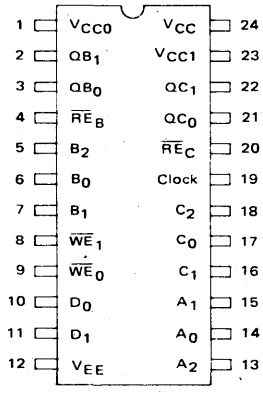
The word to be written is selected by addresses A_0–A_2. Each bit of the word has a separate write enable to allow more flexibility in system design. A write occurs on the positive transition of the clock. Data is enabled by having the write enables at a low level when the clock makes the transition. To inhibit a bit from being written, the bit enable must be at a high level when the clock goes low and not change until the clock goes high. Operation of the clock and the bit enables can be reversed. While the clock is low a positive transition of the bit enable will write that bit into the address selected by A_0–A_2.

READ

When the clock is high any two words may be read out simultaneously, as selected by addresses B_0–B_2 and C_0–C_2, including the word written during the preceding half clock cycle. When the clock goes low the addressed data is stored in the slaves. Level changes on the read address lines have no effect on the output until the clock again goes high. Read out is accomplished at any time by enabling output gates (B_0–B_1), (C_0–C_1).

t_{pd}:
Clock to Data out = 5 ns (typ)
(Read Selected)
Address to Data out = 10 ns (typ)
(Clock High)
$\overline{\text{Read Enable}}$ to Data out = 2.8 ns (typ)
(Clock high, Addresses present)
P_D = 610 mW/pkg (typ no load)

PIN ASSIGNMENT

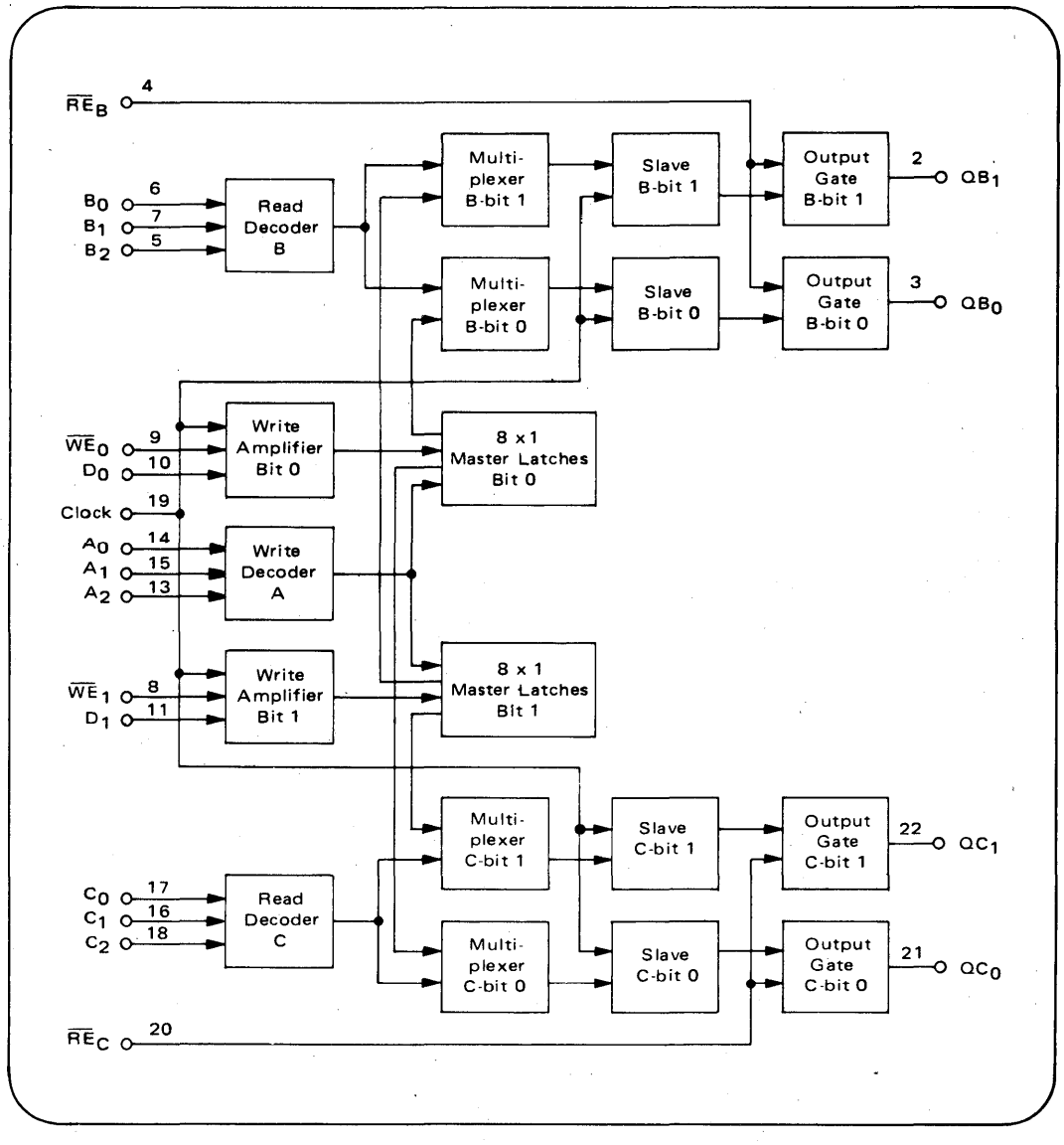


TRUTH TABLE

*MODE	INPUT							OUTPUT			
	**Clock	$\overline{WE}_0$	$\overline{WE}_1$	D_0	D_1	$\overline{RE}_B$	$\overline{RE}_C$	QB_0	QB_1	QC_0	QC_1
Write	L→H	L	L	H	H	H	H	L	L	L	L
Read	H	ϕ	ϕ	ϕ	ϕ	L	L	H	H	H	H
Read	H→L	ϕ	ϕ	ϕ	ϕ	L	L	H	H	H	H
Read	L→H→L	H	H	ϕ	ϕ	L	L	H	H	H	H
Write	L→H	L	L	L	H	H	H	L	L	L	L
Read	H	ϕ	ϕ	ϕ	ϕ	L	L	L	H	L	H

**Note: Clock occurs sequentially through Truth Table
*Note: A0-A2, B0-B2, and C0-C2 are all set to same address location throughout Table.
ϕ = Don't Care

BLOCK DIAGRAM



4

ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	0°C		+25°C			+75°C		Unit
		Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	–	150	–	118	150	–	150	mAdc
Input Current	I_{inH}								μAdc
Pins 10, 11, 19		–	245	–	–	245	–	245	
All other pins		–	200	–	–	200	–	200	
Switching Times ①									ns
Read Mode									
Address Input	$t_{B\pm QB\pm}$	4.0	15.3	4.5	10	14.5	4.5	15.5	
$\overline{\text{Read Enable}}$	$t_{\overline{RE}-QB+}$	1.1	5.3	1.2	3.5	5.0	1.2	5.5	
Data	$t_{Clock+QB-}$	1.7	7.3	2.0	5.0	7.0	2.0	7.6	
Setup									
Address	$t_{setup(B-Clock-)}$	–	–	8.5	5.5	–	–	–	
Hold									
Address	$t_{hold(Clock-B+)}$	–	–	-1.5	-4.5	–	–	–	
Write Mode									
Setup									
$\overline{\text{Write Enable}}$	$t_{setup(\overline{WE}-Clock+)}$	–	–	7.0	4.0	–	–	–	
	$t_{setup(\overline{WE}+Clock-)}$	–	–	1.0	-2.0	–	–	–	
Address	$t_{setup(A-Clock+)}$	–	–	8.0	5.0	–	–	–	
Data	$t_{setup(D-Clock+)}$	–	–	5.0	2.0	–	–	–	
Hold									
$\overline{\text{Write Enable}}$	$t_{hold(Clock+\overline{WE}+)}$	–	–	5.5	2.5	–	–	–	
	$t_{hold(Clock+\overline{WE}-)}$	–	–	1.0	-2.0	–	–	–	
Address	$t_{hold(Clock+A+)}$	–	–	1.0	-3.0	–	–	–	
Data	$t_{hold(Clock+D+)}$	–	–	1.0	-2.0	–	–	–	
Write Pulse Width	$PW_{\overline{WE}}$	–	–	8.0	5.0	–	–	–	
Rise Time, Fall Time (20% to 80%)	t_r, t_f	1.1	4.2	1.1	2.5	4.0	1.1	4.5	

①AC timing figures do not show all the necessary presetting conditions.

4

READ TIMING DIAGRAMS

Access (Clock High)

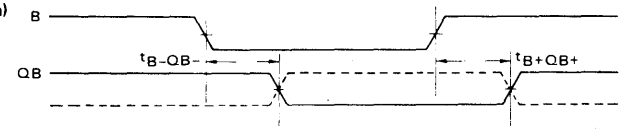


FIGURE 1

Enable

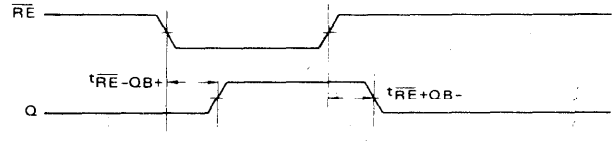


FIGURE 2

Data
(Address Selected)

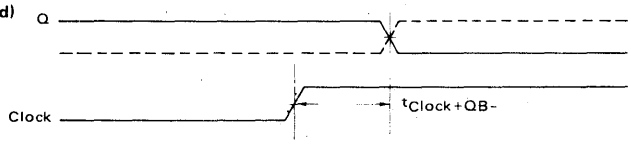


FIGURE 3

Setup and Hold

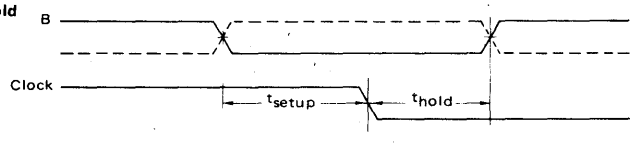


FIGURE 4

4

WRITE TIMING DIAGRAM

Enable Setup

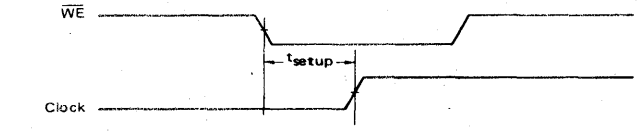


FIGURE 5

Enable Hold

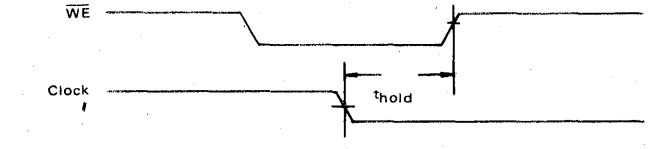


FIGURE 6

Disable

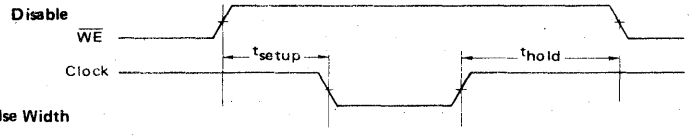


FIGURE 7

Pulse Width

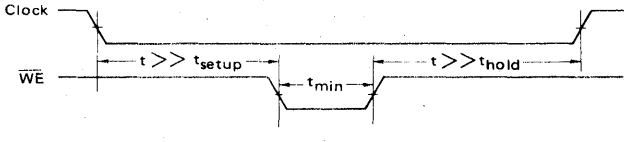


FIGURE 8

Address

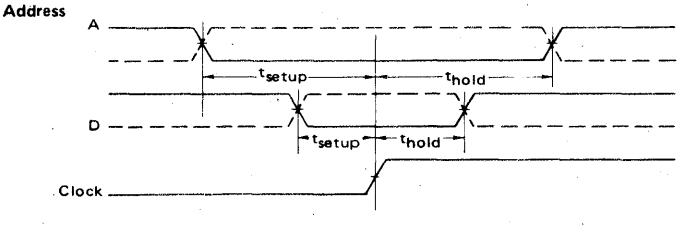
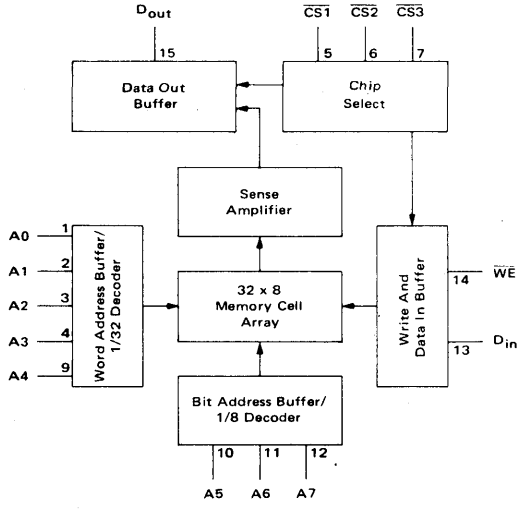


FIGURE 9

4

MCM10144/MCM10544

256 X 1-BIT RANDOM ACCESS MEMORY



The MCM10144/10544 is a 256 word X 1-bit RAM. Bit selection is achieved by means of an 8-bit address A0 through A7.

The active-low chip select allows memory expansion up to 2048 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM ($\overline{CS}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_{in} is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at D_{out}.

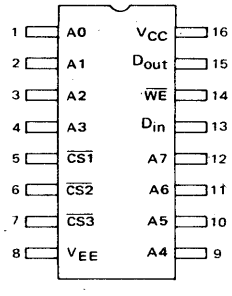
- Typical Address Access Time = 17 ns
- Typical Chip Select Access Time = 4.0 ns
- 50 kΩ Input Pulldown Resistors on Chip Select
- Power Dissipation (470 mW typ @ 25°C) Decreases with Increasing Temperature
- Pin-for-Pin Replacement for F10410

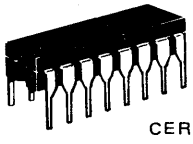
TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$*	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

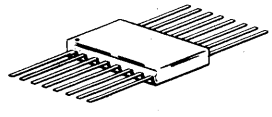
* $\overline{CS} = \overline{CS1} + \overline{CS2} + \overline{CS3}$ ϕ = Don't Care.

PIN ASSIGNMENT





L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

4

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	−55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	—	140	—	135	—	130	—	125	—	125	mAdc
Input Current High	I_{inH}	—	375	—	220	—	220	—	220	—	220	μAdc

−55°C and +125°C test values apply to MC105xx devices only.

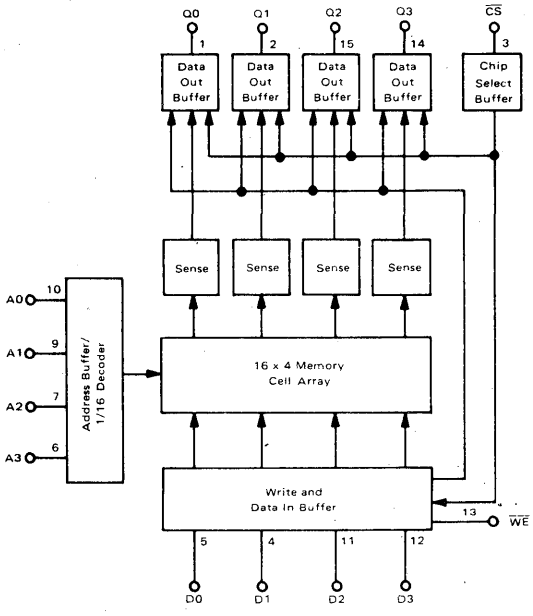
SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10144 T_A = 0 to +75°C, V_{EE} = −5.2 Vdc ± 5%		MCM10544 T_A = −55 to +125°C, V_{EE} = −5.2 Vdc ± 5%		Unit	Conditions
		Min	Max	Min	Max		
Read Mode						ns	Measured from 50% of input to 50% of output. See Note 2.
Chip Select Access Time	t_{ACS}	2.0	10	2.0	10		
Chip Select Recovery Time	t_{RCS}	2.0	10	2.0	10		
Address Access Time	t_{AA}	7.0	26	7.0	26		
Write Mode						ns	t_{WSA} = 8.0 ns Measured at 50% of input to 50% of output. t_W = 25 ns.
Write Pulse Width	t_W	25	—	25	—		
Data Setup Time Prior to Write	t_{WSD}	2.0	—	2.0	—		
Data Hold Time After Write	t_{WHD}	2.0	—	2.0	—		
Address Setup Time Prior to Write	t_{WSA}	8.0	—	8.0	—		
Address Hold Time After Write	t_{WHA}	0.0	—	0.0	—		
Chip Select Setup Time Prior to Write	t_{WSCS}	2.0	—	2.0	—		
Chip Select Hold Time After Write	t_{WHCS}	2.0	—	2.0	—		
Write Disable Time	t_{WS}	2.5	10	2.5	10		
Write Recovery Time	t_{WR}	2.5	10	2.5	10		
Rise and Fall Time	t_r, t_f					ns	Measured between 20% and 80% points.
Address to Output		1.5	7.0	1.5	7.0		
$\overline{CS}$ or $\overline{WE}$ to Output		1.5	5.0	1.5	5.0		
Capacitance						pF	Measured with a pulse technique.
Input Capacitance	C_{in}	—	5.0	—	5.0		
Output Capacitance	C_{out}	—	8.0	—	8.0		

NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10144; 100 Ω, MCM10544. $C_L \leq$ 5.0 pF (including jig and stray capacitance). Delay should be derated 30 ps/pF for capacitive load up to 50 pF.
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

MCM10145/MCM10545

16 X 4-BIT REGISTER FILE (RAM)



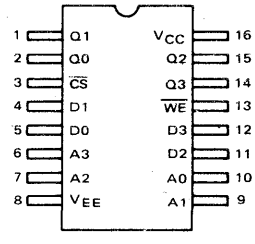
The MCM10145/10545 is a 16 word X 4-bit RAM. Bit selection is achieved by means of a 4-bit address A0 through A3.

The active-low chip select allows memory expansion up to 32 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM ($\overline{CS}$ input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_n is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at Q_n.

- Typical Address Access Time = 10 ns
- Typical Chip Select Access Time = 4.5 ns
- 50 kΩ Pulldown Resistors on All Inputs
- Power Dissipation (470 mW typ @ 25°C) Decreases with Increasing Temperature

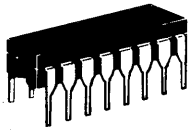
PIN ASSIGNMENT



TRUTH TABLE

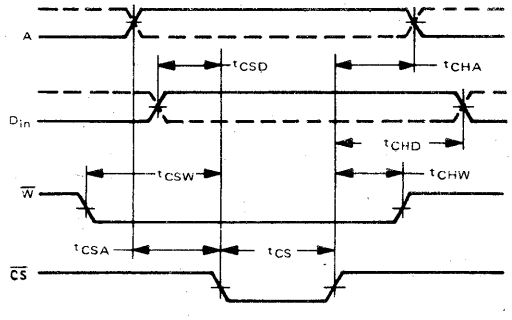
MODE	INPUT			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D_n	Q_n
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

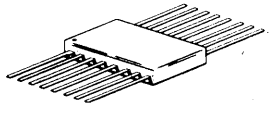
ϕ = Don't Care.



L SUFFIX
CERAMIC PACKAGE
CASE 620

FIGURE 1 – CHIP ENABLE STROBE MODE





F SUFFIX
CERAMIC PACKAGE
CASE 650

4

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	−55°C Min	−55°C Max	0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	I_{EE}	–	135	–	130	–	125	–	120	–	120	mAdc
Input Current High	I_{inH}	–	375	–	220	–	220	–	220	–	220	μAdc

-55°C and +125°C test values apply to MC105xx devices only.

SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10145 T_A = 0 to +75°C, V_{EE} = −5.2 Vdc ± 5% Min	MCM10145 Max	MCM10545 T_A = −55 to +125°C, V_{EE} = −5.2 Vdc ± 5% Min	MCM10545 Max	Unit	Conditions
Read Mode						ns	Measured from 50% of
Chip Select Access Time	t_{ACS}	2.0	8.0	2.0	10		input to 50% of output.
Chip Select Recovery Time	t_{RCS}	2.0	8.0	2.0	10		See Note 2.
Address Access Time	t_{AA}	4.0	15	4.0	18		
Write Mode						ns	t_{WSA} = 5 ns
Write Pulse Width	t_W	8.0	–	8.0	–		Measured at 50% of
Data Setup Time Prior to Write	t_{WSD}	0	–	0	–		input to 50% of output.
Data Hold Time After Write	t_{WHD}	3.0	–	4.0	–		t_W = 8 ns.
Address Setup Time Prior to Write	t_{WSA}	5.0	–	5.0	–		
Address Hold Time After Write	t_{WHA}	1.0	–	3.0	–		
Chip Select Setup Time Prior to Write	t_{WSCS}	0	–	5.0	–		
Chip Select Hold Time After Write	t_{WHCS}	0	–	0	–		
Write Disable Time	t_{WS}	2.0	8.0	2.0	10		
Write Recovery Time	t_{WR}	2.0	8.0	2.0	10		
Chip Enable Strobe Mode						ns	Guaranteed but not
Data Setup Prior to Chip Select	t_{CSD}	0	–	–	–		tested on standard
Write Enable Setup Prior to Chip Select	t_{CSW}	0	–	–	–		product. See Figure 1.
Address Setup Prior to Chip Select	t_{CSA}	0	–	–	–		
Data Hold Time After Chip Select	t_{CHD}	2.0	–	–	–		
Write Enable Hold Time After Chip Select	t_{CHW}	0	–	–	–		
Address Hold Time After Chip Select	t_{CHA}	4.0	–	–	–		
Chip Select Minimum Pulse Width	t_{CS}	18	–	–	–		
Rise and Fall Time	t_r, t_f					ns	Measured between 20%
Address to Output		1.5	7.0	1.5	7.0		and 80% points.
$\overline{CS}$ to Output		1.5	5.0	1.5	5.0		
Capacitance						pF	Measured with a pulse
Input Capacitance	C_{in}	–	6.0	–	6.0		technique.
Output Capacitance	C_{out}	–	8.0	–	8.0		

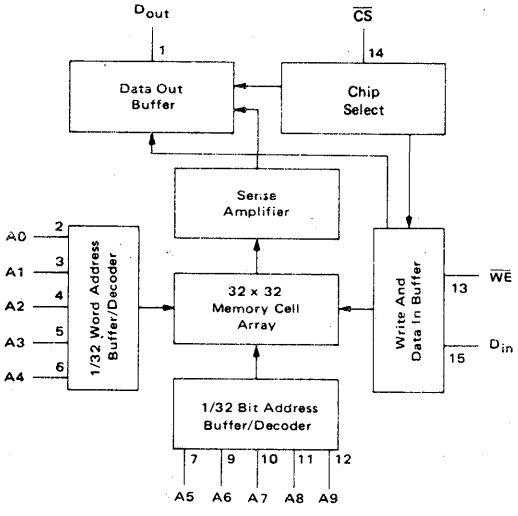
NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10145; 100 Ω, MCM10545. $C_L \leq$ 5.0 pF (including jig and Stray Capacitance). Delay should be derated 30 ps/pF for capacitive loads up to 50 pF.

2. The maximum Address Access Time is guaranteed to be the worst-case bit in the memory.

3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

MCM10146/MCM10546

1024 X 1-BIT RANDOM ACCESS MEMORY



The MCM10146/10546 is a 1024 X 1-bit RAM. Bit selection is achieved by means of a 10-bit address, A0 to A9.

The active-low chip select is provided for memory expansion up to 2048 words.

The operating mode of the RAM ($\overline{CS}$ input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low, the chip is in the write mode, the output, D_{out}, is low and the data state present at D_{in} is stored at the selected address. With $\overline{WE}$ high, the chip is in the read mode and the data stored at the selected memory location will be presented non-inverted at D_{out}. (See Truth Table.)

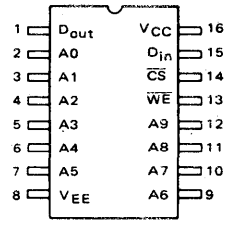
- Pin-for-Pin Compatible with the 10415
- Power Dissipation (520 mW typ @ 25°C) Decreases with Increasing Temperature
- Typical Address Access of 24 ns
- Typical Chip Select Access of 4.0 ns
- 50 kΩ Pulldown Resistor on Chip Select Input

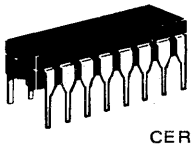
TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

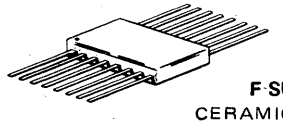
ϕ = Don't Care.

PIN ASSIGNMENT





L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650-03

4

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	−55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	–	155	–	150	–	145	–	125	–	125	mAdc
Input Current High	I_{inH}	–	375	–	220	–	220	–	220	–	220	μAdc
Logic "0" Output Voltage	V_{OL}	-1.970	-1.655	-1.920	-1.665	-1.900	-1.650	-1.880	-1.625	-1.870	-1.545	Vdc

NOTE: −55°C and +125°C test values apply to MCM105XX only.

SWITCHING CHARACTERISTICS (Note 1)

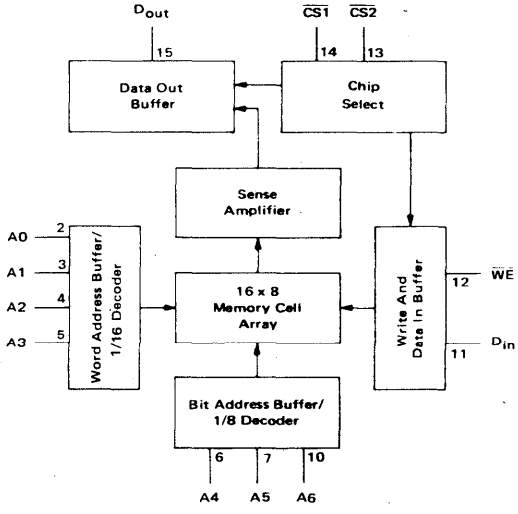
Characteristics	Symbol	MCM10146 T_A = 0 to +75°C, V_{EE} = −5.2 Vdc ± 5%		MCM10546 T_A = −55 to +125°C, V_{EE} = −5.2 Vdc ± 5%		Unit	Conditions
		Min	Max	Min	Max		
Read Mode						ns	Measured at 50% of input
Chip Select Access Time	t_{ACS}	2.0	7.0	2.0	8.0		to 50% of output.
Chip Select Recovery Time	t_{RCS}	2.0	7.0	2.0	8.0		See Note 2.
Address Access Time	t_{AA}	8.0	29	8.0	40		
Write Mode						ns	t_{WSA} = 8.0 ns.
Write Pulse Width (To guarantee writing)	t_W	25	–	25	–		Measured at 50% of input to 50% of output.
Data Setup Time Prior to Write	t_{WSD}	5.0	–	5.0	–		t_W = 25 ns
Data Hold Time After Write	t_{WHD}	5.0	–	5.0	–		
Address Setup Time Prior to Write	t_{WSA}	8.0	–	10	–		
Address Hold Time After Write	t_{WHA}	2.0	–	8.0	–		
Chip Select Setup Time Prior to Write	t_{WSCS}	5.0	–	5.0	–		
Chip Select Hold Time After Write	t_{WHCS}	5.0	–	5.0	–		
Write Disable Time	t_{WS}	2.8	7.0	2.8	12		
Write Recovery Time	t_{WR}	2.8	7.0	2.8	12		
Rise and Fall Time	t_r, t_f					ns	Measured between 20% and
$\overline{CS}$ or $\overline{WE}$ to Output		1.5	4.0	1.5	4.0		80% points.
Address to Output		1.5	8.0	1.5	8.0		
Capacitance						pF	Measured with a pulse
Input Capacitance	C_{in}	–	5.0	–	5.0		technique.
Output Capacitance	C_{out}	–	8.0	–	8.0		

NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10146; 100 Ω, MCM10546. $C_L \leq$ 5.0 pf including jig and stray capacitance. For Capacitance Loading ≤ 50 pF, delay should be derated by 30 ps/pF.
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

4

MCM10147/MCM10547

128 X 1-BIT RANDOM ACCESS MEMORY



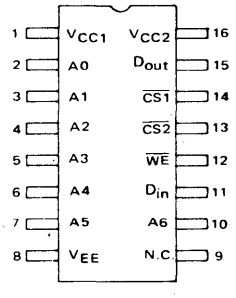
The MCM1047/10547 is a fast 128-word X 1-bit RAM. Bit selection is achieved by means of a 7-bit address, A0 through A6.

The active-low chip selects and fast chip select access time allow easy memory expansion up to 512 words without affecting system performance.

The operating mode ($\overline{CS}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_{in} is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at D_{out}.

- Typical Address Access Time of 10 ns
- Typical Chip Select Access Time of 4.0 ns
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation (420 mW typ @ 25°C) Decreases with Increasing Temperature
- Similar to F10405

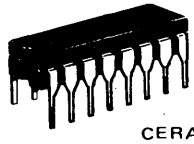
PIN ASSIGNMENT



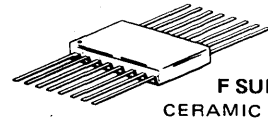
TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$*	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

*$\overline{CS} = \overline{CS1} + \overline{CS2}$ ϕ = Don't Care.



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

4

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	−55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	–	115	–	105	–	100	–	95	–	95	mAdc
Input Current High	I_{inH}	–	375	–	220	–	220	–	220	–	220	μAdc

-55°C and +125°C test values apply to MC105xx devices only.

SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10147 T_A = 0 to +75°C, V_{EE} = −5.2 Vdc ±5%		MCM10547 T_A = −55 to +125°C, V_{EE} = −5.2 Vdc ±5%		Unit	Conditions
		Min	Max	Min	Max		
Read Mode						ns	Measured from 50% of input to 50% of output. See Note 2.
Chip Select Access Time	t_{ACS}	2.0	8.0	*	*		
Chip Select Recovery Time	t_{RCS}	2.0	8.0	*	*		
Address Access Time	t_{AA}	5.0	15	*	*		
Write Mode						ns	t_{WSA} = 4.0 ns Measured at 50% of input to 50% of output. t_W = 8.0 ns.
Write Pulse Width	t_W	8.0	–	*	–		
Data Setup Time Prior to Write	t_{WSD}	1.0	–	*	–		
Data Hold Time After Write	t_{WHD}	3.0	–	*	–		
Address Setup Time Prior to Write	t_{WSA}	4.0	–	*	–		
Address Hold Time After Write	t_{WHA}	3.0	–	*	–		
Chip Select Setup Time Prior to Write	t_{WSCS}	1.0	–	*	–		
Chip Select Hold Time After Write	t_{WHCS}	1.0	–	*	–		
Write Disable Time	t_{WS}	2.0	8.0	*	*		
Write Recovery Time	t_{WR}	2.0	8.0	*	*		
Rise and Fall Time	t_r, t_f	1.5	5.0	*	*	ns	Measured between 20% and 80% points.
Capacitance						pF	Measured with a pulse technique.
Input Capacitance	C_{in}	–	5.0	–	*		
Output Capacitance	C_{out}	–	8.0	–	*		

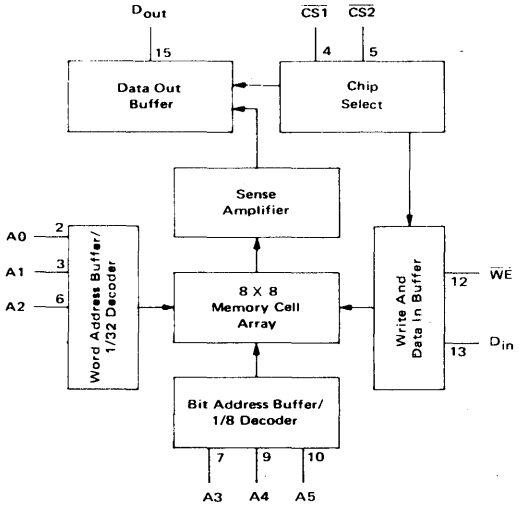
NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10147; 100 Ω, MCM10547.
$C_L \leq 5.0$ pF (including jig and stray capacitance).
Delay should be derated 30 ps/pF for capacitive load up to 50 pF.
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

*To be determined; contact your Motorola representative for up-to-date information.

MOTOROLA

MCM10148/MCM10548

64 X 1-BIT RANDOM ACCESS MEMORY



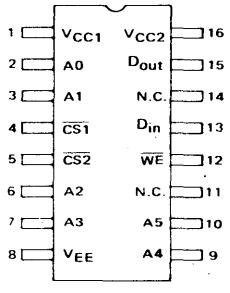
The MCM10148/10548 is a fast 64-word X 1-bit RAM. Bit selection is achieved by means of a 6-bit address, A0 through A5.

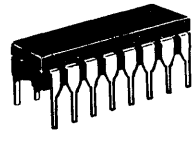
The active-low chip selects and fast chip select access time allow easy memory expansion up to 256 words without affecting system performance.

The operating mode ($\overline{CS}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_{in} is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at D_{out}.

- Typical Address Access Time of 10 ns
- Typical Chip Select Access Time of 4.0 ns
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation (420 mW typ @ 25°C) Decreases with Increasing Temperature

PIN ASSIGNMENT



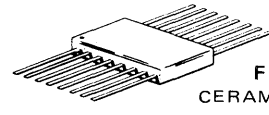


L SUFFIX
CERAMIC PACKAGE
CASE 620

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$*	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

*$\overline{CS} = \overline{CS1} + \overline{CS2} + \overline{CS3}$ ϕ = Don't Care.



F SUFFIX
CERAMIC PACKAGE
CASE 650

4

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	−55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	–	115	–	105	–	100	–	95	–	95	mAdc
Input Current High	I_{inH}	–	375	–	220	–	220	–	220	–	220	μAdc

−55°C and +125°C test values apply to MC105xx devices only.

SWITCHING CHARACTERISTICS (Note 1)

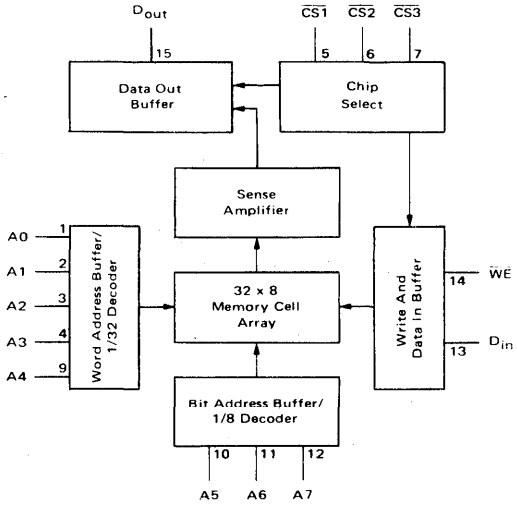
Characteristics	Symbol	MCM10148 T_A = 0 to +75°C, V_{EE} = −5.2 Vdc ±5%		MCM10548 T_A = −55 to +125°C, V_{EE} = −5.2 Vdc ±5%		Unit	Conditions
		Min	Max	Min	Max		
Read Mode						ns	Measured from 50% of input to 50% of output. See Note 2.
Chip Select Access Time	t_{ACS}	–	7.5	–	*		
Chip Select Recovery Time	t_{RCS}	–	7.5	–	*		
Address Access Time	t_{AA}	–	15	–	*		
Write Mode						ns	t_{WSA} = 5.0 ns Measured at 50% of input to 50% of output. t_W = 8.0 ns.
Write Pulse Width	t_W	8.0	–	*	–		
Data Setup Time Prior to Write	t_{WSD}	3.0	–	*	–		
Data Hold Time After Write	t_{WHD}	2.0	–	*	–		
Address Setup Time Prior to Write	t_{WSA}	5.0	–	*	–		
Address Hold Time After Write	t_{WHA}	3.0	–	*	–		
Chip Select Setup Time Prior to Write	t_{WSCS}	3.0	–	*	–		
Chip Select Hold Time After Write	t_{WHCS}	0	–	*	–		
Write Disable Time	t_{WS}	2.0	7.5	*	*		
Write Recovery Time	t_{WR}	2.0	7.5	*	*		
Rise and Fall Time	t_r, t_f	1.5	5.0	*	*	ns	Measured between 20% and 80% points.
Capacitance						pF	Measured with a pulse technique.
Input Capacitance	C_{in}	–	5.0	–	*		
Output Capacitance	C_{out}	–	8.0	–	*		

NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10148; 100 Ω, MCM10548.
$C_L \leq 5.0$ pF (including jig and stray capacitance)
Delay should be derated 30 ps/pF for capacitive load up to 50 pF.
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

*To be determined; contact your Motorola representative for up-to-date information.

MCM10152/MCM10552

256 X 1-BIT RANDOM ACCESS MEMORY



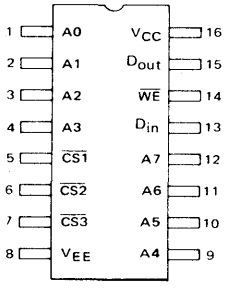
The MCM10152/10552 is a 256-word X 1-bit RAM. Bit selection is achieved by means of an 8-bit address A0 through A7.

The active-low chip select allows memory expansion up to 2048 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM ($\overline{CS}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_{in} is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at D_{out}.

- Typical Address Access Time = 11 ns
- Typical Chip Select Access Time = 4.0 ns
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation (570 mW typ @ 25°C) Decreases with Increasing Temperature
- Pin-for-Pin Compatible with F10410/10414

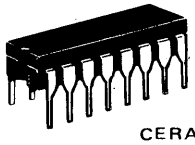
PIN ASSIGNMENT



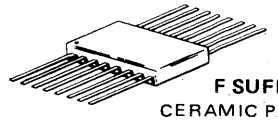
TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$*	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

*$\overline{CS} = \overline{CS1} + \overline{CS2} + \overline{CS3}$ ϕ = Don't Care.



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

4

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	–	140	–	135	–	130	–	125	–	125	mAdc
Input Current High	I_{inH}	–	375	–	220	–	220	–	220	–	220	μAdc

-55°C and +125°C test values apply to MC105xx devices only.

SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10152 T_A = 0 to +75°C, V_{EE} = -5.2 Vdc ±5%		MCM10552 T_A = -55 to +125°C, V_{EE} = -5.2 Vdc ±5%		Unit	Conditions
		Min	Max	Min	Max		
Read Mode							Measured from 50% of
Chip Select Access Time	t_{ACS}	2.0	7.5	*	*		input to 50% of output.
Chip Select Recovery Time	t_{RCS}	2.0	7.5	*	*		See Note 2.
Address Access Time	t_{AA}	7.0	15	*	*		
Write Mode						ns	t_{WSA} = 5.0 ns
Write Pulse Width	t_W	10	–	*	–		Measured at 50% of input
Data Setup Time Prior to Write	t_{WSD}	2.0	–	*	–		to 50% of output.
Data Hold Time After Write	t_{WHD}	2.0	–	*	–		t_W = 10 ns.
Address Setup Time Prior to Write	t_{WSA}	5.0	–	*	–		
Address Hold Time After Write	t_{WHA}	3.0	–	*	–		
Chip Select Setup Time Prior to Write	t_{WSCS}	2.0	–	*	–		
Chip Select Hold Time After Write	t_{WHCS}	2.0	–	*	–		
Write Disable Time	t_{WS}	2.5	7.5	*	*		
Write Recovery Time	t_{WR}	2.5	7.5	*	*		
Rise and Fall Time	t_r, t_f	1.5	5.0	*	*	ns	Measured between 20% and 80% points.
Capacitance						pF	Measured with a pulse
Input Capacitance	C_{in}	–	5.0	–	*		technique.
Output Capacitance	C_{out}	–	8.0	–	*		

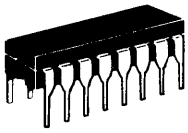
NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10152; 100 Ω, MCM10552.
$C_L \leq$ 5.0 pF (including jig and stray capacitance).
Delay should be derated 30 ps/pF for capacitive load up to 50 pF.
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

*To be determined; contact your Motorola representative for up-to-date information.

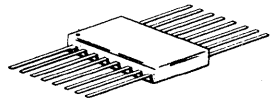
4

MCM10139/MCM10539

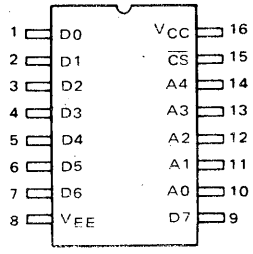
32 x 8-BIT PROGRAMMABLE READ-ONLY MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 620



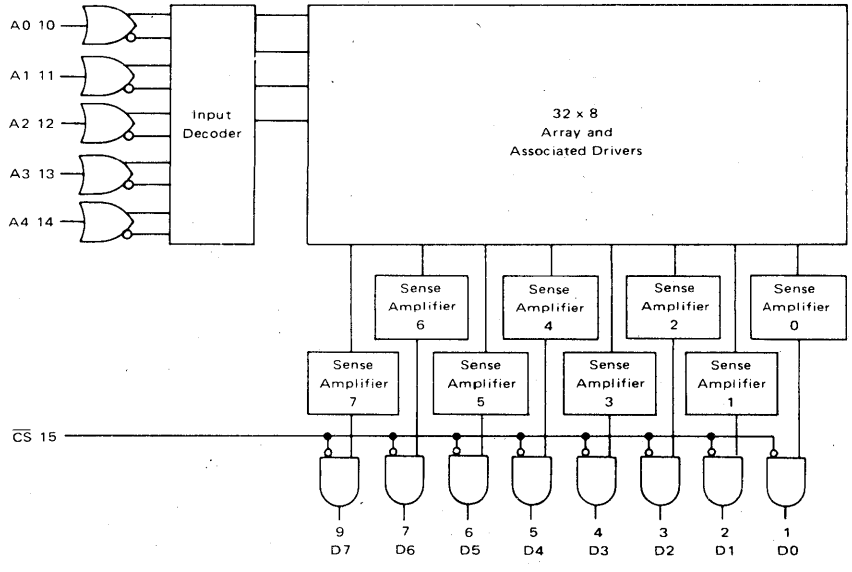
F SUFFIX
CERAMIC PACKAGE
CASE 650



The MCM10139/10539 is a 256-bit field programmable read only memory (PROM). Prior to programming, all stored bits are at logic 0 (low) levels. The logic state of each bit can then be changed by on-chip programming circuitry. The memory has a single negative logic chip enable. When the chip is disabled ($\overline{CS}$ = high), all outputs are forced to a logic 0 (low).

- Typical Address Access Time = 15 ns
- Typical Chip Select Access Time = 10 ns
- 50 kΩ Input Pulldown Resistors on all inputs
- Power Dissipation (520 mW typ @ 25°C) Decreases with Increasing Temperature

BLOCK DIAGRAM



4

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	−55°C		−0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	–	160	–	150	–	145	–	140	–	160	mAdc
Input Current High	I_{inH}	–	450	–	265	–	265	–	265	–	265	μAdc
Logic "0" Output Voltage	V_{OL}											Vdc
MCM10139		–	–	-2.010	-1.665	-1.990	-1.650	-1.970	-1.625	–	–	
MCM10539		-2.060	-1.655	–	–	-1.990	-1.620	–	–	-1.960	-1.545	

SWITCHING CHARACTERISTICS (Note 1)

Characteristic	Symbol	MCM10139 (V_{EE} = −5.2 Vdc ±5%; T_A = 0°C to +75°C)	MCM10539 (V_{EE} = −5.2 Vdc ± 5 %; T_A = −55°C to +125°C)	Conditions
Chip Select Access Time	t_{ACS}	15 ns Max	*	Measured from 50% of input to 50% of output. See Note 2
Chip Select Recovery Time	t_{RCS}	15 ns Max	*	
Address Access Time	t_{AA}	20 ns Max	*	
Rise and Fall Time	t_r, t_f	3.0 ns Typ	*	Measured between 20% and 80% points.
Input Capacitance	C_{in}	5.0 pF Max	*	Measured with a pulse technique.
Output Capacitance	C_{out}	8.0 pF Max	*	

NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10139; 100 Ω, MCM10539. $C_L \leq$ 5.0 pF including jig and stray capacitance. For Capacitance Loading ≤ 50 pF, delay should be derated by 30 ps/pF.
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

*To be determined; contact your Motorola representative for up-to-date information.

FIGURE 1 – MANUAL PROGRAMMING CIRCUIT

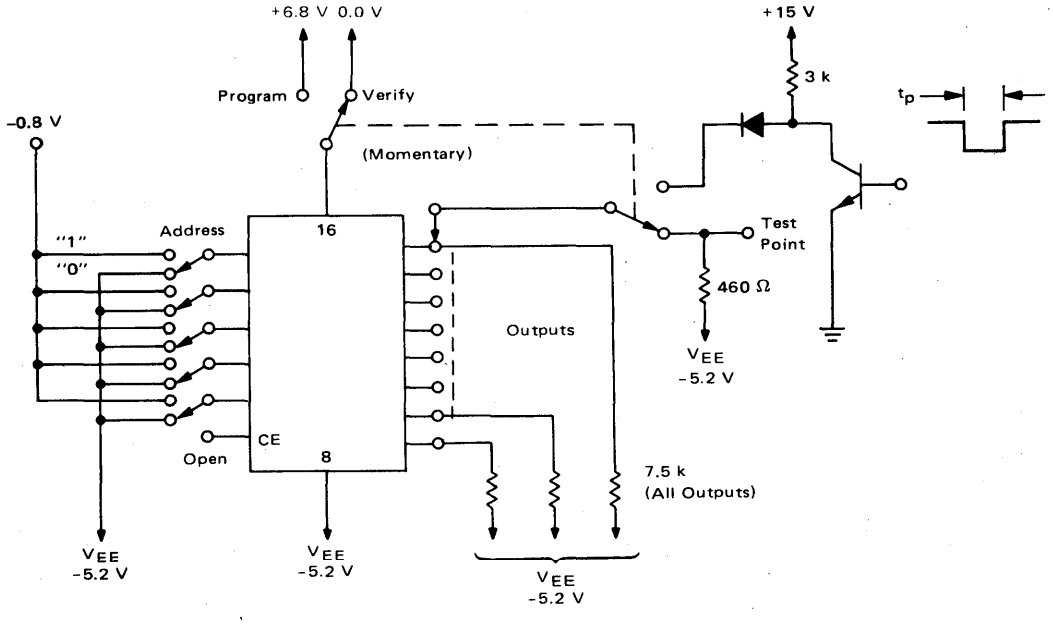
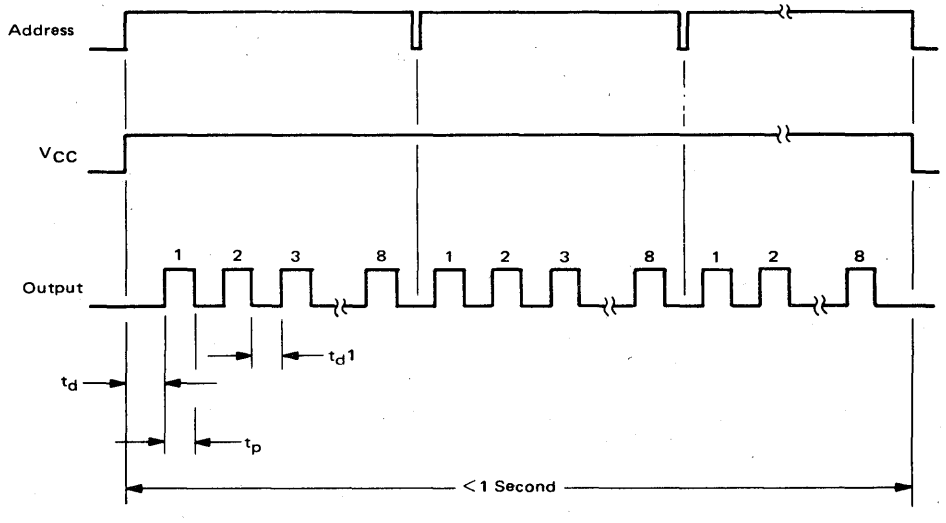


FIGURE 2 – AUTOMATIC PROGRAMMING CIRCUIT



RECOMMENDED PROGRAMMING PROCEDURE*

The MCM10139 is shipped with all bits at logical "0" (low). To write logical "1s", proceed as follows.

MANUAL (See Figure 1)

Step 1 Connect V_{EE} (Pin 8) to -5.2 V and V_{CC} (Pin 16) to 0.0 V. Address the word to be programmed by applying -1.2 to -0.6 volts for a logic "1" and -5.2 to -4.2 volts for a logic "0" to the appropriate address inputs.

Step 2 Raise V_{CC} (Pin 16) to +6.8 volts.

Step 3 After V_{CC} has stabilized at +6.8 volts (including any ringing which may be present on the V_{CC} line), apply a current pulse of 2.5 mA to the output pin corresponding to the bit to be programmed to a logic "1".

Step 4 Return V_{CC} to 0.0 Volts.

CAUTION

To prevent excessive chip temperature rise, V_{CC} should not be allowed to remain at +6.8 volts for more than 1 second.

Step 5 Verify that the selected bit has programmed by connecting a 460 Ω resistor to -5.2 volts and measuring the voltage at the output pin. If a logic "1" is not detected at the output, the procedure should be repeated once. During verification V_{IH} should be -1.0 to -0.6 volts.

Step 6 If verification is positive, proceed to the next bit to be programmed.

AUTOMATIC (See Figure 2)

Step 1 Connect V_{EE} (Pin 8) to -5.2 volts and V_{CC} (Pin 16) to 0.0 volts. Apply the proper address data and raise V_{CC} (Pin 16) to +6.8 volts.

Step 2 After a minimum delay of 100 μs and a maximum delay of 1.0 ms, apply a 2.5 mA current pulse to the first bit to be programmed ($0.1 \leq PW \leq 1$ ms).

Step 3 Repeat Step 2 for each bit of the selected word specified as a logic "1". (Program only one bit at a time. The delay between output programming pulses should be equal to or less than 1.0 ms.)

Step 4 After all the desired bits of the selected word have been programmed, change address data and repeat Steps 2 and 3.

NOTE: If all the maximum times listed above are maintained, the entire memory will program in less than 1 second. Therefore, it would be permissible for V_{CC} to remain at +6.8 volts during the entire programming time.

Step 5 After stepping through all address words, return V_{CC} to 0.0 volts and verify that each bit has programmed. If one or more bits have not programmed, repeat the entire procedure once. During verification V_{IH} should be -1.0 to -0.6 volts.

*NOTE: For devices that program incorrectly—return serialized units with individual truth tables. Noncompliance voids warranty.

4

PROGRAMMING SPECIFICATIONS

Characteristic	Symbol	Limits			Units	Conditions
		Min	Typ	Max		
Power Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	Vdc	
To Program	V_{CCP}	+6.04	+6.8	+7.56	Vdc	
To Verify	V_{CCV}	0	0	0	Vdc	
Programming Supply Current	I_{CCP}	–	200	600	mA	V_{CC} = +6.8 Vdc
Address Voltage	V_{IH} Program	-1.2	–	-0.6	Vdc	
Logical "1"	V_{IH} Verify	-1.0	–	-0.6	Vdc	
Logical "0"	V_{IL}	-5.2	–	-4.2	Vdc	
Maximum Time at $V_{CC} = V_{CCP}$	–	–	–	1.0	sec	
Output Programming Current	I_{OP}	2.0	2.5	3.0	mAdc	
Output Program Pulse Width	t_p	0.5	–	1.0	ms	
Output Pulse Rise Time	–	–	–	10	μs	
Programming Pulse Delay (1)						
Following V_{CC} change	t_d	0.1	–	1.0	ms	
Between Output Pulses	t_{d1}	0.01	–	1.0	ms	

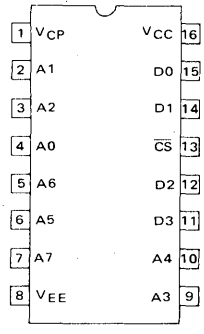
NOTE 1. Maximum is specified to minimize the amount of time V_{CC} is at +6.8 volts.

MOTOROLA

MCM10149/MCM10549

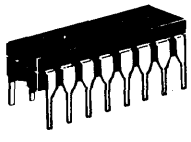
256 X 4-BIT PROGRAMMABLE READ-ONLY MEMORY

PIN ASSIGNMENT

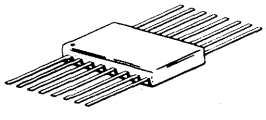


The MCM10149/10549 is a 256-word X 4-bit field programmable read only memory (PROM). Prior to programming, all stored bits are at logic 1 (high) levels. The logic state of each bit can then be changed by on-chip programming circuitry. The memory has a single negative logic chip enable. When the chip is disabled ($\overline{CS}$ = high), all outputs are forced to a logic 0 (low).

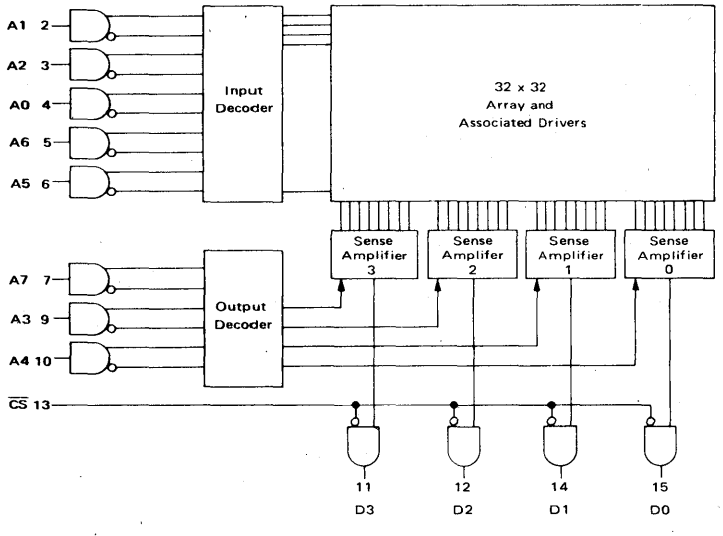
- Typical Address Access Time of 20 ns
- Typical Chip Select Access Time of 8.0 ns
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation (540 mW typ @ 25°C) Decreases with Increasing Temperature



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650



4

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	−55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	–	140	–	135	–	130	–	125	–	125	mAdc
Input Current High	I_{inH}	–	450	–	265	–	265	–	265	–	265	μAdc

-55°C and +125°C test values apply to MC105xx devices only.

SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10149 T_A = 0 to +75°C, V_{EE} = −5.2 Vdc ±5%		MCM10549 T_A = −55 to +125°C, V_{EE} = −5.2 Vdc ±5%		Unit	Conditions
		Min	Max	Min	Max		
Read Mode						ns	Measured from 50% of input to 50% of output. See Note 1.
Chip Select Access Time	t_{ACS}	2.0	10	*	*		
Chip Select Recovery Time	t_{RCS}	2.0	10	*	*		
Address Access Time	t_{AA}	7.0	25	*	*		
Rise and Fall Time	t_r, t_f	1.5	7.0	*	*	ns	Measured between 20% and 80% points.
Capacitance						pF	Measured with a pulse technique.
Input Capacitance	C_{in}	–	5.0	–	5.0		
Output Capacitance	C_{out}	–	8.0	–	8.0		

NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10149; 100 Ω, MCM10549.
$C_L \leq 5.0$ pF (including jig and stray capacitance)
Delay should be derated 30 ps/pF for capacitive load up to 50 pF
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.
4. $V_{CP} = V_{CC}$ = Gnd for normal operation.

*To be determined; contact your Motorola representative for up-to-date information.

PROGRAMMING THE MCM10149 †

During programming of the MCM10149, input pins 7, 9, and 10 are addressed with standard MECL 10K logic levels. However, during programming input pins 2, 3, 4, 5, and 6 are addressed with 0 V $\leq V_{IH} \leq$ + 0.25 V and $V_{EE} \leq V_{IL} \leq$ −3.0 V. It should be stressed that this deviation from standard input levels is required only during the programming mode. During normal operation, standard MECL 10,000 input levels must be used.

With these requirements met, and with $V_{CP} = V_{CC}$ = 0 V and V_{EE} = − 5.2 V ± 5%, the address is set up. After a minimum of 100 ns delay, V_{CP} (pin 1) is ramped up to +12 V ± 0.5 V (total voltage V_{CP} to V_{EE} is now 17.2 V, +12 V − [−5.2 V]). The rise time of this V_{CP} voltage pulse should be in the 1-10 μs range, while its pulse width (t_{w1}) should be greater than 100 μs but less than 1 ms. The V_{CP} supply current at +12 V will be approximately 525 mA while current drain from V_{CC} will be approximately 175 mA. A current limit should therefore be set on both of these supplies. The current limit on the V_{CP} supply should be set at 700 mA while the V_{CC} supply should be limited to 250 mA. It should be noted that the V_{EE} supply must be capable of sinking the combined current of the V_{CC} and V_{CP} supplies while maintaining a voltage of −5.2 V ± 5%.

Coincident with, or at some delay after the V_{CP} pulse has reached its 100% level, the desired bit to be fused can be selected. This is done by taking the corresonding output pin to a voltage of +2.85 V ±5%. It is to be noted that only one bit is to be fused at a time. The other three unselected outputs should remain terminated through their 50 ohm load resistor (100 ohm for MCM10549) to −2.0 V. Current into the selected output is 5 mA maximum.

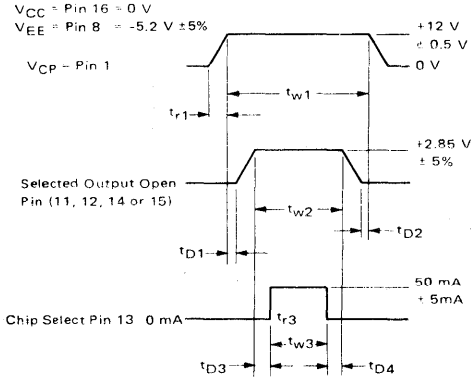
After the bit select pulse has been applied to the appropriate output, the fusing current is sourced out of the chip select pin 13. The 0% to 100% rise time of this current pulse should be 250 ns max. Its pulse width should be greater than 100 μs. Pulse magnitude is 50 mA ±5.0 mA. The voltage clamp on this current source is to be −6.0 V.

After the fusing current source has returned 0 mA, the bit select pulse is returned to it initial level, i.e., the output is returned through its load to −2.0 V. Thereafter, V_{CP} is returned to 0 V. Strobing of the outputs to determine success in programming should occur no sooner than 100 ns after V_{CP} has returned to 0 V. The remaining bits are programmed in a similar fashion.

† NOTE: For devices that program incorrectly, return serialized units with individual truth tables. Non compliance voids warranty.

PROGRAMMING SPECIFICATIONS

The following timing diagrams and fusing information represent programming specifications for the MCM10149.



The timing diagram is shown for programming one bit. Note that only one bit is blown at a time. All addressing must be done 100 ns prior to the beginning of the V_{CP} pulse, i.e., V_{CP} = 0 V. Likewise, strobing of the outputs to determine success in programming should occur no sooner than 100 ns after V_{CP} returns to 0 V.

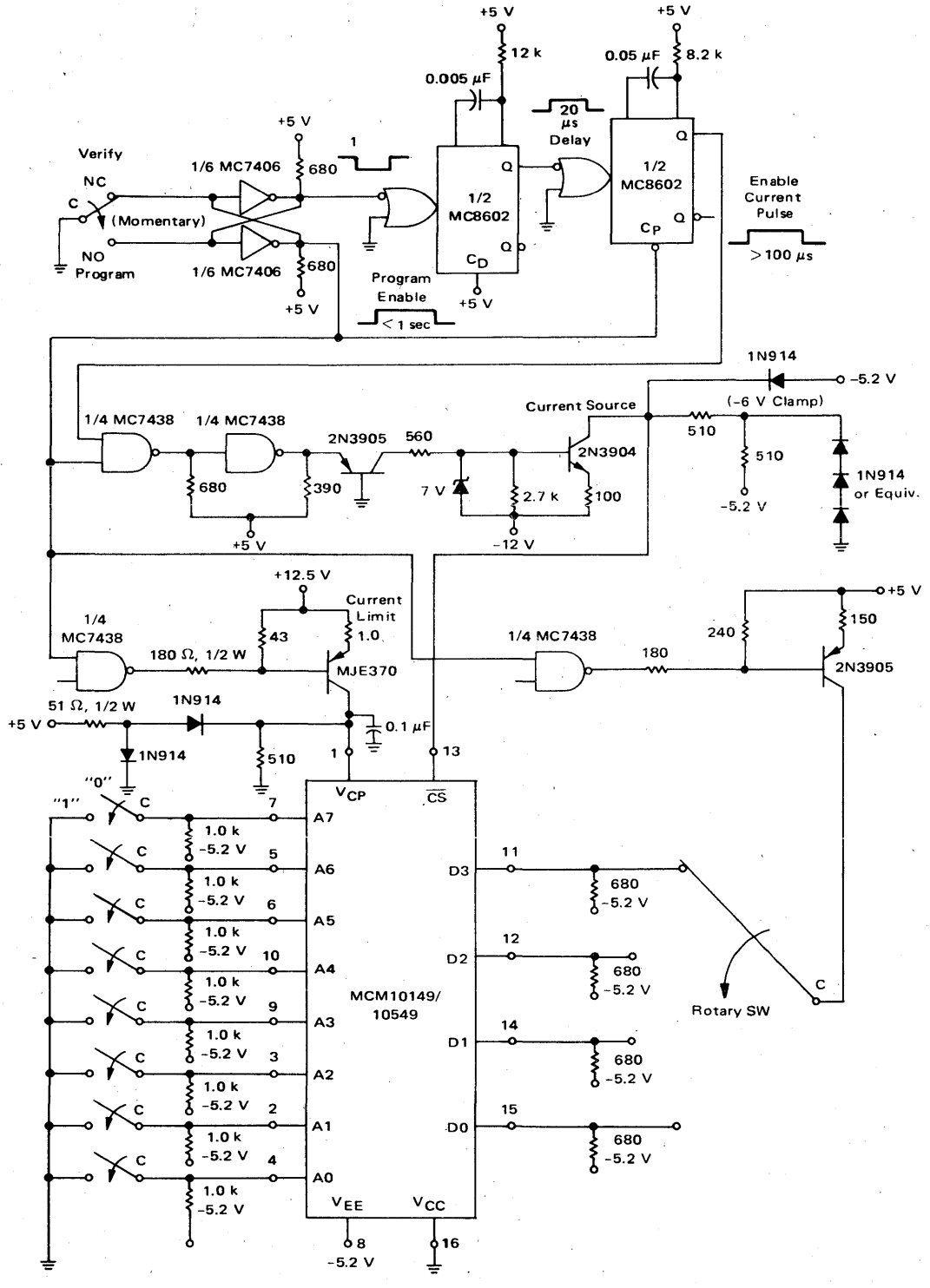
Note that the fusing current is defined as a positive current out of the chip select, pin 13. A programming duty cycle of ⩽ 15% is to be observed.

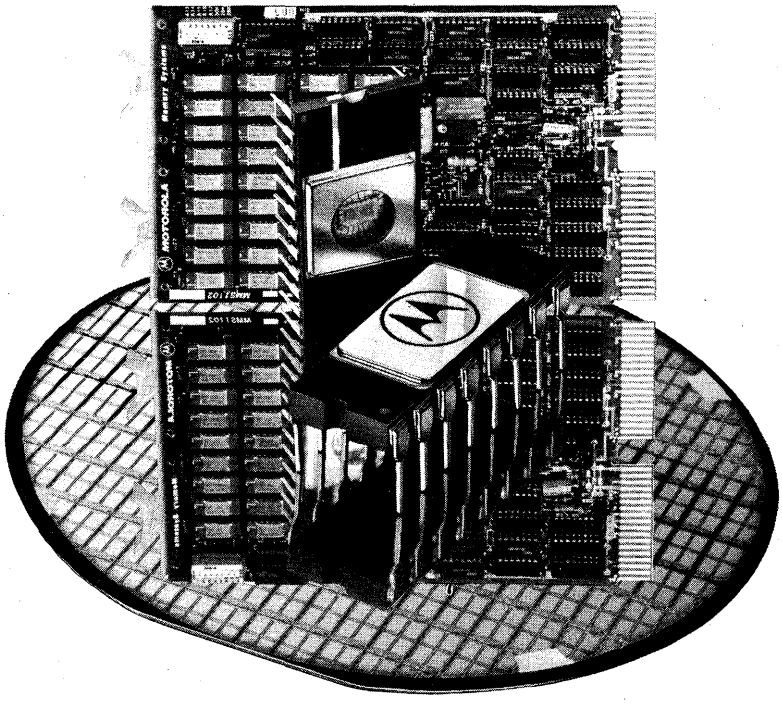
Definitions and values of timing symbols are as follows.

Symbol	Definition	Value
t_{r1}	Rise Time, Programming Voltage	⩾ 1 μs
t_{w1}	Pulse Width, Programming Voltage	⩾ 100 μs < 1 ms
t_{D1}	Delay Time, Programming Voltage Pulse to Bit Select Pulse	⩾ 0
t_{w2}	Pulse Width, Bit Select	⩾ 100 μs
t_{D2}	Delay Time, Bit Select Pulse to Programming Voltage Pulse	⩾ 0
t_{D3}	Delay Time, Bit Select Pulse to Programming Current Pulse	⩾ 1 μs
t_{r3}	Rise Time, Programming Current Pulse	250 ns max
t_{w3}	Pulse Width, Programming Current Pulse	⩾ 100 μs
t_{D4}	Delay Time, Programming Current Pulse to Bit Select Pulse	⩾ 1 μs

4

MANUAL PROGRAMMING CIRCUIT





Memory Boards 5

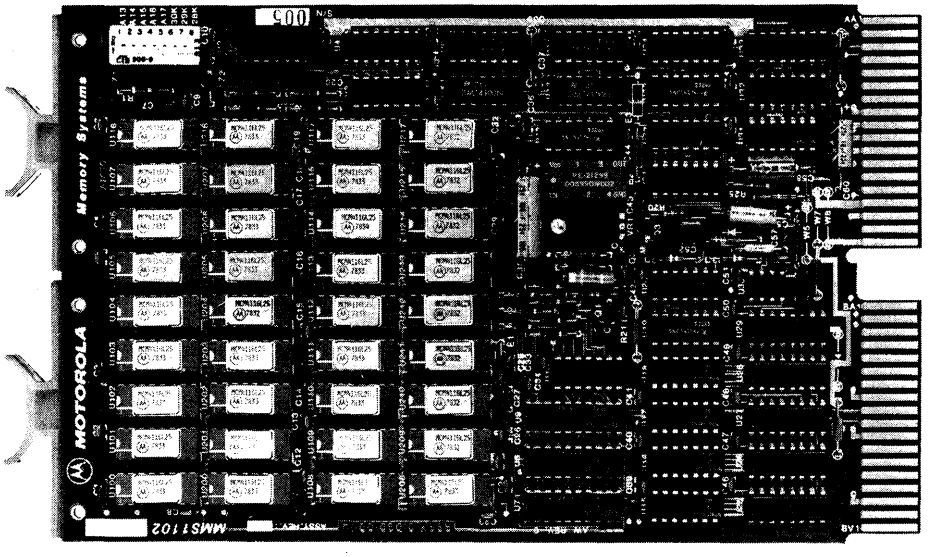
MOTOROLA

MMS1102

Advance Information

ADD-ON MEMORY CARD FOR THE LSI-11 FAMILY

The MMS1102 is a dual height (5.187" × 8.94") add-on memory card for the LSI-11 family of computers. It is compatible with the LSI-11/2 and LSI-11 processors as well as the PDP 11V03 computer systems. It incorporates byte parity storage as well as generation and detection logic.



Specification Highlights

INTERFACE	LSI-11, "Q" Bus-Plus.
CAPACITY	8K words × 16 bits, 16K words × 16 bits, 32K words × 16 bits.
PARITY	Optional on-board storage, generation and detection logic for both upper and lower byte. Parity option does not degrade access times.
SPEED	The MMS1102-3X has a read access time under 300 ns. Read access time is defined here as the time from receipt of SYNC H to the transmission of RPLY H, assuming that the SYNC H to DIN H time is no greater than 160 ns.
ADDRESSING	Switch-selectable, to start on any 4K word boundary between 0 and 128K.
I/O PAGE USE	Three switches allow any one of the lowest three kilowords of the I/O page to be used as Read/Write memory.
BATTERY BACKUP	Jumper selectable; allows the MMS1102 to be operated from a separate uninterrupted power source (+5 BBU and +12 BBU).
REFRESH	Implemented internal to the MMS1102 and totally transparent to the system.

This is advance information and specifications are subject to change without notice.

5

MMS1102-XX ORDERING INFORMATION

Storage Capacity	Part Number (With Parity and Controller)	Part Number (No Parity)
16 Kilobytes	MMS1102-31PC	MMS1102-31
32 Kilobytes	MMS1102-32PC	MMS1102-32
64 Kilobytes	MMS1102-34PC	MMS1102-34

MMS1102-3X — AC OPERATING CHARACTERISTICS

	Read Access (ns)		Write Access (ns)	
	Typical	Worst Case	Typical	Worst Case
Access Time*	250	300	125	175
Cycle Time**	470	500	350	400
Refresh Latency***	175	400	175	400

*As measured from receipt of RSYNC H to transmission of TRPLY H.
**This is the reciprocal of the maximum continuous transfer rate, assuming no refresh interference.
***Occurs approximately once every 16 microseconds.

MMS1102 POWER REQUIREMENTS

Nominal Voltage	Min	Max	Current Requirements (mA)				Input Pins
			Standby		Active		
			Typical	Worst Case	Typical	Worst Case	
+5 VDC (Total)	4.75	5.25	725 925*	800 1000*	775 1000*	850 1100*	AA2, BA2
+12 VDC	11.40	12.60	100	150	250	400	AD2, BD2
+5 VDC (BBU)	4.75	5.25	400	500	450	550	AV1**
+12 VDC (BBU)	11.40	12.60	100	150	250	400	AS1***

*Parity version only.
**In systems without battery backup this voltage is obtained from the regular +5 V rail via an on-board jumper.
***The +12 V supply requirement can be met via an on-board jumper from the regular +12 V rail.

MMS1102 BACKPLANE CONNECTOR PIN ASSIGNMENT

Row	A		B	
Side	1	2	1	2
Pin				
A	—	+5 V	BDCOK H	+5 V
B	—	—	—	—
C	BAD16 L**	GND	—	GND
D	BAD17 L	+12 V	—	+12 V
E	—	BDOUT L	—	BDAL 2 L
F	—	BRPLY L	—	BDAL 3 L
H	—	BDIN L	—	BDAL 4 L
J	GND	BSYNC L	GND	BDAL 5 L
K	} *	BWTBT L	} *	BDAL 6 L
L	}	—	}	BDAL 7 L
M	GND	BIAKI L } ***	GND	BDAL 8 L
N	—	BIAKO L }	—	BDAL 9 L
P	—	BBS7 L	—	BDAL 10 L
R	BREF L	BDMGI L } ***	—	BDAL 11 L
S	+12 V BBU	BDMGO L }	—	BDAL 12 L
T	GND	—	GND	BDAL 13 L
U	—	BDAL 0 L	—	BDAL 14 L
V	+5 V BBU	BDAL 1 L	+5 V	BDAL 15 L

*Must be hardwired on backplane or damage to MOS devices may result.
**Or PRTYER or PRTYCK.
***Hardwired on MMS1102.

5

MOTOROLA

MMS1110

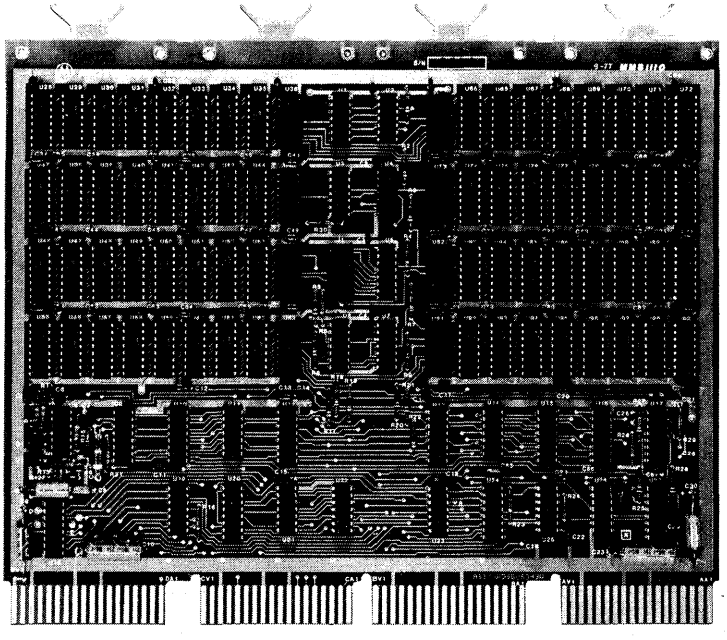
Advance Information

16K x 16
LSI-11 ADD-IN SEMICONDUCTOR MEMORY

The Motorola MMS1110 is a 16K-word x 16-bit plug-in main memory system designed for use with DEC's LSI-11 microcomputer system. The MMS1110 mounts directly into a H9270 backplane slot and is both hardware and software compatible with the LSI-11 system.

The memory module employs the MCM6604 4K Dynamic RAM components, mounted on a single PC board that contains timing, control and bus interface logic. Memory refreshing is controlled by the LSI-11.

Address select changes are possible with jumpers to provide up to 28K of main memory. A parity option, which generates, stores, and checks parity on the MMS1110, is available for custom LSI-11 systems.



MMS1110 FEATURES

- High Density
- Low Cost
- Fast Access and Cycle Times
- High Reliability
- Byte Operation
- Modular Expandability (Address Select Jumpers)
- Options Available

MMS1110-1	12K x 16
MMS1110-2	8K x 16
MMS1110P	16K x 18 (parity)
MMS1110-3	4K x 16

5

This is advance information and specifications are subject to change without notice.

SPECIFICATIONS

CAPACITY

16K words per board

WORD LENGTH

16 bits

PERFORMANCE

Access Time	450 ns max
Read Cycle Time	800 ns min
Write Cycle Time	800 ns min
Read-Modify-Write Cycle Time	1275 ns min

DC POWER REQUIREMENTS

	Standard		With Parity	
	Active*	Standby	Active*	Standby
+5 V ± 5%	6.0 W max	6.0 W max	7.5 W max	7.5 W max
+12 V ± 5%	12.5 W max	2.8 W max	14.0 W max	3.1 W max
Total	18.5 W max	8.8 W max	21.5 W max	10.6 W max

*Continuous operation such as DMA

MODES OF OPERATION

Read – Word
Write – Word/Byte
Read-Modify-Write Cycle – Word/Byte

INTERFACE CHARACTERISTICS

Compatible with DEC Q bus**

STANDARD I/O SIGNALS

Sync	(BSYNC L)
Data In	(BDIN L)
Data Out	(BDOUT L)
Reply	(BRPLY L)
Refresh	(BREF L)
Write Byte	(BWTBT L)
Date/Address	(BDAL0 L – BDAL15 L)
Power Up	(BDCOK H)

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PHYSICAL DIMENSIONS OF BOARD

10.45" x 8.9" x 0.44"

ENVIRONMENT

Operating	0°C to +55°C
Non-Operating	-40°C to +125°C
Humidity	To 90% without condensation

**Trademark of Digital Equipment Corporation

MOTOROLA

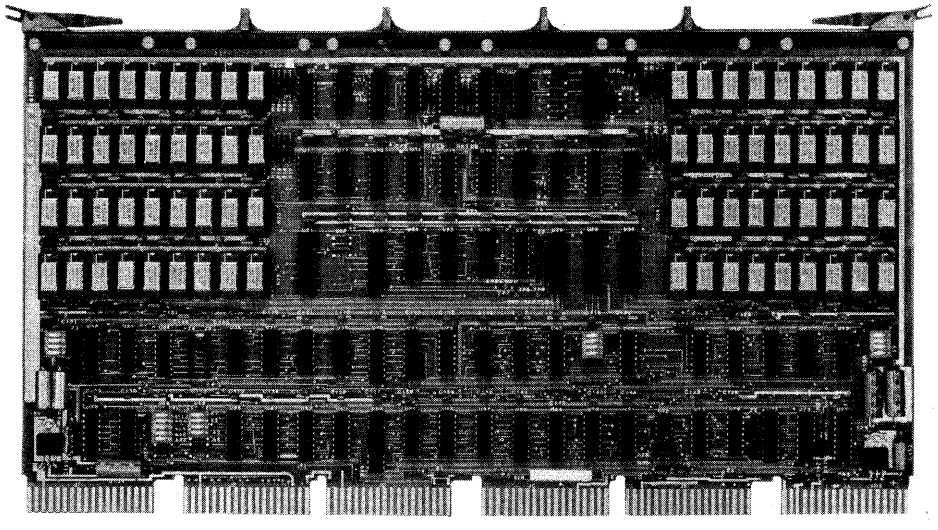
MMS1117

Advance Information

PDP-11* UNIBUS* COMPATIBLE RANDOM ACCESS MEMORIES, UP TO 128 KILOBYTES OF STORAGE CAPACITY PLUS OPTIONAL PARITY CONTROLLER ON A SINGLE CARD

The MMS1117 family of memory systems offers owners of PDP-11* computers an opportunity to easily add storage capacity and parity features to their system. Each member of the family is contained on a single plug-in circuit card that interfaces mechanically and electrically with the following models of UNIBUS* PDP-11* processors: 11/04, 11/05, 11/10, 11/34, 11/35, 11/40, 11/45, 11/50, 11/55, and 11/60. It plugs into a single hex SPC slot in any of the following backplanes: DD11-B, DD11-C, DD11-D and DD11-P.

The MMS1117 can provide up to 128K 8-bit bytes of main memory on a single module. Quick address select changes are possible via onboard switches. In addition, 1 or 2 kilowords of I/O page can selectively be made available for random access storage. Optional parity as well as full parity generation, detection, and exception control circuits can be provided on the same card with the memory. No additional bus loading is imposed on the system by the addition of the fully compatible parity controller option.



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MMS1117 FEATURES

- High Density
- Low Cost
- Fast Access and Cycle Times
- Low Power
- Fully UNIBUS Compatible
- High Reliability
- One UNIBUS Load

*Trademark of Digital Equipment Corporation

This is advance information and specifications are subject to change without notice.

MMS1117 OPTION DESIGNATOR SUFFIX

Typical Read Access Time	Parity Options	Total Storage Capacity (in Kilobytes)			
		32K	64K	96K	128K
290 ns	Parity + Controller	-32-PC	-34-PC	-36-PC	-38-PC
	Parity Data Only	-32-P	-34-P	-36-P	-38-P
	No Parity	-32	-34	-36	-38
360 ns	Parity + Controller	-42-PC	-44-PC	-46-PC	-48-PC
	Parity Data Only	-42-P	-44-P	-46-P	-48-P
	No Parity	-42	-44	-46	-48
390 ns	Parity + Controller	-52-PC	-54-PC	-56-PC	-58-PC
	Parity Data Only	-52-P	-54-P	-56-P	-58-P
	No Parity	-52	-54	-56	-58

ACCESS AND CYCLE TIMES

Option Designator Suffix	Write		Read		Cycle	
	Typical	Worst Case	Typical	Worst Case	Typical	Worst Case
-3X	105	125	290	315	375	390
-4X	115	135	360	390	480	500
-5X	115	135	390	420	560	585

MMS1117 POWER REQUIREMENTS

Nominal Voltage	Voltage Tolerance		Current Requirements		Input Pins
	Min	Max	Standby—Typ/WC (Amps)	Active—Typ/WC (Amps)	
+5 Vdc	4.75	5.25	2.0/2.5	2.0/2.5	DA2, EA2, FA2
+15 Vdc	15	20	0.15/0.20	0.35/0.70	AV1, AR1, CE1, CU1
−15 Vdc	−7.0	−20	0.015/0.030	0.015/0.030	FB2

MMS1117 BACK PLANE CONNECTOR PIN ASSIGNMENT

Row	A		B		C		D		E		F	
Side	1	2	1	2	1	2	1	2	1	2	1	2
Pin A					[**			+5 V		+5 V		+5 V
Pin B					[**							−15 V
Pin C		Gnd		Gnd	PA	Gnd		Gnd	A12	Gnd		Gnd
Pin D			+5BB			D15			A17	A15		
Pin E			*SSyn	*PA DE	***V_{DD}	D14			MSyn	A16		
Pin F						D13			A02	C1		
Pin H					D11	D12			A01	A00		
Pin J						D10			SSyn	C0		
Pin K						D09		[**	A14	A13		
Pin L						D08	Init	[**	A11			
Pin M						D07		[**				
Pin N	*P1				DCL0	D04		[**		A08		
Pin P	*P0					D05		[**	A10	A07		
Pin R	***V_{DD}					D01		[**	A09			
Pin S					PB	D00		[**				
Pin T	Gnd		Gnd		Gnd	D03	Gnd	[**	Gnd		Gnd	
Pin U					***V_{DD}	D02			A06	A04		
Pin V	***V_{DD}					D06			A05	A03		

*Options for use with External Parity Controller.

**Grant Continuity Jumpers

***V_{DD} is any voltage between +15 Vdc and +20 Vdc on any one of the four listed pins.

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MOTOROLA

MMS1118

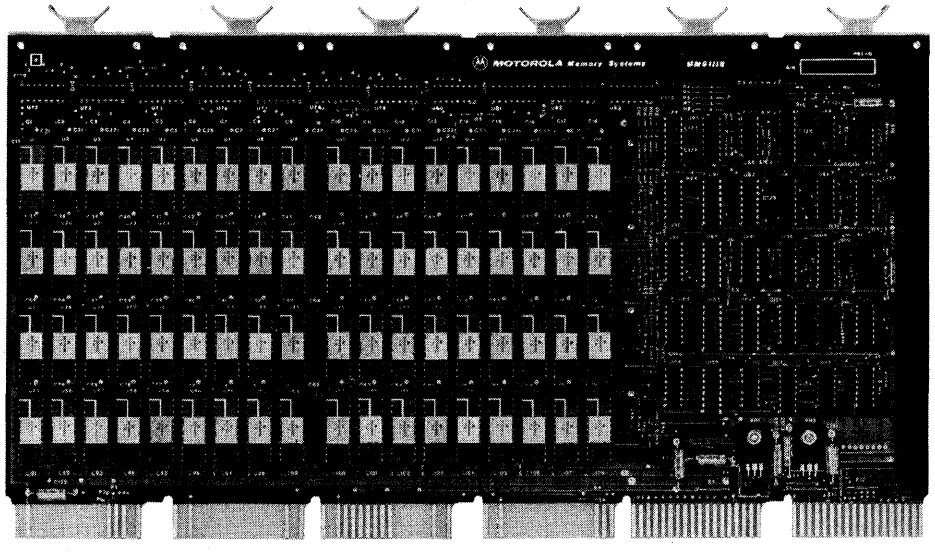
Advance Information

16K x 18 BIT PDP-11 ADD-IN SEMICONDUCTOR MEMORY

The Motorola MMS1118 is a 16K x 18 bit plug-in main memory system designed for DEC's PDP-11/04 and 34 computer family. The MMS1118 mounts directly into DEC's Modified UNIBUS* and is both hardware and software compatible in the PDP-11 systems with or without parity.

The system employs the low power MCM6605A-2 4K Dynamic RAM component. These RAM components are mounted on a single PC board that contains timing, control and bus interface logic.

With DEC's memory management unit, the MMS1118 can provide up to 127K words of main memory. Quick address select changes are possible with onboard jumpers. The low power and fast access time of the MMS1118 will greatly enhance the cost performance of a PDP-11 computer.



MMS1118 FEATURES

- High Density
- Low Cost
- Fast Access and Cycle Times
- Low Power
- Byte Operation
- High Reliability
- Modular Expandability (Address Select Jumpers)
- Module Interchangeability
- Short Circuit Memory Protection
- Optional Systems Available
  - MMS1118-1 12K x 18
  - MMS1118-2 8K x 18
- Power Down/Card Select Option
- Compatible with DD11L Backplane (Consult Factory)

*Trademark of Digital Equipment Corporation

This is advance information and specifications are subject to change without notice.

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SPECIFICATIONS

CAPACITY
8K, 12K and 16K words per board

WORD LENGTH
18 bits

PERFORMANCE

Access Time	550 ns max
Read Cycle Time	700 ns min
Write Cycle Time	700 ns min
Cycle Time with Refresh Interrupt	1400 ns min

DC CURRENT REQUIREMENTS

	Active**	Standby
+ 5V±5%	1.9 A max	1.9 A max
+ 15V±5%	400 mA max	60 mA max
−15V±20%	15 mA max	10 mA max

**Continuous operation such as DMA

MODES OF OPERATION
Read — Word
Write — Word/Byte

INTERFACE CHARACTERISTICS
Compatible with DEC's Modified UNIBUS*

STANDARD I/O SIGNALS

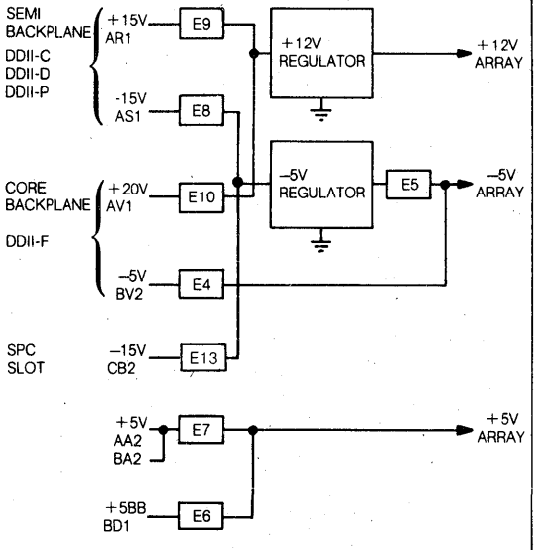
Master Sync — MSYN	Internal Slave Sync — INTSSYN
Byte Select — CO	Parity Bits — PO, P1
Read/Write — C1	DC Low — DCLO
Slave Sync — SSYN	Address — AO-A17
Parity Detect — PARDET	Data — DO-D15

PHYSICAL DIMENSIONS OF BOARD
15.7" x 8.94" x 0.44"

ENVIRONMENT

Operating	0°C to 55°C
Non-operating	− 40°C to 125°C
Humidity	90% without condensation

BACKPLANE OPTIONS



Semiconductor memory backplane DDII-C, D, P	Core backplane DDII-F
Without battery backup Cut: E4, E6, E10, E13	With −15 V on CB2: Cut E4, E6, E8, E9
With battery backup Cut: Er, E7, E10	Without −15 V on CB2 With −5 V on BV2 Cut: E5, E6, E8, E9, E13

Power options selectable by zero ohm resistors shown above.

ADDRESSING

Jumper table for starting addresses

Starting Address (Octal)	Addresses below starting address	Jumper selection A	B	C	D	E
000000	0K	1	1	1	0	0
020000	4K	1	1	0	1	1
040000	8K	1	1	0	1	0
060000	12K	1	1	0	0	1
100000	16K	1	1	0	0	0
120000	20K	1	0	1	1	1
140000	24K	1	0	1	1	0
160000	28K	1	0	1	0	1
200000	32K	1	0	1	0	0
220000	36K	1	0	0	1	1
240000	40K	1	0	0	1	0
260000	44K	1	0	0	0	1
300000	48K	1	0	0	0	0
320000	52K	0	1	1	1	1
340000	56K	0	1	1	1	0
360000	60K	0	1	1	0	1
400000	64K	0	1	1	0	0
420000	68K	0	1	0	1	1
440000	72K	0	1	0	1	0
460000	76K	0	1	0	0	1
500000	80K	0	1	0	0	0
520000	84K	0	0	1	1	1
540000	88K	0	0	1	1	0
560000	92K	0	0	1	0	1
600000	96K	0	0	1	0	0
620000	100K	0	0	0	1	1
640000	104K	0	0	0	1	0
660000	108K	0	0	0	0	1
700000	112K	0	0	0	0	0
720000	116K	1	1	1	1	1
740000	120K	1	1	1	1	0

Jumper table for board options

Memory capacity		Jumper selection F	H	J
16K	(normal use)	1	0	1
12K	only	1	1	1
14K	(Lower 2K of I/O page assigned to memory)***	1	1	0
15K	(Lower 3K of I/O page assigned to memory)***	0	1	0

***Set switches A-E for starting address of 100000 (Octal)
1=OPEN=HIGH 0=CLOSED=LOW

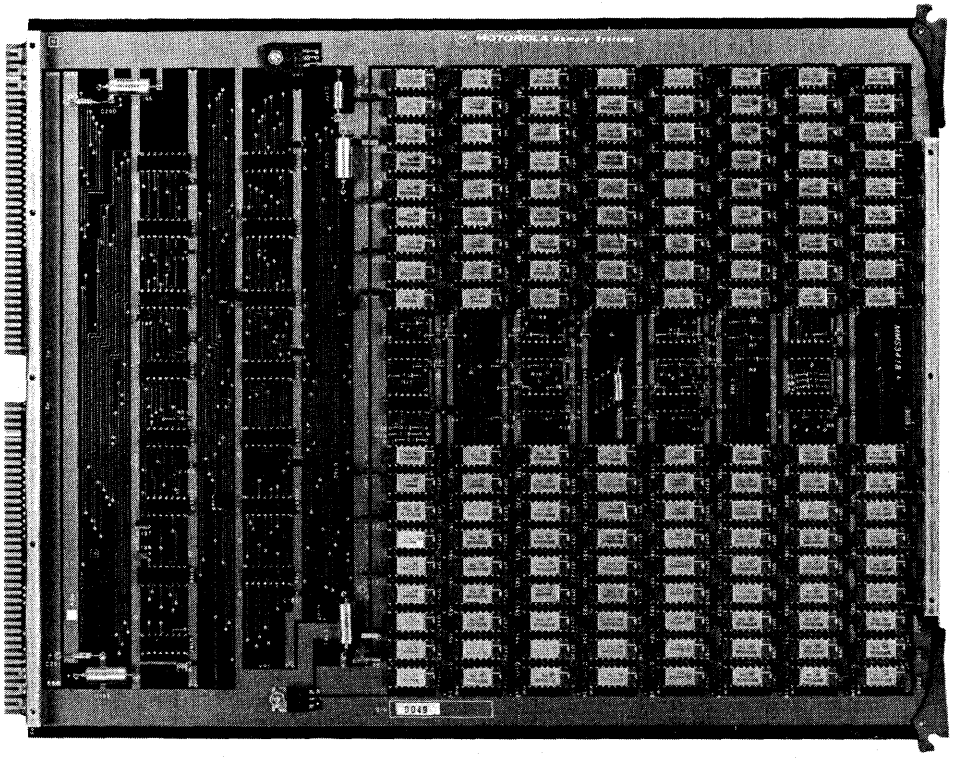
MOTOROLA

MMS3418

Advance Information

128K × 18
SEMICONDUCTOR MEMORY

The Motorola MMS3418 Memory Array Card provides 128K words by 18 bits of memory. It is designed for use with a memory control card such as Motorola's MMSCC-2 in systems requiring a very large memory. Multiple memory array cards can be used to increase word length and/or number of words stored.



Basically the MMS3418 is an array of 144 high-density, 16-pin, 16K dynamic RAM devices arranged in eight rows of eighteen. Buffer and driver circuits on the card interface the array to system circuitry. Gate and multiplexer circuits, which are controlled by external signals, function to connect the proper combination of address, strobe, and enable signals to the array to provide read, write, and distributed refresh operations. Sequencing and timing is a function of the associated system circuits.

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This is advance information and specifications are subject to change without notice.

SPECIFICATIONS

CAPACITY
128K Words per Board (K = 1024)

WORD LENGTH
18 Bits per Board

CYCLE TIME

Read Cycle Time	700 ns max
Write Cycle Time	700 ns max

Determined by associated memory control card

ACCESS TIME
475 ns max

MODES OF OPERATION
Read 18 Bits, Write 18 Bits, Distributed Refresh

DC POWER REQUIREMENTS

Voltage	Active	Standby
+5 V ± 5%	2 A max	2 A max
+15 V ± 5%	1 A max	0.6 A max
−9 V ± 10%	0.1 A max	0.1 A max

ENVIRONMENT

Operating Temperature	0 to 70°C
Non-Operating Temperature	−40 to 125°C

Humidity to 90% without condensation

BOARD DIMENSIONS
See outline diagram

INPUT/OUTPUT SIGNALS

Name	Description	Connector Pin
D0 to D17	Bidirectional data, 18 bits	P1-9 to P1-26
A1 to A11, A12 to A14	Memory address, 14 bits	P2-8 to P2-18, P2-48 to P2-50
RA0 to RA6	Refresh address, 7 bits	P2-51 to P2-57
R/W	Read or write control, 1 signal	P2-21
$\overline{BS}$	Board select, 1 signal	P2-30
$\overline{DATA\ ENABLE}$	Data output enable, 1 signal	P2-32
$\overline{RAS0}$ to $\overline{RAS7}$	Row address strobe, 8 signals	P2-72 to P2-65
$\overline{REF}$	Refresh control, 1 signal	P2-24
$\overline{CAS}$	Column address strobe, 1 signal	P2-26
CAE	Column address enable, 1 signal	P2-25

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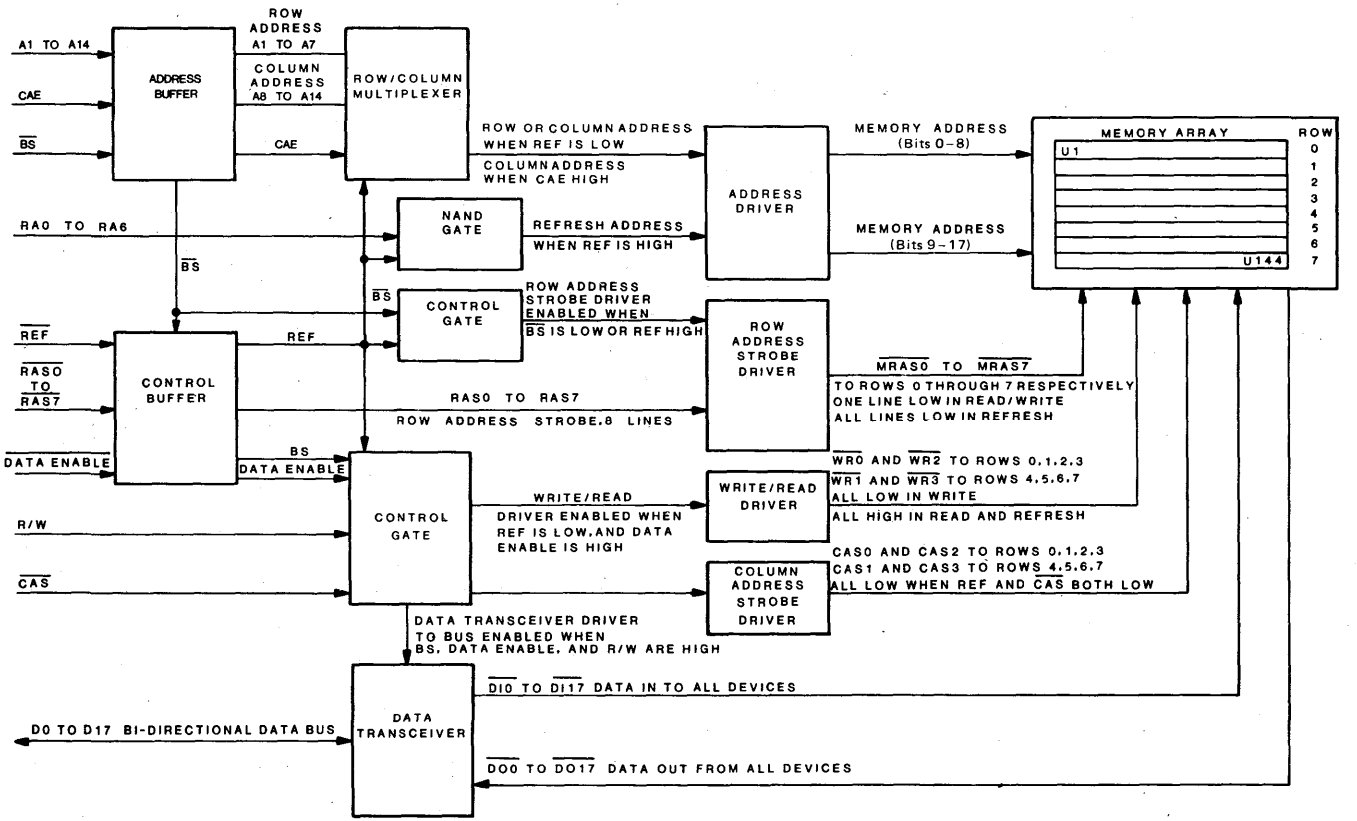
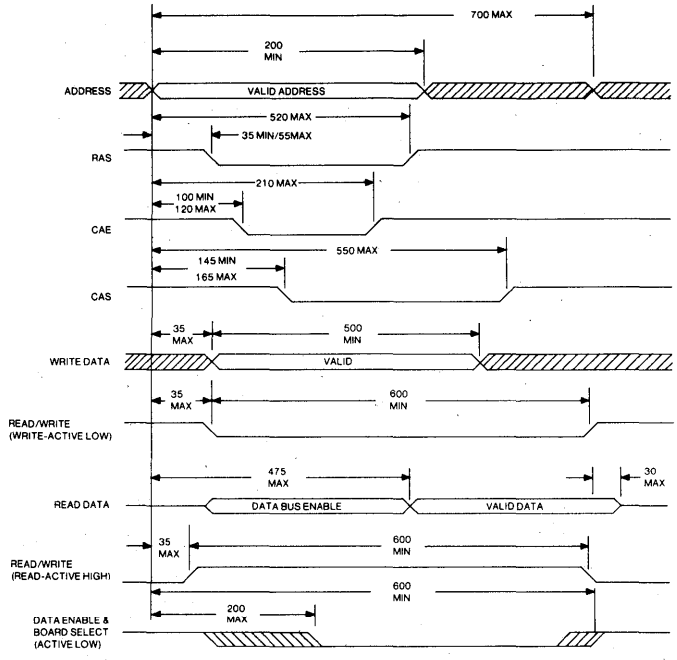
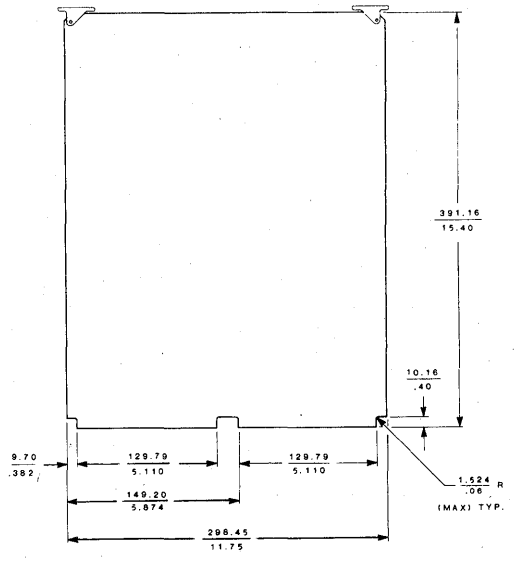
MMS3418 MEMORY ARRAY CARD BLOCK DIAGRAM



MMS3418 MEMORY ARRAY CARD TIMING DIAGRAM (ALL TIMES IN NANOSECONDS)



BOARD OUTLINE AND DIMENSIONS



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MOTOROLA

MMS68102

Advance Information

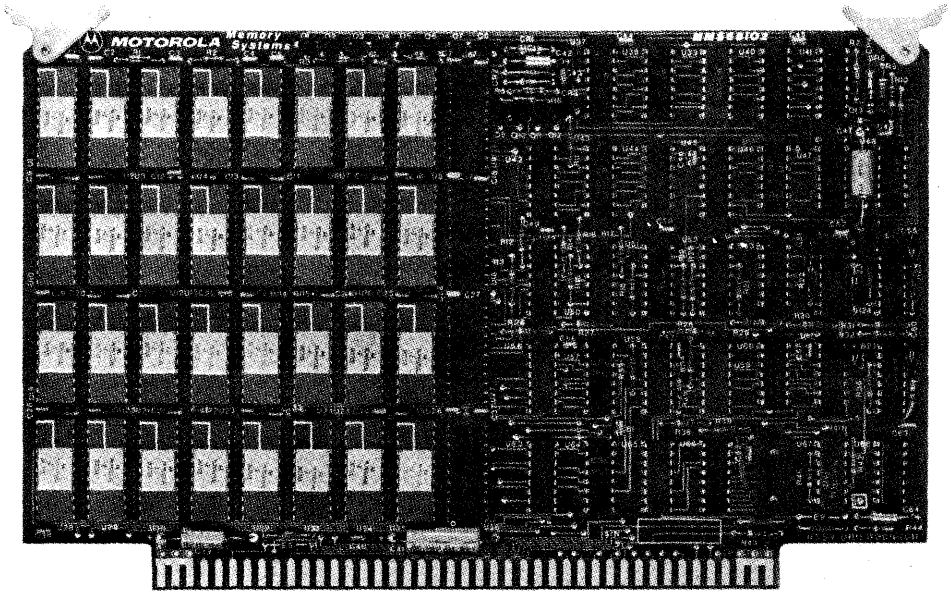
16K x 8 NON-VOLATILE SEMICONDUCTOR MEMORY

The Motorola MMS68102 is a 16K x 8-Bit Non-Volatile Memory System designed for use with the M6800 EXORciser System.*

The system employs the MCM6605 22 pin 4K dynamic RAM component. These RAM components are mounted on a single PC board that contains timing, control, and bus interface logic. The refresh requirement is handled by stealing cycles from the processor. CMOS logic is used in the refresh and powerfail circuits to allow low power battery backup operation.

The MMS68102, using an external battery backup circuit, has the capability of refreshing itself while power is removed from the EXORciser power supply. This refresh capability enables the module to retain its stored data during a power loss.

The MMS68102 may be paralleled to provide 64K words of memory. Onboard jumpers provide easy address select changes.



MMS68102 FEATURES

- High Density
- Low Cost
- Fast Access and Cycle Times
- High Reliability
- Modular Expandability (Address Select Switches)
- Module Interchangeability
- Low Power Battery Backup Operation
- Systems Available
  MMS68102-1 8K x 8
  MMS68102A 16K x 9
  MMS68102A-1 8K x 9

* Trademark of Motorola, Inc.

This is advance information and specifications are subject to change without notice.

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SPECIFICATIONS

CAPACITY
16K words per board

WORD LENGTH
8 bits

PERFORMANCE

Access Time**	280 ns max
Read Cycle Time	1.0 μs min
Write Cycle Time	1.0 μs min
Refresh Cycle Time	1.0 μs min

**Measured from rising edge of MEMCLK

DC POWER REQUIREMENTS 16K x 8(9)

	Active***	Standby	Battery Backup
+5 V ±5%	4.2 Wmax	4.2 Wmax	—
+12 V ±5%	3.4 Wmax	1.4 Wmax	.3 Wmax
Total	7.6 Wmax	5.6 Wmax	.3 Wmax

MODES OF OPERATION
Read Cycle
Write Cycle

***Continuous operation such as DMA

INTERFACE CHARACTERISTICS
M6800 EXORciser Compatible

STANDARD I/O SIGNALS

Memory Clock	(MEMCLK)
Valid Memory Address	(VMA)
Read/Write	(R/W)
Address	(A0-A15)
Data	($\overline{D0}$-$\overline{D7}$)
Valid User Address	(VUA)
Refresh Request	($\overline{REFREQ}$)
Refresh Grant	(REFGRANT)
Battery +12 Volts	(BAT+12)

ADDITIONAL I/O SIGNALS

Power Fail (12 Volt Signal)	(STDBY) Pin V
Refresh Clock (12 Volt Signal)	($\overline{REFCLK}$) Pin 27
Parity Data	($\overline{D8}$) Pin 28

PHYSICAL DIMENSIONS OF BOARD
6" x 9.75" x .5"

ENVIRONMENT

Operating	0°C to 70°C
Non-Operating	−40°C to 125°C
Humidity	To 90% without condensation

PREPROGRAMMING:

★ CAUTION. The MMS68102 comes prewired in the following manner:
(1) Master Refresh
(2) VUA
(3) Lower 32K Address Boundary
For Alterations of the above see Table 1.

Table 1

OPTIONS	JUMPERS IN	JUMPERS OUT
VUA VMA	E4 E5	E5 E4
Master Refresh Slave Refresh	E1 & E6	 E1 & E6
Lower 32K Upper 32K	E3 E2	E2 E3

ADDRESSING

A fully populated MMS68102 can be programmed with jumpers to occupy a 16K Memory Address Space, but must be mapped on a 32K boundary.

The independent 4K blocks of the MMS68102 are shown as blocks A, B, C, & D in Figure 1. These blocks need not be mapped into any contiguous address space, but should not be mapped into the same one.

An example of mapping block A into address space (12K-16K) is as follows:
Lower 32K is selected with E2 out & E3 in.
Block A enable Pin 9 or 10 of J1, from Table 3, is connected to Pin 7 of J1, from Table 2, for the (12K-16K) address space.

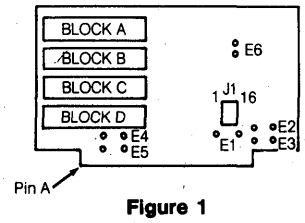


Figure 1

Table 2

LOWER 32K	UPPER 32K	J1 PIN
0K-4K	32K-36K	1
4K-8K	36K-40K	3
8K-12K	40K-44K	5
12K-16K	44K-48K	7
16K-20K	48K-52K	2
20K-24K	52K-56K	4
24K-28K	56K-60K	6
28K-32K	60K-64K	8

Table 3

J1 PIN	BLOCK ENABLE
9 & 10	A
11 & 12	B
13 & 14	C
15 & 16	D

MOTOROLA

MMS68103

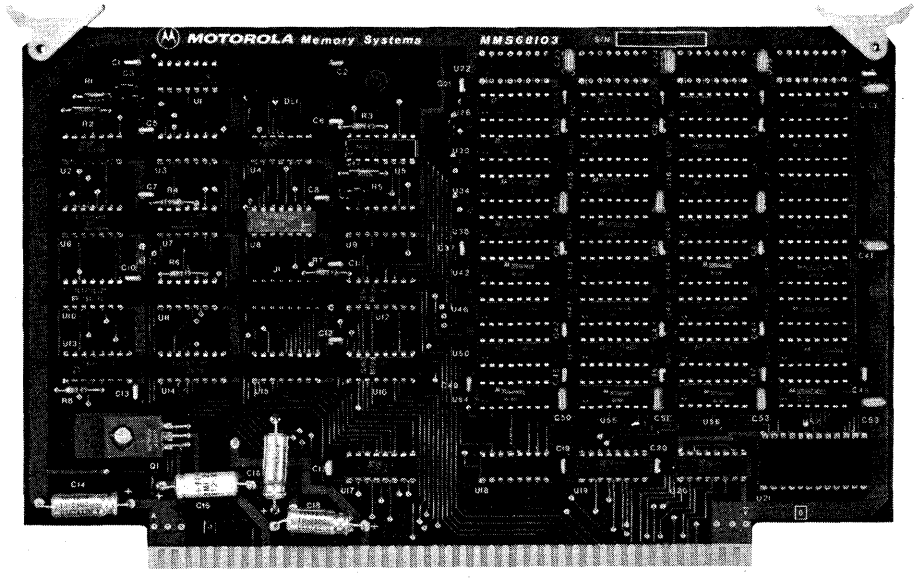
Advance Information

16K x 8 SEMICONDUCTOR MEMORY FOR M6800 SYSTEMS

The Motorola MMS68103 is a 16K-word × 8-bit plug-in memory module designed for use with M6800 based systems.

The module employs high density, 16-pin, 4K dynamic RAM components, mounted on a single PC board that contains timing, control, and bus interface logic. A hidden refresh scheme requires no additional cycles or interface from the CPU. This permits the use of valuable CPU time for purposes other than refreshing.

The MMS68103 can provide up to 64K words of memory. Address select changes are easily made with on-board address jumpers.



MMS68103 FEATURES

- Hidden Refresh
- High Density
- Low Cost
- Fast Access and Cycle Times
- High Reliability
- Modular Expandability (Address Select Jumpers)
- MEK6800D2 Compatible
- MicroModule Compatible
- Options Available
  - MMS68103-1 8K x 8
  - MMS68103A 16-K x 9
  - MMS68103A-1 8K x 9

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This is advance information and specifications are subject to change without notice.

SPECIFICATIONS

CAPACITY

16K words per board

WORD LENGTH

8 bits

PERFORMANCE

Access Time	475 ns max	
Read Cycle Time	1.0 μs min.	2.5 μs max*
Write Cycle Time	1.0 μs min.	2.5 μs max*

*(256 BØ2 cycles required within 640 μs)

DC POWER REQUIREMENTS

	Active*	Standby
+5 V ±5%	6.0 W max	6.0 W max
+12 V ±5%	4.0 W max	2.0 W max
−12 V ±10%	0.02 W max	0.02 W max
Total	10.02 W max	8.02 W max

*Continuous operation such as DMA

MODES OF OPERATION

Read Cycle
Write Cycle

INTERFACE CHARACTERISTICS

MC6800 Compatible

STANDARD I/O SIGNALS

Bus Ø2	(BØ2)
Valid User Address	(VUA)
Read/Write	(R/W)
Address	(A0-A15)
Data	($\overline{D0}$-$\overline{D7}$)

PHYSICAL DIMENSIONS OF BOARD

6.00" x 9.75" x 0.44"

ENVIRONMENT

Operating	0°C to 70°C
Non-Operating	−40°C to 125°C
Humidity	To 90% without condensation

MOTOROLA

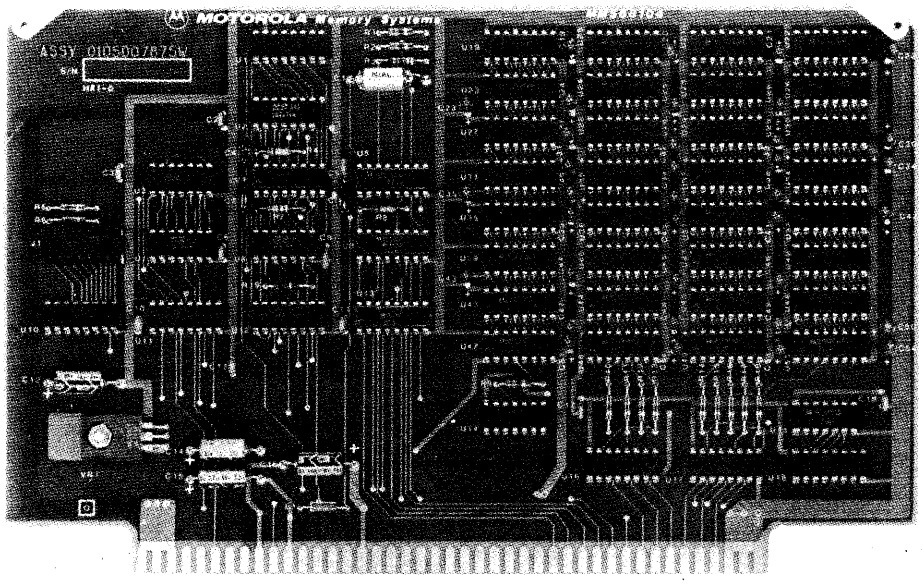
MMS68104

16K x 8 SEMICONDUCTOR MEMORY FOR M6800 SYSTEMS

The Motorola MMS68104 is a 16K x 8-bit plug in memory system designed for use with the MEK6800D2 Kit.

The system employs the high density 16 pin 4K dynamic RAM component. These RAM components are mounted on a single PC board that contains timing, control, and bus interface logic. The system employs a handshake refresh that interfaces with the CPU.

The MMS68104 can provide up to 64K words of memory. Address select changes are easily made with on-board address jumpers.



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MMS68104 FEATURES

- High Density
- Low Cost
- High Reliability
- Modular Expandability (Address Select Jumpers)

SPECIFICATIONS

CAPACITY

16K words per board

WORD LENGTH

8 bits

PERFORMANCE

Access Time	650ns max*
Read Cycle Time	1.5μs min
Write Cycle Time	1.5μs min

*From leading edge of MEMCLK

DC CURRENT REQUIREMENTS

	Active**	Standby
+5 V ±5%	920 mA max	920 mA max
+12 V ±5%	450 mA max	80 mA max
−12 V ±10%	10 mA max	10 mA max
Total	1.4 A max	1.1 A max

**Continuous operation such as DMA

INTERFACE CHARACTERISTICS

MC6800 Compatible

STANDARD I/O SIGNALS

Memory Clock	(MEMCLK)	Refresh Grant	(REF GNT)
Valid Memory Address	(VMA)	Refresh Request	(REF REQ)
Read/Write	(R/W)		
Address	(A0-A15)		
Data	(D0-D7)		

PHYSICAL DIMENSIONS OF BOARD

6.00" x 9.75" x 0.44"

ENVIRONMENT

Operating	0°C to 50°C
Non-Operating	−40°C to 125°C
Humidity	To 90% without condensation

ADDRESSING

The MMS68104 can be programmed with jumpers to occupy 16K in a 64K memory address space in independent 8K blocks. To map the first 8K block into an address space, connect either J1-10, 13, 14 or 16 to the indicated pin in the following table. To map the second 8K block into an address space, connect either J1-9, 11, 12 or 15 to the indicated pin in the following table.

HEXADECIMAL ADDRESS	ADDRESS SPACE	PIN NUMBER ON J1
0000 — 1FFF	0K — 8K	1
2000 — 3FFF	8K — 16K	2
4000 — 5FFF	16K — 24K	4
6000 — 7FFF	24K — 32K	6
8000 — 9FFF	32K — 40K	3
A000 — BFFF	40K — 48K	5
C000 — DFFF	48K — 56K	7
E000 — FFFF	56K — 64K	8

MEMORY EXPANSION

Four MMS68104 memory boards may be connected to the same bus to provide up to 64K words. When two or more MMS68104s are connected to the same bus, E1 should be removed from all but one of the memory boards. (E1 is a green zero ohm jumper located near the connector edge on the MMS68104.) This enables the one MMS68104 to act as the master when requesting refresh cycles which all of the memory boards utilize.

APPLICATION TO MEK6800D2 KIT

The following is a description of the modifications and additions that are needed for using the MMS68104 memory card in the MEK6800D2 kit.

1. Unplug 6810 RAMS (U14, U16, U18, U19) on kit board.
2. Cut foil path to U7, pin 4. Tie pin 4 to +5V.
3. Plus, the following additions: See Figure 1.
4. For further information on adding data terminal and memory expansion refer to Application Note 771.

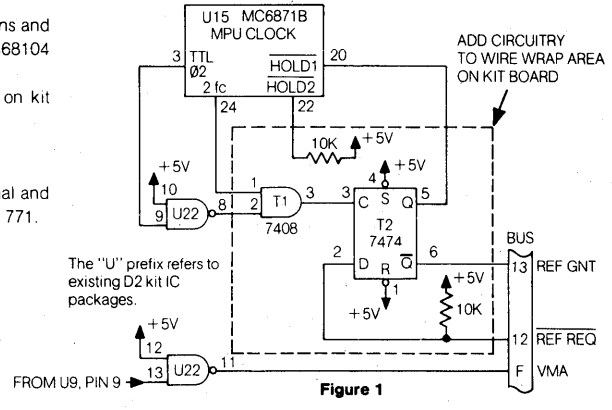
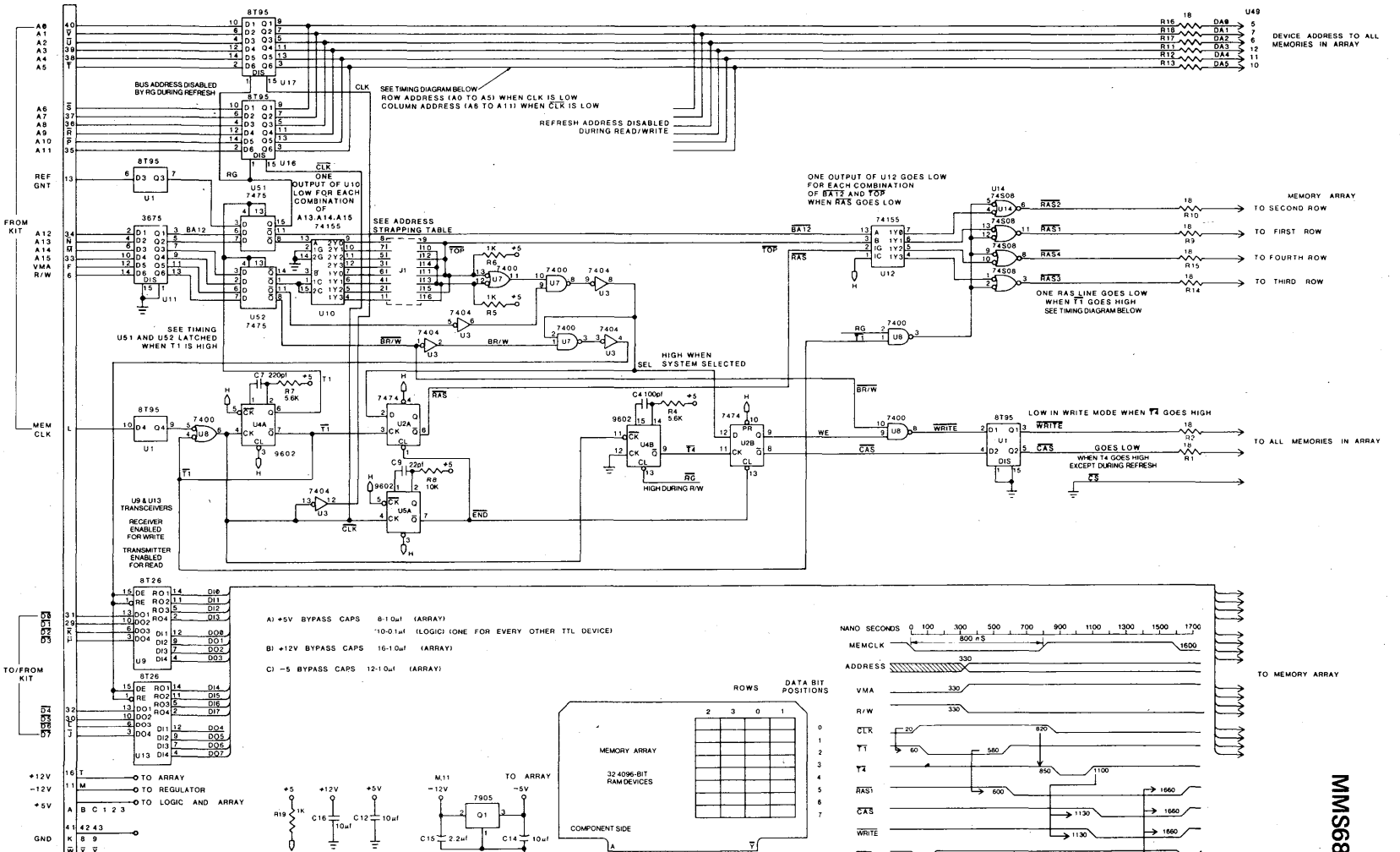


Figure 1



SCHEMATIC REVISION 2
APPLIES TO MEMORY BOARD REV A

MMS68104 Memory System Read/Write Schematic Diagram

MMS68104

5-21

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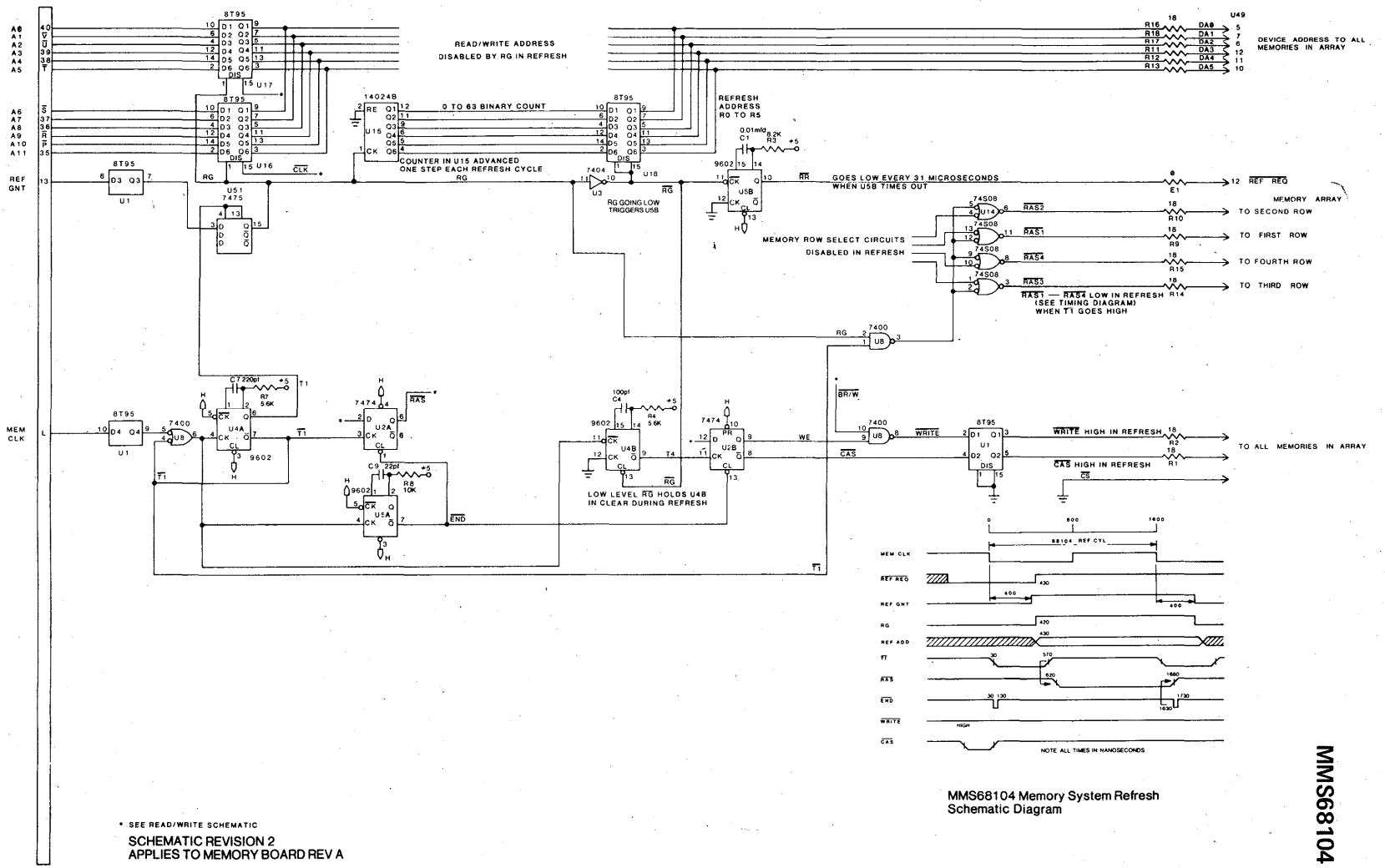


* SEE READ/WRITE SCHEMATIC

SCHEMATIC REVISION 2
APPLIES TO MEMORY BOARD REV A

MMS68104 Memory System Refresh
Schematic Diagram

MOTOROLA

MMS80810

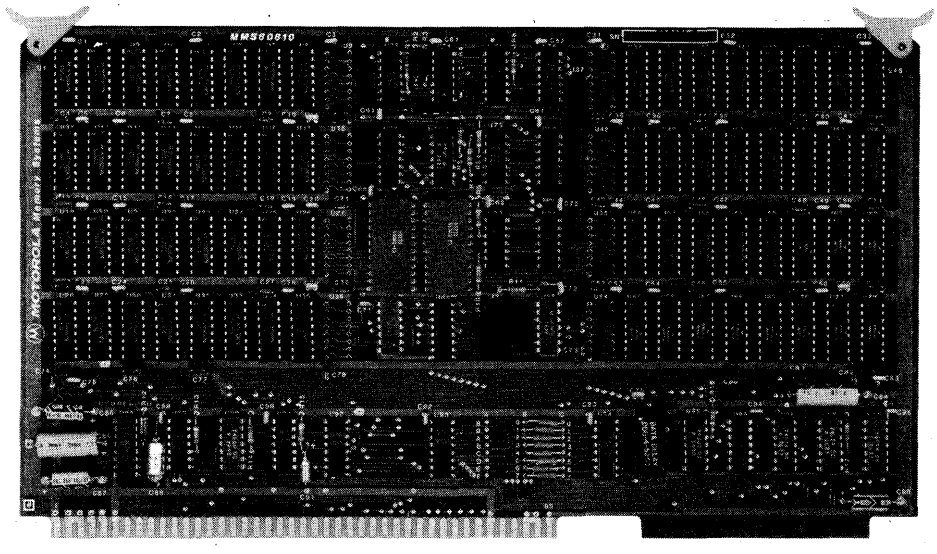
Advance Information

32K x 8 SEMICONDUCTOR MEMORY FOR 8080A SYSTEMS

The Motorola MMS80810 is a 32K-word x 8 bit plug in memory system designed for use with 8080A based systems and is pin compatible with SBC 80/10 single board computer.

The system employs the high density 16 pin 4K dynamic RAM component. The RAM components are mounted on a single PC board that contains timing, control and bus interface logic. Refresh logic is also contained on the memory board. A refresh cycle is generated by on-board refresh logic and is asynchronous to the CPU.

A fully populated MMS80810 can be programmed with jumpers to occupy 32K words out of a possible 64K memory space in independent 8K segments. The 8K segments must begin at 8K boundaries. Address select changes are easily made with on-board address jumpers.



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MMS80810 FEATURES

- High density
- Low cost
- Fast access and cycle times
- High Reliability
- Modular Expandability (Address Select Jumpers)
- Modular Interchangeability
- Optional Systems Available:

  MMS80810-1 16K x 8

This is advance information and specifications are subject to change without notice.

SPECIFICATIONS

CAPACITY

32K words per board

WORD LENGTH

8 bits

PERFORMANCE

Access Time	400 ns max*
Read Cycle Time	760 ns min*
Write Cycle Time	760 ns min*

*Refresh cycle can extend these times by 760 ns.

MODES OF OPERATION

Read Cycle
Write Cycle

INTERFACE CHARACTERISTICS

SBC 80/10 Compatible

STANDARD I/O SIGNALS

Read	MRDC/
Write	MWTC/
System Reset	INIT/
Address	ADR0/-ADRF/
Data	DAT0/-DAT7/
Transfer Acknowledge	XACK/

PHYSICAL DIMENSIONS OF BOARD

12" x 6.75" x 0.5"

ENVIRONMENT

Operating	0°C to 70°C
Non-Operating	−40°C to 125°C
Humidity	To 90% without condensation

DC POWER REQUIREMENTS

	32K x 8		16K x 8	
	Active*	Standby	Active*	Standby
+5 V ±5%	6.0 W max	6.0 W max	6.0 W max	6.0 W max
+12 V ±5%	7.5 W max	3.0 W max	6.5 W max	1.5 W max
−5 V ±10%	0.1 W max	0.1 W max	0.1 W max	0.1 W max
Total	13.6 W max	9.1 W max	12.6 W. max	7.6 W max

*Continuous operation such as DMA

I.C. SOCKET MEMORY ADDRESS PIN OUT		
HEXADECIMAL ADDRESS	ADDRESS SPACE	PIN # ON J1
0000-1FFF	0K-8K	1
2000-3FFF	8K-16K	3
4000-5FFF	16K-24K	5
6000-7FFF	24K-32K	7
8000-9FFF	32K-40K	2
A000-BFFF	40K-48K	4
C000-DFFF	48K-56K	6
E000-FFFF	56K-64K	8

Table 1.

8K BLOCK ENABLES	
Block	Pin # ON J1
A	9, 10
B	11, 12
C	13, 14
D	15, 16

Table 2.

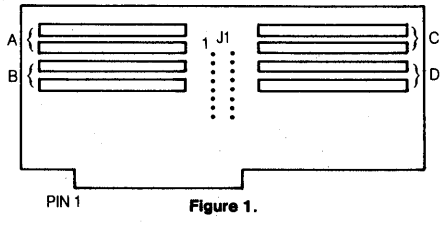
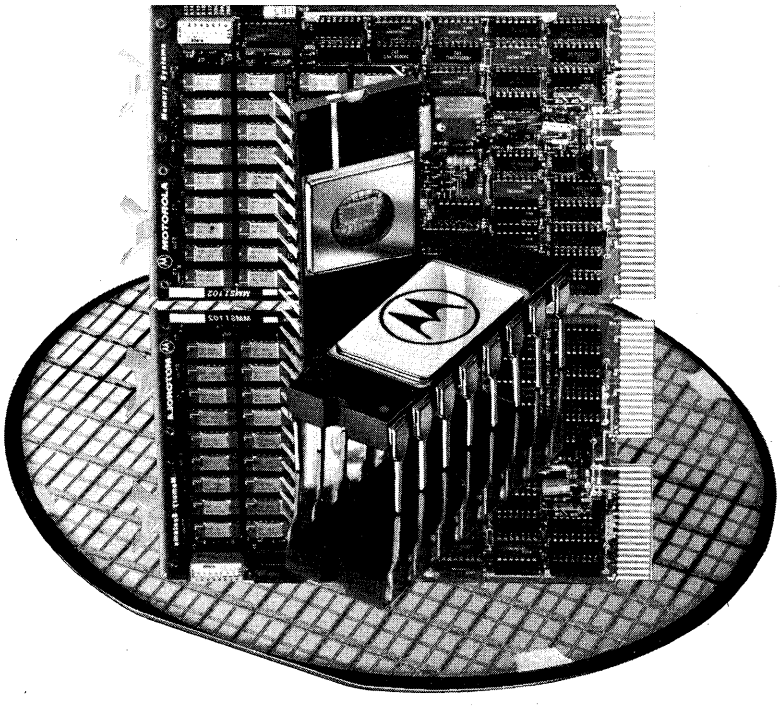


Figure 1.

The independent 8K blocks of the MMS80810 are shown as blocks A, B, C & D in Figure 1. These blocks need not be mapped into any contiguous address space, but should not be mapped into the same one.

An example of mapping block A into address space (8K-16K) is as follows:

Block A Enable Pin 9 or 10 of J1, from Table 2 is connected to Pin 3 of J1, from Table 1, for the (8K-16K) address space. For 16K, blocks A & B will be populated.



Mechanical Data

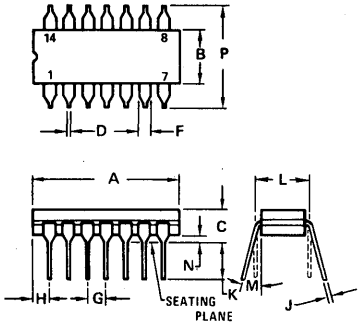
6

MECHANICAL DATA

The packaging availability for each device is indicated on the individual data sheets. Dimensions for the packages are given in this section.

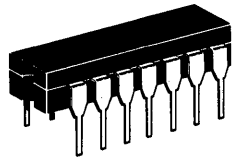
14-PIN PACKAGES

CERAMIC PACKAGE
CASE 632



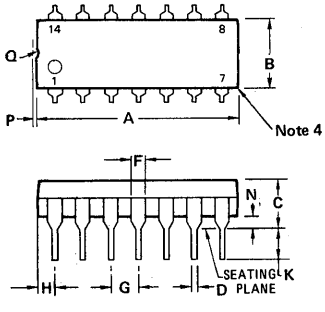
DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.58	0.015	0.023
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	1.91	2.29	0.075	0.090
J	0.20	0.38	0.008	0.015
K	3.18	5.08	0.125	0.200
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

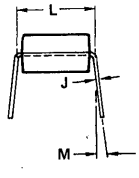
CASE 632-06



NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH MO-001 AA OUTLINE SHALL APPLY.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "A" AND "B" (632-06) DO NOT INCLUDE GLASS RUN-OUT.
4. LEADS WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT SEATING PLANE AND MAXIMUM MATERIAL CONDITION.

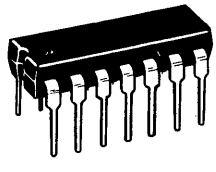
PLASTIC PACKAGE
CASE 646





DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

CASE 646-05

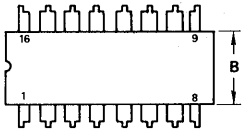


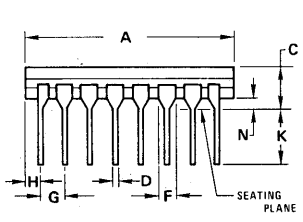
NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

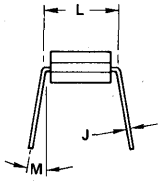
6

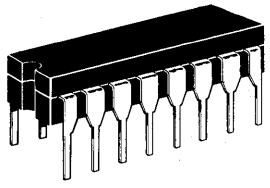
16-PIN PACKAGES

CERAMIC PACKAGE
CASE 620







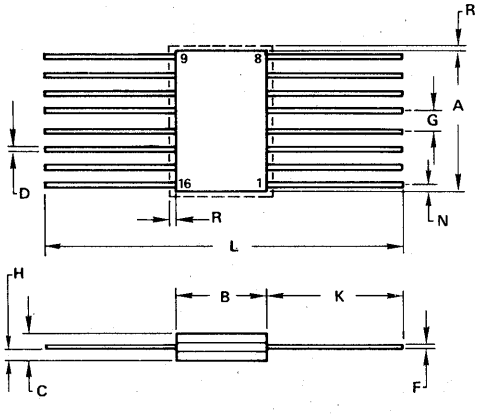


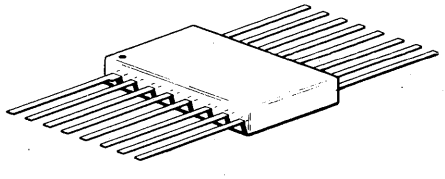
DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	5.08	0.125	0.200
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

CASE 620-06

1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. PACKAGE INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIM "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT.
5. DIM "F" MAY NARROW TO 0.76 mm (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

CERAMIC PACKAGE
CASE 650





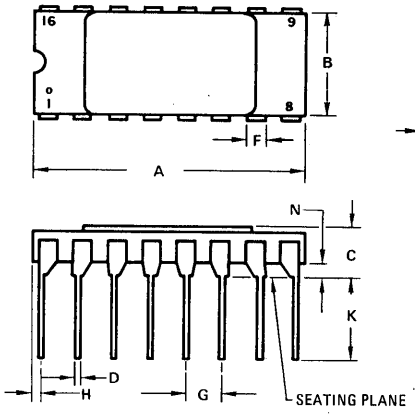
DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.22	7.24	0.245	0.285
C	1.52	2.03	0.060	0.080
D	0.41	0.48	0.016	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.64	0.89	0.025	0.035
K	6.35	9.40	0.250	0.370
L	18.92	–	0.745	–
N	–	0.51	–	0.020
R	–	0.38	–	0.015

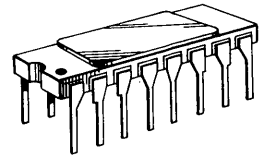
CASE 650-03

NOTES:
1. LEAD NO. 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER.
2. LEADS WITHIN 0.13 mm (0.005) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

16-PIN PACKAGES (Continued)

CERAMIC PACKAGE
CASE 690





NOTE:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

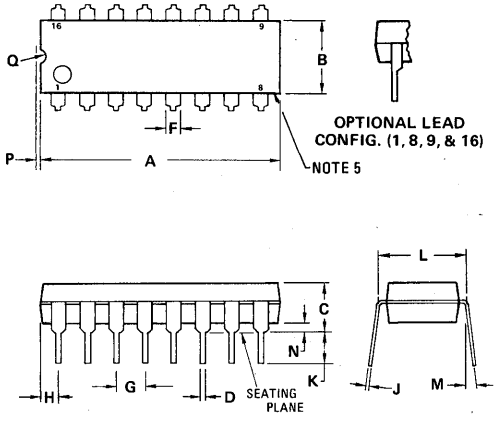
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.07	20.57	0.790	0.810
B	7.11	7.62	0.280	0.300
C	2.67	3.81	0.105	0.150
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	3.56	4.06	0.140	0.160
L	7.62 BSC		0.300 BSC	
M	–	10°	–	10°
N	0.38	1.40	0.015	0.055

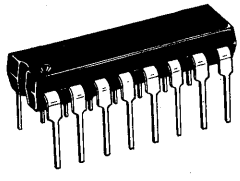
CASE 690-11

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.07	20.57	0.790	0.810
B	7.11	7.62	0.280	0.300
C	2.67	3.94	0.105	0.155
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	3.18	5.08	0.125	0.200
L	7.62 BSC		0.300 BSC	
M	–	10°	–	10°
N	0.38	1.40	0.015	0.055

CASE 690-12

PLASTIC PACKAGE
CASE 648





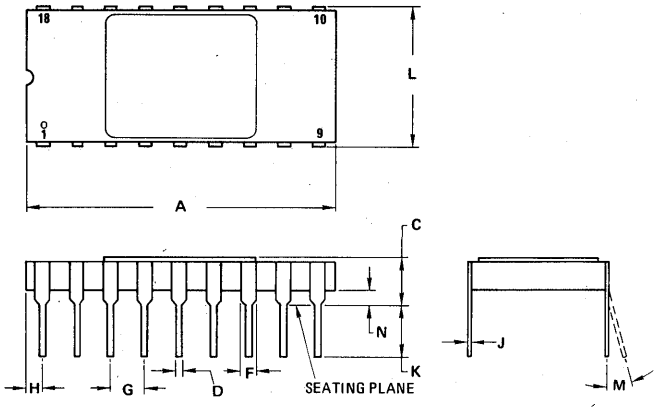
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

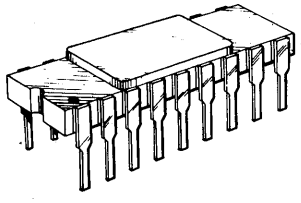
CASE 648-05

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 8, 9, and 16).
5. ROUNDED CORNERS OPTIONAL.

18-PIN PACKAGES

CERAMIC PACKAGE
CASE 680



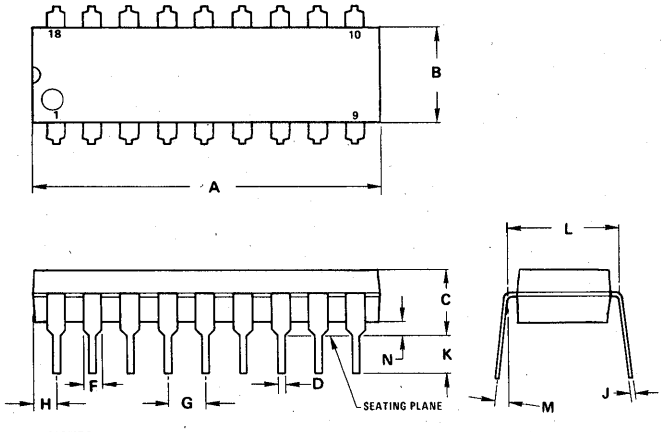


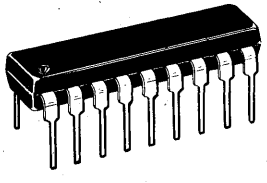
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.48	23.24	0.885	0.915
B	7.16	7.57	0.282	0.298
C	3.18	4.27	0.125	0.168
D	0.38	0.58	0.015	0.023
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.68	4.44	0.105	0.175
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.38	1.40	0.015	0.055

CASE 680-06

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RAD OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

PLASTIC PACKAGE
CASE 707





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.94	4.57	0.155	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

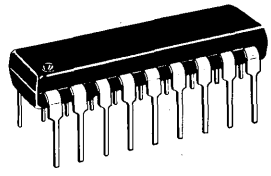
CASE 707-02

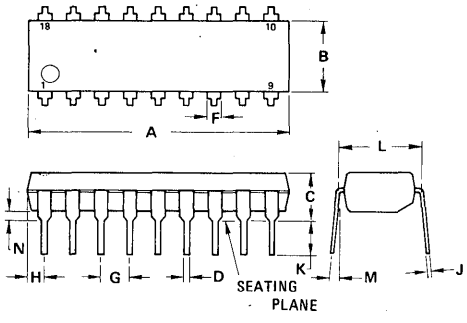
NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

6

18-PIN PACKAGES (Continued)

PLASTIC PACKAGE
CASE 701-01





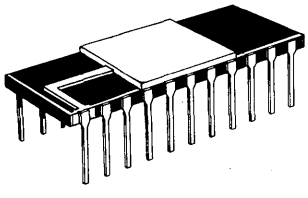
NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUM OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM "G").
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

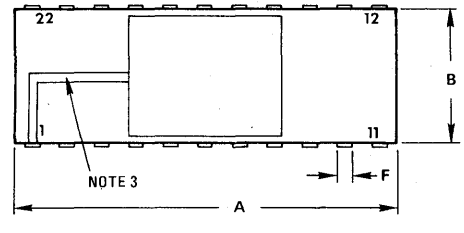
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	23.11	23.88	0.910	0.940
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	0^0	10^0	0^0	10^0
N	0.51	1.02	0.020	0.040

CASE 701-01

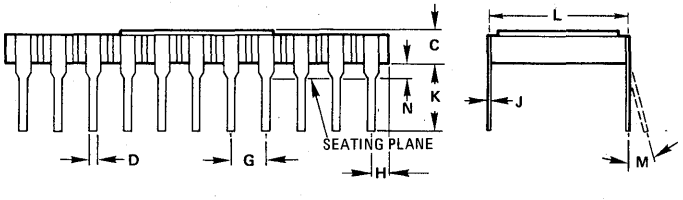
22-PIN PACKAGES

CERAMIC PACKAGE
CASE 677





NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. EXPOSED CONTACT TO LEAD 1, OPTIONAL.

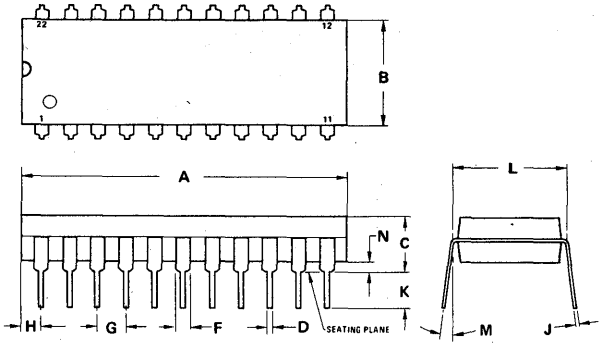


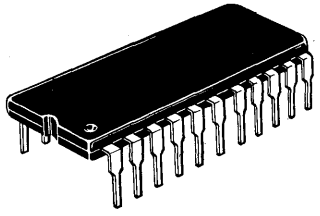
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.15	27.71	1.069	1.091
B	9.65	10.06	0.380	0.396
C	2.79	3.56	0.110	0.140
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.51	1.52	0.020	0.060
J	0.20	0.30	0.008	0.012
K	3.18	4.45	0.125	0.175
L	9.91	10.41	0.390	0.410
M	–	10^0	–	10^0
N	0.64	1.27	0.025	0.050

CASE 677-05

22-PIN PACKAGES (Continued)

PLASTIC PACKAGE
CASE 708





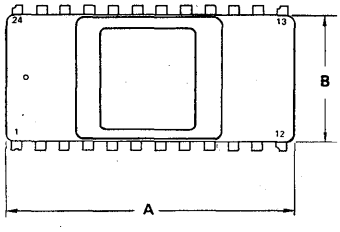
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	28.83	29.59	1.135	1.165
B	8.64	9.14	0.340	0.360
C	4.57	5.08	0.180	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.78	2.03	0.070	0.080
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	9.65	10.16	0.380	0.400
M	0^0	10^0	0^0	10^0
N	0.51	1.02	0.020	0.040

CASE 708-01

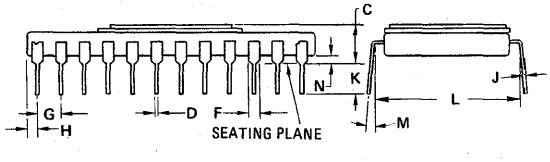
NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

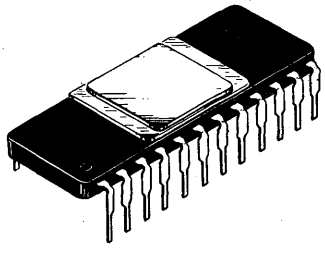
24-PIN PACKAGES

CERAMIC PACKAGE
CASE 684



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE WITH MAXIMUM MATERIAL CONDITION.
2. LEAD NO. 1 CUT FOR IDENTIFICATION, OR BUMP ON TOP.
3. DIM "L" TO INSIDE OF LEADS. (MEASURED 0.51 mm (0.020) BELOW PKG BASE)





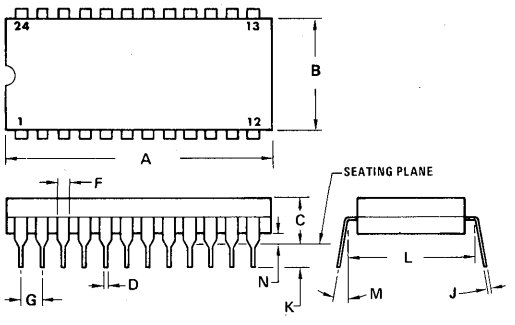
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	29.34	30.86	1.155	1.215
B	12.70	14.22	0.500	0.560
C	3.05	3.94	0.120	0.155
D	0.38	0.51	0.015	0.020
F	0.89	1.40	0.035	0.055
G	2.54 BSC		0.100 BSC	
H	0.89	1.40	0.035	0.055
J	0.20	0.30	0.008	0.012
K	2.92	3.68	0.115	0.145
L	14.86	15.87	0.585	0.625
M	–	15^0	–	15^0
N	0.51	1.14	0.020	0.045

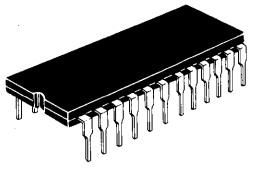
CASE 684-04

6

24-PIN PACKAGES (Continued)

CERAMIC PACKAGE
CASE 623



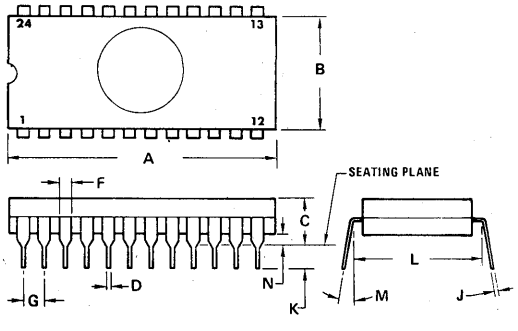


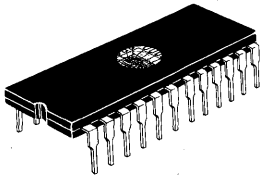
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.26	1.230	1.270
B	12.70	13.72	0.500	0.540
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.29	4.06	0.090	0.160
L	15.24 BSC		0.600 BSC	
M	0^0	15^0	0^0	15^0
N	0.51	1.27	0.020	0.050

CASE 623-03

NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL)

CERAMIC PACKAGE
CASE 623A





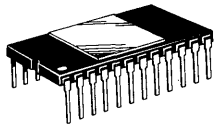
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.26	1.230	1.270
B	12.70	13.72	0.500	0.540
C	4.06	5.84	0.160	0.230
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.29	4.06	0.090	0.160
L	15.24 BSC		0.600 BSC	
M	0^0	15^0	0^0	15^0
N	0.51	1.27	0.020	0.050

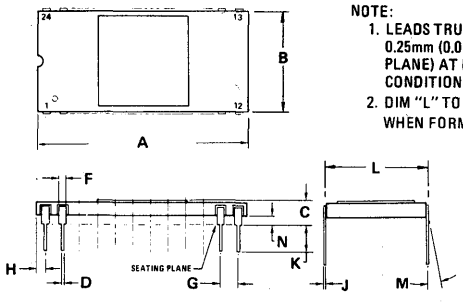
CASE 623A-01

NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

24-PIN PACKAGES (Continued)

CERAMIC PACKAGE
CASE 716

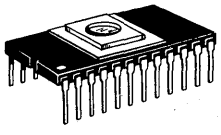


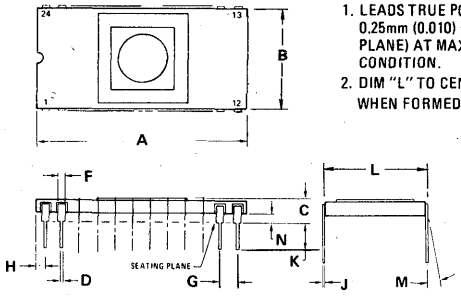


NOTE:
1. LEADS TRUE POSITIONED WITHIN 0.25mm (0.010) DIA (AT SEATING PLANE) AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.64	30.99	1.088	1.220
B	14.94	15.34	0.588	0.604
C	2.67	4.32	0.105	0.170
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	2.54	4.19	0.100	0.165
L	14.99	15.49	0.590	0.610
M	–	10^0	–	10^0
N	1.02	1.52	0.040	0.060

CASE 716-06





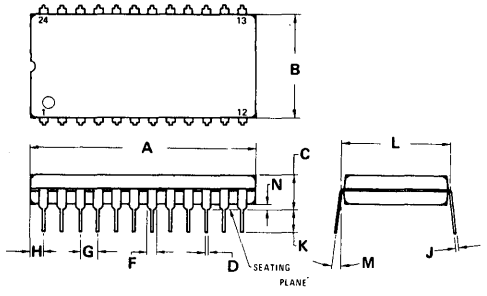
NOTE:
1. LEADS TRUE POSITIONED WITHIN 0.25mm (0.010) DIA (AT SEATING PLANE) AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

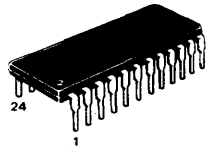
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.64	30.99	1.088	1.220
B	14.94	15.34	0.588	0.604
C	3.18	5.08	0.125	0.200
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	2.54	4.19	0.100	0.165
L	14.99	15.49	0.590	0.610
M	–	10^0	–	10^0
N	1.02	1.52	0.040	0.060

CASE 716-07

24-PIN PACKAGES (Continued)

PLASTIC PACKAGE
CASE 709





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

CASE 709-02

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

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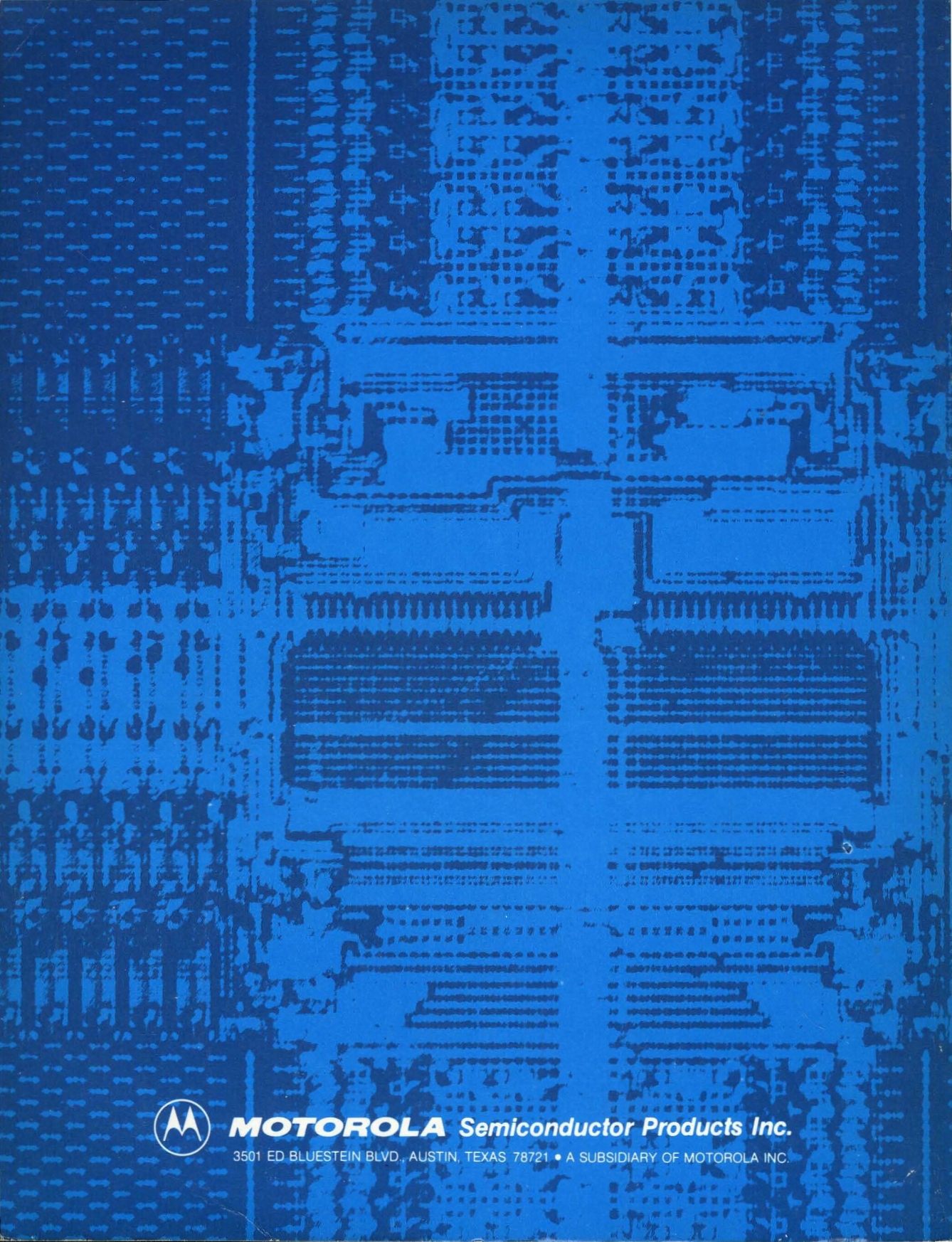

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